SPIE. ADVANCED LITHOGRAPHY+ PATTERNING

26 February–2 March 2023
San Jose Convention Center
San Jose, CA

SUBMIT ABSTRACTS BY
14 SEPTEMBER 2022
Share your research and make important connections throughout the semiconductor industry

Present your work in optical lithography, metrology, or EUV. Share advancements at the meeting where leaders come to network and solve lithography and patterning challenges. We look forward to gathering with you in San Jose.

Submit your abstract today: [www.spie.org/al23call](http://www.spie.org/al23call)
Plan to participate

The SPIE Advanced Lithography + Patterning Symposium has been the showcase of the latest advances in lithography and patterning technology for over four decades. The technology landscape keeps on evolving to incubate more sophisticated and diversified information and computing technologies. The semiconductor technology sector, now in the More-than-Moore era, is facing more challenges that require holistic patterning solutions that involve a higher level of interactions among process technologies, devices, and system design sectors. The 2023 symposium will cover the full spectrum of the advances and challenges in state-of-the-art lithography and integrated patterning technology through several topical conferences. Advances in areas of nano- and micro-patterning for semiconductor IC device applications will be presented in sessions covering optical lithography, extreme-UV (EUV) lithography, computational patterning, metrology/inspection, patterning materials, etch/deposition technology, and System-Design-Technology co-optimization. As novel patterning and non-IC lithography technologies, such as heterogenous wafer packaging, IoT devices including micro-machines and microsensors, AR/VR devices, FP Displays, have become more widely explored, related topics in these areas are also addressed.

To cope with the changes in the technology landscape and to better serve as the premium platform for bringing together the lithography and patterning communities involved with semiconductor devices, micro-/nano-systems, AR/VR devices, displays, and related fields, the 2023 symposium is carefully structured into six functionally distinct conferences that are organized by current practitioners of the art working together with organizing committees of experts in these fields. Joint sessions between the conferences will be aligned with several predefined Application Tracks: machine learning, stochastic effects, and overlay. These Application Tracks will offer attendees the opportunity to cover important topics common across these interest areas and minimize presentation overlap.

Participants come from a broad array of backgrounds to share and learn about state-of-the-art advances of all aspects of patterning technologies. Through a series of provocative panel discussions and seminars, the meeting also probes current issues being faced as we extend current methods, move toward alternative approaches, and identify new ways to complement one technology with another. This meeting also provides the unique and primary forum for meeting and interacting with a wide range of industry experts, researchers, academics, and key players working on patterning technology development. Attendance ensures that participants learn and share the latest developments in areas of central importance to many vital technology fields. We welcome your participation for SPIE Advanced Lithography and Patterning 2023 and urge you to submit your abstracts to the appropriate conference as described in each conference's call for papers and encourage your colleagues to do the same. Relevant topics for new technology groups, keynote talks, or panel discussions are also solicited.

The 2023 meeting recognizes the importance of fostering a new generation of innovative and strongly skilled lithographers and patterning engineers for the development of electronic and photonic devices and systems technology to advance the digital age. We are offering, for the third year, a student grant program to waive students' registration and subsidize travel expenses. We have established a one-on-one student mentor pairing program aiming to connect technology leaders with students to guide the latter in exploring and planning to succeed in this industry. We would like to engage with academia to encourage and equip students to participate in this ever-exciting and rewarding symposium and career.

2022 Symposium Chairs

Kafai Lai
Univ. of Hong Kong (USA)
Symposium Chair

Qinghuang Lin
LAM Research Corp. (USA)
Symposium Co-Chair
The premier event for the lithography community

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SPIE remains committed to advancing light-based research and meeting the needs of our constituents by providing you with an opportunity for sharing your work and connecting you with the global science and engineering community. We look forward to your participation.
For over fifty years photolithography has been at the center of the growth of the semiconductor industry. The art of shaping matter with photons influences the way we live today and the drive into the future. The need for more powerful chips and greater memory storage has driven the evolution of advanced lithography tooling, photomasks, processes, and systems. The advent of extreme ultraviolet lithography (EUV) at 13.5nm wavelength and its introduction into high-volume manufacturing (HVM) ensures the extendibility of lithography to tighter dimensions for the fabrication of more powerful devices and support the exponential growth of data management. Its use in conjunction with optical lithography (g-line, i-line, KrF, ArF) enables a wide range of resolution for new devices in an ever-increasing array of applications, like AI, IoT, silicon photonics, MEMS, etc.

The Optical and EUV Nanolithography XXXVI conference covers both EUV and optical projection-based lithography systems, practices, and their applications in IC technology. It is the leading forum for scientists and engineers from around the world to present and discuss research on the advancement of lithography technologies. We welcome technical and scientific papers in the following areas:

**LITHOGRAPHY EQUIPMENT**
- optical lithography equipment
- optical mask-less exposure tools
- optical and EUV tool design and innovation
- high-NA EUV imaging systems
- throughput, defectivity, and productivity
- imaging performance
- focus, dose, overlay control, and budgets
- aberrations, flare, and out-of-band light.

**SOURCES**
- light sources for EUV and optical lithography systems
- power scaling of EUV sources
- efficiency and reliability
- source characterization
- EUV source collectors, cleaning, and lifetime.

**MASKS**
- substrates and blanks
- patterned and blank mask inspection
- actinic, e-beam, and DUV inspection methods
- defect characterization, mitigation, and repair
- optical and EUV mask absorber materials and patterning
- mask process
- mask roughness
Optical and EUV Nanolithography XXXVI (AL101) continued

- pellicle development and platform integration
- mask architectures for higher numerical apertures
- mask writing techniques
- mask design fit to multi-beam mask writers.

PATTERNING
- optical system and mask induced defect, electrical, and yield signatures
- resolution enhancement techniques
- imaging simulations and source-mask optimization (SMO)
- optical and EUV lithography mixing
- EUV to optical matching
- multi-patterning, 193i, and EUVL
- edge placement control
- on-product overlay control
- EUV process optimization
- stochastics control.

SYSTEMS FOR IOT, ADVANCED PACKAGING AND HETEROGENEOUS INTEGRATION
- equipment design and characterization for non-IC applications
- light sources for non-IC applications
- mask technology for non-IC applications.

Students submitting papers to Optical and EUV Nanolithography XXXVI will be considered for the ASML Best Student Paper. This award is given each year at this conference and recognizes extraordinary work achieved by students interested in the photolithography field, and strongly supports the contributions made to scientific advancement at the conference. The award includes a plaque along with a monetary award to help the student’s future research activities.

THE NICK COBB MEMORIAL SCHOLARSHIP
An annual award of US$10,000 supporting the education of a graduate student studying in a field related to advanced lithography.

Jointly funded by SPIE and Siemens EDA.

Nick Cobb
The scholarship honors the memory of Nick Cobb, an SPIE Senior Member and chief engineer at Mentor Graphics—now Siemens EDA—and his groundbreaking contributions enabling optical and process proximity correction for IC manufacturing.

SIEMENS
Siemens EDA will also provide the winner travel support to SPIE Advanced Lithography + Patterning 2023 to receive the award.

Learn more: spie.org/nickcobb
CALL FOR PAPERS

DTCO and Computational Patterning II (AL102)

Conference Chair: Ryoung-Han Kim, IMEC (Belgium)
Conference Co-Chair: Neal V. Lafferty, Mentor, a Siemens Business (USA)

Program Committee: Jason P. Cain, Advanced Micro Devices, Inc. (USA); Luigi Capodieci, Motivo, Inc. (USA); Lifu Chang, MOSIS Integrated Circuit Fabrication Service (USA); Dan J. Dechene, IBM Thomas J. Watson Research Ctr. (USA); David M. Fried, Lam Research Corp. (USA); Yuri Granik, Siemens Industry Software Inc. (USA); Harsha Grunes, Intel Corp. (USA); Sridiya Jayaram, Mentor, a Siemens Business (USA); Seongtae Jeong, SAMSUNG Electronics Co., Ltd. (USA); Sungwoo Ko, SK Hynix, Inc. (Korea, Republic of); Sachiko Kobayashi, KIOXIA Corp. (Japan); Kafai Lai, The Univ. of Hong Kong (USA); Ya-Chieh Lai, Cadence Design Systems, Inc. (USA); Lars W. Liebmann, TEL Technology Ctr., America, LLC (USA); Kevin Lucas, Synopsys, Inc. (USA); Larry Melvin, Intel Corp. (USA); Shigeki Nojima, KIOXIA Corp. (Japan); Vivek K. Singh, Intel Corp. (USA); Seung Chul Song, Qualcomm (USA); Kunal N. Taravade, Synopsys, Inc. (USA); Chun-Ming Wang, Western Digital Corp. (USA); Lynn T. Wang, GLOBALFOUNDRIES Inc. (USA); Yayi Wei, Institute of Microelectronics, Chinese Academy of Sciences (USA); Chi-Min Yuan, NXP Semiconductors (USA)

The 2023 Design Technology Co-Optimization (DTCO) and Computational Patterning conference at SPIE Advanced Lithography and Patterning is calling for papers. Topics including design technology co-optimization (DTCO), system technology co-optimization (STCO), design for manufacturability (DFM), design for yield (DFY), computational patterning, deep learning and machine learning, and modeling to co-optimize design and technology to improve chip power, performance, area, and cost are encouraged as focus. In addition, academic topics potentially relevant to the semiconductor industry are encouraged to submit. Topics of interest include, but are not limited to:

DESIGN TECHNOLOGY CO-OPTIMIZATION (DTCO) AND SYSTEM TECHNOLOGY CO-OPTIMIZATION (STCO)
- pattern-based design optimization
- design-intent to manufacturing
- performance-power-manufacturability optimization
- layout style and lithography co-optimization (including optical source and design co-optimization)
- design for novel patterning process
- design optimization for technology
- DTCO for standard cells and memory including standard cell, SRAM, and digital designs
- STCO and 3D integration
- 3D packaging, integration and heterogeneous integration and its impact to design, DFM, OPC and other fields.

DESIGN FOR MANUFACTURING (DFM), DESIGN FOR YIELD (DFY): TECHNOLOGY, IP AND SYSTEM
- physical layout optimization
- design rule development strategies and methodologies
- layout optimization for systematic and random yield loss reduction
- layout optimization for minimizing circuit variability
- design and verification methodologies including hot spot analysis
- manufacturing friendly circuit design styles and methodologies
- design-to-manufacturing methodologies for analog circuits, MEMS, and other microlithography applications
- design-to-manufacturing economics
- cost-performance tradeoffs between design and manufacturing
- design-to-manufacturing flow methodologies for productivity improvement, time-to-market, and cost reduction
- DFM for “more than Moore” applications (analog, RF, digital/SoC, etc.).

COMPUTATIONAL PATTERNING (EUV AND DUV)
- computational patterning consideration for anamorphic high-NA EUV, including stitching impacts on design and DTCO applications for mitigation
- new approaches for multi-patterning, decomposition, and interaction with design and patterning
- propagating electrical design intent for RET/OPC and manufacturing optimization and verification.

DEEP LEARNING, MACHINE LEARNING, AND AI TECHNIQUES
- machine learning on design, process, mask, and OPC methodologies
- new machine learning concepts and algorithms that are potentially applicable to semiconductor industry
- data analytics for layout analysis and optimization or process modeling and control.

MODELING, SIMULATION, AND COMPUTATION
- modeling for accuracy and defect detection
- applications of new computation architectures such as quantum computing, TPU, etc.

Submit your abstract today: spie.org/al23call
Publishing peer-reviewed papers on lithography and patterning topics

Harry Levinson
HJL Lithography, USA
Editor-in-Chief

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Metrology, Inspection, and Process Control
XXXVII (AL103)

Conference Chair: John C. Robinson, KLA Corp. (USA)
Conference Co-Chair: Matthew J. Sendelbach, TEL Technology Ctr., America, LLC (USA)

Program Committee: Ofer Adan, Applied Materials Israel, Ltd. (Israel); John A. Allgair, BRIDG (USA); Masafumi Asano, Tokyo Electron Ltd. (Japan); Bryan M. Barnes, National Institute of Standards and Technology (USA); Cornel Bozdag, Micron Technology, Inc. (USA); Benjamin D. Bunday, AMAG Consulting, LLC (USA); Xiaomeng Chen, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); Hugo Cramer, ASML Netherlands B.V. (Netherlands); Timothy F. Crimmins, Intel Corp. (USA); Shunsuke Koshihara, Hitachi High-Technologies Corp. (Japan); Yi-Sha Ku, Industrial Technology Research Institute (Taiwan); Byoung-Ho Lee, SK hynix, Inc. (Korea, Republic of); Myungjun Lee, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Philippe Leray, IMEC (Belgium); Narender Rana, Western Digital Corp. (USA); Christopher J. Raymond, Ono Innovation Inc. (USA); Daniel Schmidt, IBM Thomas J. Watson Research Ctr. (USA); Nivea G. Schuch, ASELTA Nanographics (France); Alexander Starikov, I&I Consulting (USA); Alok Vaid, GLOBALFOUNDRIES Inc. (USA)

Metrology-based analysis, identification, and control of error sources continue to enable rapid evolution of lithography and patterning. Metrology of exposure dose and focus supports ever-smaller process windows. Dimensional metrology in layouts facilitates resolution enhancement and validation of control. Extremely tight overlay is required for multiple patterning. Development of materials, equipment, and processing in EUV, direct-write, nanoimprint, directed self-assembly, etch, and deposition drive further innovation of metrology tools and applications.

This conference is the leading forum for the exchange of foundational information and discussion of novel concepts in patterning-related metrology, inspection, and process control. Consistent with the conference charter and goals, please submit original technical papers in these and related technology areas:

METROLOGY AND INSPECTION
• optical full-field and scanned microscopy, scatterometry, and interference microscopy
• novel measurement techniques with high-resolution optics, scatterometry, SEM, AFM, x-ray
• particle-beam scanned microscopy, materials characterization, and elemental analysis
• design rules, design compliance, hot spots, design-based metrology and inspection
• metrology for design rules and process margins, budgeting, and budget control
• metrology for lithography development, patterning model build, and validation
• metrology on photomasks, including pre-compensation, OPC, and phase shifting
• machine learning in metrology and inspection for capability and productivity
• hybrid metrology, including computational or virtual metrology
• parametric electrical testing and other device performance-based metrology
• applications in emerging patterning technologies including optical immersion and EUV lithography, direct-write, nano-imprint, and directed self-assembly
• applications in manufacturing of ICs, cell stacking, wafer bonding, TSV and 3D integration, displays, thin-film heads, MEMS, MOEMS, bio-arrays, lab-on-the-chip, integrated optoelectronics and other micro- and nano-systems.

CRITICAL DIMENSION, PATTERN PLACEMENT, AND OVERLAY
• 1D, 2D, and 3D metrology of CD and pattern placement, including within device layouts
• alignment, registration and overlay metrology, processing and metrology integration
• feature edge, edge profile and edge position, roughness of edge, width, and centerline
• optical, SEM, and AFM based in-die overlay on small targets and devices.

MEASUREMENT SYSTEM MODELING AND SIMULATION
• physics and mathematical models of metrology process and detection methods
• physical characterization of both systems and samples, model parameters
• data analysis methods, library-based image analysis, and algorithms.

CALIBRATION AND ACCURACY
• metrology quality, error diagnostics, and data culling
• measurement resolution and error, including precision and accuracy
• standards and reference materials, calibration methods, hybrid metrologies
• reference measurement systems and metrology comparisons
• tool fleet performance, maintenance, and matching.

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CALL FOR PAPERS
PROCESS CHARACTERIZATION, CONTROL, PERFORMANCE, AND YIELD
• process metrology and monitors, segmentation, and reduction of variance
• metrology sampling, excursion detection, costs, device performance, and yield
• data analysis and visualization, modeling and fingerprint detection
• advanced process control, data feedback, and feed forward
• big data analysis and diagnostic methodologies, data management.
DEFECT DETECTION, ANALYSIS, AND CONTROL
• detection and control of systematic, random, and low photon count stochastic pattern defects
• defect review, defect reduction, yield improvement, and effective data use
• artificial intelligence and machine learning applied to defect detection, analysis, and control
• environmental contamination, including impacts on processing and defects.
PERFORMANCE LIMITS IN METROLOGY AND INSPECTION
• responses to commanded skews and cross-technology comparisons
• models of tool-sample interaction, noise, and error mechanisms.

SAVE THE DATE
Abstracts Due: 14 September 2022
Author Notification: 21 November 2022
The contact author will be notified of acceptance by email.
Manuscript Due Date: 8 February 2023

PLEASE NOTE: Submission implies the intent of at least one author to register, attend the conference, present the paper as scheduled, and submit a full-length manuscript for publication in the conference proceedings.

THE DIANA NYYSSONEN MEMORIAL BEST PAPER AWARD
The Diana Nyssssonen Memorial Best Paper Award is intended to honor the best paper of the Conference on Metrology, Inspection, and Process Control. It recognizes the most significant contribution to the field, based on the technical merit and persuasiveness of the oral presentation, as well as on the overall quality of the paper published in the conference proceedings. The Diana Nyssssonen Memorial Award consists of an SPIE citation and an honorarium.
Award Sponsored by Hitachi

THE KAREL URBÁNEK BEST STUDENT PAPER AWARD
The Karel Urbánek Best Student Paper Award recognizes the most promising contribution to the field by a student, based on the technical merit and persuasiveness of the paper presentation at the conference. The Karel Urbánek Best Student Paper Award consists of an SPIE citation and an honorarium.
To be eligible, the leading author and presenter of the paper must be a student. To establish eligibility, the principal author’s bio submitted with the abstract must state the academic status and the institution, as well as the advisor’s name and contact information.
Award Sponsored by KLA

THE VLADIMIR UKRAINTSEV AWARD FOR COLLABORATIONS IN METROLOGY
The newly established Vladimir Ukraintsev Award for Collaborations in Metrology recognizes the most significant publication on inter-disciplinary explorations of metrology accuracy, round-robin studies, dissemination of best-known methods, and other industry collaborations. The recipient to be determined by the Metrology, Inspection, and Process Control program committee occasionally, as warranted, based on potential to influence the industry by an oral or poster presentation and conference proceedings paper. The Vladimir Ukraintsev Award for Collaborations in Metrology, when awarded, will be presented at the subsequent year’s conference.
Novel Patterning Technologies 2023 (AL104)

Conference Chair:  J. Alexander Liddle, National Institute of Standards and Technology (USA)

Conference Co-Chair:  Ricardo Ruiz, Lawrence Berkeley National Lab. (USA)

Program Committee:  Alan D. Brodie, KLA Corp. (USA); Tito L. Busani, The Univ. of New Mexico (USA); Richard A. Farrell, Facebook Inc. (USA); Sandip Halder, imec (Belgium); Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan); Daniel J. C. Herr, The Univ. of North Carolina at Greensboro (USA); Tatsushiko Higashiki, KIOXIA Corp. (Japan); EriK R. Hosler, PsiQuantum Corp. (USA); Koji Ichimura, Dai Nippon Printing Co., Ltd. (Japan); Stephen M. Kuebler, Univ. of Central Florida (USA); Chi-Chun Liu, IBM Corp. (USA); Hans Loeschnier, IMS Nanofabrication GmbH (Austria); Laurent Pain, CEA-LETI (France); Eric M. Panning, Intel Corp. (USA); Ivo W. Rangelow, Technische Univ. Ilmenau (Germany); Douglas J. Resnick, Canon Nanotechnologies, Inc. (USA); Martha I. Sanchez, Applied Materials, Inc. (USA); Chandrasekhar Sarma, Intel Corp. (USA); Gurpreet Singh, Intel Corp. (USA); Ines A. Stolberg, Vistec Electron Beam GmbH (Germany); Mark A. van de Kerkhof, ASML Netherlands B.V. (Netherlands); Niels Wijnaendts van Resandt, Heidelberg Instruments Inc. (USA).

New solutions to meet current and future patterning challenges are critical to extend scale, complement existing approaches, and enable functional patterning for emerging and convergent applications, e.g., More-than-Moore. The Novel Patterning conference brings together expertise from a diverse group of industry/academia leaders within and outside the semiconductor field. This conference is an opportunity to present new ideas as well as learn more about the core challenges in advanced patterning.

This conference on novel patterning showcases novel lithography and patterning techniques that provide solutions for semiconductor IC nodes, wafer-level packaging, and non-IC related and adjacent technologies, e.g., health care, communications, energy, etc., such as MEMS/NEMS, MOEMS, displays, photonics, metamaterials, AR/VR, and micro/nanofluidics. Approaches, including maskless, roll-to-roll, 3D printing, DNA-based and colloidal self-assembly, and additive manufacturing, are welcome. Contributions are also sought which describe hybrid approaches employing a combination of lithographic aerial imaging and patterning processes such as self-aligned pitch division, tone-reversals, selective depositions, directed self-assembly, including novel approaches that demonstrate the feasibility of the bio-inspired assembly of functional nanomaterials, etc.

APPLICATION AREAS FOR NOVEL PATTERNING TECHNOLOGIES
• functional nanopatterning materials and emerging IoT applications
• novel patterning for semiconductor 7nm IC nodes and beyond
• MEMS/NEMS, MOEMS, and Microsystems
• metasurfaces and metamaterials
• photonic and/or phononic crystals
• micro/nanofluidics, lab-on-a-chip, or other bio-applications
• digital micro-mirror arrays
• multi-beam writing of masks and master templates
• semiconductor wafer-level packaging and fan-out
• bioelectronics and genomics/proteomics
• photovoltaics and related energy applications
• large-area display/flat-panel displays
• roll-to-roll/web format device manufacturing
• micro LED array fabrication
• nanopatterned sensors, waveguides, antennas
• building blocks for defect-tolerant computing
• smart resists and self-healing materials
• tools/materials to improve existing scanner performance
• quantum computing devices and qubit-technologies
• 3D integration and materials
• neuromorphic and emerging memory patterning
• atomistic nanoelectronic devices.

TECHNOLOGY AREAS FOR NOVEL PATTERNING APPLICATIONS
DIRECT WRITE OR MASKLESS LITHOGRAPHY AND PATTERNING TECHNOLOGIES
• electron or ion charged-particle beams
• optical beams
• STED, multi-color/multi-photon direct write
• resistless e-beam or ion beam direct patterning
• beam-directed nucleation, ion-beam deposition
• material ablation or material transformation reactions
• ink-jet
• scanning probe lithography, dip-pen printing, tip-based patterning
• interference, plasmonic or nearfield/evanescent wave lithography
• micromirror optical lithography
• 3D metal or ceramic sintering.

PROCESS-BASED LITHOGRAPHY AND PATTERNING
• directed self-assembly
• nanoimprint lithography
• selective deposition
• self-aligned or pitch division process integration techniques
• colloidal self-assembly and DNA patterning
• 3D patterning.

In the spirit of facilitating exchange of knowledge, we strongly encourage contributions that provide a background to the technology, details on latest results and a clear indication of the limitations/opportunities for future development.

Submit your abstract today: spie.org/al23call

Tel: +1 360 676 3290 • help@spie.org • #SPIElitho
The Advances in Patterning Materials and Processes conference is the leading forum for scientists and engineers from institutes, material as well as equipment vendors, and end-users around the world to present and discuss research on the chemistry, physics, and performance of photoresists and patterning materials and processes. Evolutionary and ultimately revolutionary innovations will continue to be required in materials and patterning processes in order to achieve the combination of resolution, edge roughness, and sensitivity required for future technology nodes and innovative emerging technologies.

This conference welcomes submissions of original papers that emphasize recent advances in high-performance patterning processes and materials and their integration in established, maturing, emerging, and new lithographic technologies including patterning for augmented reality (AR) and virtual reality (VR) applications. Original technical papers are solicited, but not limited to the following topics:

**PATTERNING MATERIALS, PROCESSES, AND APPLICATIONS**
- photoresists for EUV and 193nm (immersion) lithography
- photoresists for other wavelengths: electron beam or other maskless lithography, 248nm, i-line, and g-line
- novel development techniques: positive and negative tone (PTD, NTD) resists and developers, solvent, aqueous, or dry development processes
- multi-layer patterning materials: underlayers for reflection control, planarization, pattern transfer, and process enhancement
- selective deposition and surface modification of organic and inorganic materials: chemistry, processing, and materials science, bottom-up approaches
- self-assembling materials (DSA): chemistry and materials science, processing, and ancillary materials
- materials and processes used in vertical integration of novel devices, stacked structures, nanosheets, nanotubes, solvent based or dry processes
- materials for packaging and SOC/SIP integration
- materials for patterning and optical control of AR/VR applications
- PFAS/PFOS alternative materials, roadmap for dealing with regulatory legislation and plans for phasing out of these materials by the supplier community.

**PROCESSING AND PROCESS CONTROL**
- single and multiple patterning
- resist smoothing, rectification, trim and shrink, and tone inversion
- applied processing, including filtration, defect control, and pattern collapse mitigation
- materials challenges related to etch, process control, and metrology
- new processing techniques and applications, especially self-aligned and additive strategies.

Submit your abstract today: [spie.org/al23call](https://spie.org/al23call)
**SIMULATION AND MODELING**
- resist fundamentals and assessment of patterning and materials scaling limits
- variability, stochastics, and defectivity
- design for or simulation of new processes and applications
- AI and ML approaches to materials design, characterization, patterning, and process control.

Consistent with the conference’s charter and goals, authors are required to provide a description of chemical and physical principles as well as sufficient chemical structural detail in presented work. Submissions which do not reveal sufficient chemical details so as to add value to the readers or are principally of a commercial nature may not be accepted for presentation and publication.

**CALL FOR PAPERS**

**Abstracts Due:**
14 September 2022

**Author Notification:**
21 November 2022
The contact author will be notified of acceptance by email.

**Manuscript Due Date:**
8 February 2023

**PLEASE NOTE:** Submission implies the intent of at least one author to register, attend the conference, present the paper as scheduled, and submit a full-length manuscript for publication in the conference proceedings.

**AWARDS**

Each year the SPIE Patterning Materials and Processes Conference recognizes the outstanding oral, poster, and student submissions from the prior year’s conference via three distinguished awards:

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**C. GRANT WILLSON BEST PAPER AWARD IN PATTERNING MATERIALS AND PROCESSES**
The C. Grant Willson Best Paper Award in Patterning Materials and Processes recognizes the best oral paper presented at the previous year. Candidate papers are nominated and selected by the SPIE Patterning Materials conference committee. Judging criteria include the technical originality, completeness, relevance, quality of oral presentation, and quality of proceedings manuscript. Invited keynote talks are not eligible. The award consists of a certificate and a cash honorarium of $1,000 USD.

Award sponsored by

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**JEFFREY BYERS BEST POSTER AWARD IN PATTERNING MATERIALS AND PROCESSES**
The Jeffrey Byers Best Poster Award in Patterning Materials and Processes recognizes the best poster presented at the previous year. Candidate posters are nominated and selected by the SPIE Patterning Materials conference committee. Judging criteria include the technical originality, completeness, relevance, quality of poster presentation, and quality of proceedings manuscript. The award consists of a certificate and a cash honorarium of $750 USD.

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**HIROSHI ITO STUDENT AWARD IN PATTERNING MATERIALS AND PROCESSES**
The Hiroshi Ito Student Award in Patterning Materials and Processes recognizes the best student paper presented at the previous year. Candidate papers are nominated and selected by the SPIE Patterning Materials conference committee. To be eligible, the primary and presenting author must be a student or post-doc at the time of the conference. Judging criteria include the technical originality, completeness, relevance, quality of presentation, and quality of proceedings manuscript. Both oral and poster submissions are eligible; however, the award will not be given to a submission that is a concurrent winner of the Willson or Byers Awards. The award consists of a certificate and a cash honorarium of $1,000 USD.

Award sponsored by
The revolution in microelectronics over the last fifty years of Moore’s Law has been led by continued acceleration in dimensional scaling of logic and memory semiconductor devices. Dramatic innovations in optical and now extreme ultraviolet lithography in conjunction with novel process integration strategies have been the driving force behind much of the success of dimensional scaling. Plasmas have become the primary patterning method for foundry and advanced technology nodes, with plasma etch and deposition being key to an overall patterning strategy to create new opportunities in “complementary patterning” for the basic elements common to all patterns (lines, spaces, holes). Novel integration strategies take the basic elements to the next level by enabling more complex structures with high fidelity.

This new paradigm in scaling defines the patterning era, utilizing innovative plasma processing techniques and novel process integration to dramatically extend the achievable pattern design, dimension, and fidelity. Plasma-based processes including both etch and deposition are key to an overall patterning strategy to create new opportunities in “complementary patterning” for the basic elements common to all patterns (lines, spaces, holes). Novel integration strategies take the basic elements to the next level by enabling more complex structures with high fidelity.

This increasing interdependence of lithography technologies, photoresist technologies, plasma etch, and deposition technologies has created new opportunities in materials, integration, and the co-optimization of plasma-based patterning with lithography and process control. Historically distinct from optical imaging, the new role of these plasma-based techniques and process integration in defining critical features on-device has driven a need for more intelligent process control and automated development.

**ORIGINAL AND OVERVIEW TECHNICAL PAPERS ARE SOLICITED ON, BUT NOT LIMITED TO, THE FOLLOWING TOPICS:**

- novel discoveries of plasma-material interactions: plasma-photosresist interactions, LER/LWR/stochastics mitigation, MOL/BEOL (low-k) material interactions, novel substrate material handling (SiGe, III-V, C, nonvolatile memory) etc.
- etch challenges for 3D memory and logic architectures
- defect reduction or yield enhancement techniques by dry or wet process solutions
- new etch methodologies and their application to patterning processes, e.g.: atomic layer etching (ALE), low Te processing, high aspect ratio pattern definition, selective deposition
- patterning control through advanced process solutions: in-situ process control, process simulations, etch-aware OPC, edge place error (EPE) etc.
- machine-learning-based methodologies for process or equipment development for patterning
- novel integration strategies for pattern fidelity improvement, new design enablement, etc.
- advanced patterning, process, and selective deposition tools and processes for novel etch-pattern transfer applications
- applications of novel patterning transfer techniques to improve mask variability
- novel holistic (litho, etch, and deposition) patterning solutions for logic and memory applications
- advanced patterning solutions for emerging product applications including but not limited to: AR/VR, neuromorphic computing, quantum computing, power semiconductors (GaN, others), IoT devices, MEMS, MOEMS, other “more than Moore devices” and derivative technologies (RF, analog or mixed signal)
- advanced integration and patterning solutions for photonic devices including photonic integrated circuit devices operating at IR, NIR or visible wavelength range; LED device technology for display technology
- advances in etch or patterning technology that enables sustainability goals for the semiconductor industry.
Abstracts with a preview of results and conclusions supported by technical data are favored for oral presentation.

SESSIONS FROM 2022
- Materials and Etch Integration
- Computational Patterning and Patterning Process Control
- Atomic Layer Etching and Novel Plasma Techniques
- Joint EUV Patterning and Etch
- Patterning Solutions for Emerging Applications
- Advanced Patterning Integration.

SESSIONS FOR 2023
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- Patterning Solutions for Emerging Applications
- Advanced Patterning Integration
- Area-Selective Atomic Layer Deposition/Etching
- Highly Selective Radical Etch
- Patterning-Induced Damage
- Sustainability in Etch and Patterning Integration.

THE ADVANCED ETCH TECHNOLOGY AND PROCESS INTEGRATION BEST PAPER AWARD
New for this year, the Advanced Etch Technology and Process Integration conference will offer a Best Paper Award. All submitted papers selected for oral presentations will be considered for the award. The award will recognize the paper with the most significant contribution and innovation for solving advanced patterning challenges and the quality of the oral presentation. The award will include a certificate and monetary gift.

GENERAL INFORMATION

TECHNICAL PROGRAM
Available November 2022
The comprehensive advance technical program will list conferences, paper titles, and authors in order of presentation. The program will outline all planned special events and hotel and registration information.

REGISTRATION
All participants, including invited speakers, contributed speakers, session chairs, co-chairs, and committee members must pay a registration fee.

Fee information for conferences, courses, a registration form, and technical and general information will be available online in November 2022.

HOTELS
Opening of the hotel reservation process for this meeting is scheduled for November 2022. SPIE will arrange special discounted hotel rates for attendees that will be available when housing opens. Please do not call SPIE for information. The SPIE website will be kept current with any updates.

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Present your research at SPIE Advanced Lithography + Patterning

Below are abstract submission instructions, the accompanying submission agreement, conference presentation guidelines, and guidelines for publishing in the Proceedings of SPIE on the SPIE Digital Library. Submissions subject to chair approval.

Important dates

<table>
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<tr>
<th>Event</th>
<th>Date</th>
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<tr>
<td>Abstracts due</td>
<td>14 September 2022</td>
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<tr>
<td>Registration opens</td>
<td>November 2022</td>
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<td>Author notification and program posts online</td>
<td>21 November 2022</td>
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<td>Submission system opens for manuscripts and poster PDFs*</td>
<td>19 December 2022</td>
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<tr>
<td>Post-deadline abstracts due: Submit via conference listings</td>
<td>9 January 2023</td>
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<td>Poster PDFs due for spie.org preview and publication</td>
<td>1 February 2023</td>
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<td>Manuscript due</td>
<td>8 February 2023</td>
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<tr>
<td>Advance upload deadline for oral presentation slides**</td>
<td>24 February 2023</td>
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*Contact author or speaker must register prior to uploading

**After this date slides must be uploaded onsite at Speaker Check-In

What you will need to submit

- Title
- Author(s) information
- 250-word abstract for technical review
- 100-word summary for the program
- Keywords used in search for your paper (optional)
- Check the individual conference Call for Papers for additional requirements (for example, some conferences require 2- to 3-page extended summary for technical review, or have instructions for award competitions)

Note: Only original material should be submitted. Commercial papers, papers with no new research/development content, and papers with proprietary restrictions will not be accepted for presentation.

How to submit your abstract

- For example, visit the conference page: [www.spie.org/AL101call](http://www.spie.org/AL101call)
- You may submit more than one abstract but submit each abstract only once.
- Click the “Submit An Abstract” button on the conference page.
- Sign in to your SPIE account or create an account if you do not already have one.
- Follow the steps in the submission wizard until the submission process is completed.

Submission agreement

All presenting authors, including keynote, invited, oral, and poster presenters, agree to the following conditions by submitting an abstract:

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- Poster presenters: submit a poster PDF and optional preview video, by the advertised due dates, for publication in the Proceedings of SPIE in the SPIE Digital Library; poster PDFs may also be published and viewable in the spie.org program during and immediately after the event
- Submit a 4-page-minimum manuscript, by the advertised due date, for publication in the Proceedings of SPIE in the SPIE Digital Library
- Obtain funding for registration fees, travel, and accommodations
- Ensure that all clearances, including government and company clearance, have been obtained to present and publish. If you are a DoD contractor in the USA, allow at least 60 days for clearance
- Attend the meeting
- Present at the scheduled time
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Novel Patterning Technologies 2023
Advances in Patterning Materials and Processes
Advanced Etch Technology and Process Integration for Nanopatterning

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