Modeling of charging effect and its correction by EB mask writer EBM-6000

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ABSTRACT
The impending need of double patterning/double exposure techniques is accelerating the demand for higher pattern placement accuracy to be achieved in the upcoming lithography generations. One of the biggest error sources of pattern placement accuracy on an EB mask writer is the resist charging effect. In this paper, we provide a model to describe the resist charging behavior on a photomask written on our EBM-6000 system. We found this model was very effective in correcting and reducing the beam position error induced by the charging effect.

1. Introduction
Double patterning and double exposure techniques are to allow extension of 193nm optical lithography to the hp 32nm node. Both techniques require tighter pattern placement accuracy, including the improved overlay accuracy between two photomasks. One of the biggest error sources in overlaying two photomasks, which is inherent to e-beam lithography, is the resist surface charging effect. With the typically used 200~300nm resist thickness and 50keV e-beam, the resist surface charging can deflect the beam position in excess of 10nm. This position error induced by charging effect is strongly dependent upon the figure density variation within the pattern data, therefore, this error source results in a systematic and repeatable pattern placement error.

Currently, the most reliable method to remove the surface charging is to coat a “Charge Dissipation Layer (CDL)” on top of the resist layer. However, CDL has such drawbacks as:

• Adding a new layer can potentially induce another source of contamination defects;
• The fundamental characteristics of CDL are those of acid, and therefore it absolutely is not a good friend of chemically amplified resist (CAR);
• Users must purchase additional coating equipment adding cost to what is already said to be substantially high mask making cost.

Continues on page 3.
Is the BACUS Symposium Focus Still Relevant?

Peter D. Buck, Toppan Photomasks, Inc.

This is my second year on the BACUS Symposium Program Committee, and having been completely overwhelmed by the task of reviewing the abstracts submitted for last year’s Symposium, this year I decided to take a more systematic approach. I ranked the abstracts for relevance to the mask industry based on a set of semi-objective criteria I defined as follows:

<table>
<thead>
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<th>Rank</th>
<th>Relevance</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>5</td>
<td>Directly about mask manufacturing methods, techniques, problems, solutions</td>
<td>29%</td>
</tr>
<tr>
<td>4</td>
<td>About the use of masks in the manufacturing of integrated circuits</td>
<td>14%</td>
</tr>
<tr>
<td>3</td>
<td>Describes mask manufacturing tools, their design, characterization and performance</td>
<td>8%</td>
</tr>
<tr>
<td>2</td>
<td>The abstract mentions masks however briefly or obliquely</td>
<td>28%</td>
</tr>
<tr>
<td>1</td>
<td>Nothing remotely to do with masks, mask manufacturing or mask use, doesn’t even mention masks</td>
<td>21%</td>
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My justification for this personal ranking system is based on the assumption that the BACUS Symposium has traditionally been and should continue to be primarily about the technology related to the manufacturing and use of photomasks, secondarily about the commercial aspects of the industry (tools and materials) and least about everything else. After all, the official conference name is “Photomask Technology” and the invitation refers to “…latest developments and innovation in photomask research, design, processing, and manufacturing solutions.”

After reviewing the abstracts and looking at the statistics, I found the following breakdown:

<table>
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<th>Rank</th>
<th>Relevance</th>
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<tbody>
<tr>
<td>5</td>
<td>Mask manufacturing</td>
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<td>4</td>
<td>Mask use</td>
<td>14%</td>
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<tr>
<td>3</td>
<td>Mask tools</td>
<td>28%</td>
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<tr>
<td>2</td>
<td>Mentions masks</td>
<td>8%</td>
</tr>
<tr>
<td>1</td>
<td>No relevance</td>
<td>21%</td>
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Almost two thirds of the papers have strong relevance to our industry according to the criteria noted previously; the other third is about other topics, primarily OPC and DFM.

If I sort by source I find that 37% of abstracts were submitted by IC and mask manufacturers while suppliers submitted another 40%. There is little participation from academia at 8%. Does this indicate a mature industry focused primarily on solving manufacturing problems with a declining emphasis on innovation?

Fourteen percent of the submissions are from EDA software suppliers including most of the “no relevance” papers. Our symposium is being gradually taken over by topics not directly related to the mask industry if you accept my narrowly defined criteria. Even our 2008 Symposium keynote speaker is from the EDA industry. This is an observation, not a criticism.

Perhaps it is time to re-charter the BACUS Symposium as a technical forum focused on the mask in the context of its role as part of the total imaging system that includes everything past “DRC clean” through mask manufacturing, including litho engineering and OPC. Certainly at the leading edge it is impossible to not consider the mask in terms of its influence on lithography and the calibration accuracy of the OPC model. Behind the leading edge, some IC manufacturers are even considering outsourcing the entire data front-end for improved cycle time and lower costs – to mask manufacturers, of all people.

Put in this perspective, perhaps the “no relevance” abstracts should be legitimized by acknowledging in the Symposium charter that design is inextricably linked to lithography through the mask and mask manufacturing. This would enable the solicitation of abstracts on topics that reference the integration of the design-to-litho flow, centered on the mask in its role as the transformation filter between the design and successful lithography, both as a limiter and an enabler.

It’s happening anyway. BACUS is not just about masks anymore.
Continued from cover.

Therefore, it is desirable that CDL-free “Charging Effect Correction (CEC)” is brought to the mask making industry from mask writer side.

Many authors had published articles in the study of resist charging effect. It is quite amazing to note that the charging effect and its qualitative analysis were already reported in 1981 by Miyazaki.1 In 1991, Sturans2 reported the beam position error due to charging in an exaggerated case where no conductive coating existed near the edge of a photomask, but the charging problem in the normal writing area has only recently been recognized as a serious issue.

When a sample of insulator is exposed by e-beam, the primary electrons get trapped in the deeper region to create a negatively charged layer, while a large amount of secondary electrons escape from the sample to create a positively charged layer near the top surface. This double layer model was theoretically proposed by Melchinger3 and computational proofs were given to the model by Monte Carlo simulations by Ko4, Lee5, and Kotera.6 Figure 1 shows a conceptual model of this double layer structure. Since a photomask has a grounded, conductive chrome layer beneath the resist layer during exposure, we are able to safely judge that any electrostatic influence caused by the negatively charged layer below the chrome layer is negligibly small.

A quantitative measurement of the surface potential was performed by the group of Pease.7,8 They reported that the surface potential tends to become positive with electron energy above 10keV and resist thickness below 500nm.

However, no quantitative charging data is available yet for 50keV e-beam with even thinner resist thickness in today’s most recent application. The objective of this paper is to establish a model to describe the surface charging effect on our EB mask writer EBM-6000, to predict the beam position error on any arbitrary layout based on the model we established, and to finally compensate for the pattern placement error by our grid correction system.

2. EXPERIMENT

2.1. Layout and writing conditions
Figure 2 describes the test layout we used to measure the charging effect. First, we wrote an array of box patterns by 81x81 grid with 1mm pitch. Second, we wrote a 40mm square, uniform exposure pad on top of the first box array. The uniform exposure pad had slits inside so that it would not overwrite the first box array. High exposure dose of 21uC/cm² was applied to this uniform exposure pad to get the clear
signal of charging effect. Finally, we wrote the second box array with the same pitch at the same location as the first box array. The positions of two box arrays were measured by LMS IPRO. To keep the measurement time practically short, we used 41x41 grid with 2mm pitch for measurement sites. We used the resist image measurement (ADI) in order to remove any pattern placement error induced by Cr stress. By subtracting the position of the first box from that of the second box, we were able to extract the beam position error which we then attributed to the charging effect.

We prepared four different pattern densities (25, 50, 75 and 100%) for the uniform exposure pad. See figure 3 for the structure details of different pattern densities. We also tested three different CAR resists to challenge the model and judge whether its efficiency holds for multiple resists.

2.2 Writing results

Figure 4 shows the results of measured pattern placement error from the 100% uniform exposure pad for all three resists. We were able to observe a clear signature of charging effect. Resist A and resist B look similar in shape, but they differ slightly in magnitude. Resist C looks clearly different in shape from others. The charging model we are going to establish has to have a single scheme while also expressing the different behavior in both magnitude and shape for any type of resist.

Figure 5 shows X placement error in X direction, as the average of 11 rows from row number 31 through 51. The figure includes data for all densities and all resists. For each resist, the graphs show the relative placement errors normalized by the maximum absolute deviation observed on that resist. We also wrote CDL-coated plates with resist A. Figure 6 shows the same X placement error in X direction as 11-row average for CDL-coated plate. The charging signature observed in figure 5 was totally removed by CDL. This result had proven that the source of the placement error we observed was truly the charging effect.

Figure 7 gives the summary of 3 sigma numbers of X placement error in X direction as 11-row average, shown in figure 5 and 6. Again, the numbers were normalized by the maximum 3 sigma observed for each resist, i.e., by the 3 sigma of the 100% pad density. As seen in the plot, the magnitude of the placement error is not proportional to the magnitude of the pad density. This means that the charging model we are going to establish must have some formula to express this non-proportional behavior between exposure intensity and the charging density.

3. Modeling

Our model has 3 major components to describe the pattern placement error induced by the charging effect.

- Response function of beam position to the point charging source
- Fogging charging model
- Conversion function from direct/fogging exposure intensity to the charging density

3.1 Response function of beam position to point charging source

First, we need to estimate how much the beam position is deflected by a point charging source of given strength. This deflection error is a function of the distance between the incident point of beam exposure and the point of charging source.

One can denote this response function as \( p(x-x', y-y') \), where \( (x, y) \) is the incident point of beam exposure and \( (x', y') \) is the point of charging source. The final map of the beam position error can be denoted as,

\[
p(x, y) = \int \int p(x-x', y-y')C(x, y) \, dx \, dy
\]

where \( p \) is the map of beam position error and \( C \) is the distribution of charging density.

Figure 8 describes the simple approximation model we set up to calculate the response function. We assumed two parallel and infinite planes both grounded to 0V. The upper plane represents the surface of the writing chamber wall and the block of objective lens and deflector. The lower plane represents the chrome layer of a photomask. Two planes were separated by the distance of ‘L’. Both planes were considered as perfectly conductive. The point charging source was located on the resist surface whose thickness was ‘\( h \)’. Since the conductive chrome layer can be considered as a mirror in the static potential calculation, a mirror charge was located below the chrome layer with the same distance of ‘\( -h \)’. The real charge and the mirror charge work in pair as a dipole. Since the upper conductive plane can be also considered as a mirror, a set of infinite number of dipoles were arrayed with a pitch of ‘2L’.

In the actual calculation, the numbers of dipoles were truncated at a certain practical limit. The orbit of 50keV electron was numerically calculated by solving the kinetic equation, and the final deviation of the electron position when it arrived at the resist top surface was taken as the beam position error for a given incident position.

In the real configuration of a mask writer, the stage and objective block structures form additional boundary conditions to the actual static potential. However, we confirmed by FEM simulation that the impact of those minute and subtle components on the computed...
static potential was less than 5%. In this paper, we adopted simple approximation model because it enables us to use a single response function commonly at any incident/source positions, anywhere on the mask. The response function we derived from our simple approximation model is shown in figure 9.

3.2 Fogging charging model

Next, we tried to simulate the beam position error with the response function we calculated in section 3.1. We assumed simple step-function-like charging profile where only the exposed area was charged positively; namely our first charging model. In figure 10, the result of our first charging model was compared to the experimental results presented in figure 5. The shape of the calculated beam position and the actual measured positions look quite different from each other. The most pronounced discrepancy between the model and the experimental data is observed in the unexposed area, outside the uniform exposure pad.

To explain the position error observed in the unexposed area, Alles9 introduced a model of diffusion and recombination of electrons and carriers from semiconductor theory, and successfully explained the signature of the beam position error obtained experimentally. However, the material we are considering in this paper is an insulator composed of polymer resist and quartz glass. Even if it were possible for electrons to diffuse in such a wide area, they could be easily drawn by the conductive chrome layer which resides only a couple of hundreds nanometer below. Instead, we propose the concept of the fogging charging model. Fogging electrons can travel a long distance inside the vacuum chamber and they can create negatively charged area widely spread over the unexposed area. See figure 11 for the conceptual model of the combination of positively charged exposed area, and the negatively charged unexposed area.

For the distribution of the fogging electrons, we assumed a simple Gaussian model with a radius of $\sigma$,

$$F(x, y) = \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} g(x-x', y-y') D(x', y') dx' dy'$$

where

$$g(x, y) = \frac{1}{\sigma \sqrt{\pi}} e^{-\frac{x^2 + y^2}{\sigma^2}}$$

Figure 5. Placement error due to charging effect in X direction: average of 11 center rows.
Continued from page 5.

where $F$ is the fogging exposure intensity and $D$ is the direct exposure intensity.

3.3 Conversion function from exposure intensity to charging density

In section 2.2, we concluded that our charging model must account for two key experimental observations:

1. The profile change of position error as a function of pad density
2. The non-proportional behavior of the magnitude of position error as a function of pad density

To account for the first observation, one must consider different charging mechanisms for the exposed and unexposed area separately. The profile shape of the position error is defined by and responds to the balance between the charging in the exposed area and charging in the unexposed area. To implement this concept, we introduced a commonly known phenomenon called Electron Beam Induced Conductivity (EBIC)\(^{11}\) to our model. In the unexposed area, the fogging charging continues to accumulate, but once the area is exposed, a strong EBIC occurs, allowing the accumulated charging from prior exposure to travel to the conductive chrome layer beneath the resist and finally to ground. Once the exposure stops, a certain amount of charging is retained from the direct exposure, and as the exposure sequence continues, the charging by the fogging electrons from the vicinity area again starts to accumulate.

To account for the second observation, we prepared polynomial expressions to convert the direct and fogging exposure intensity to the charging density:

\[
C = C_0(D) + C_1(F) = (d_0 + d_1D) + (e_0F + e_1F^2 + e_2F^3) + f_1F^4 + f_2F^5 + f_3F^6
\]

For the unexposed area:

\[
C = C_0(F) = f_1F + f_2F^2 + f_3F^3
\]

Linking all equations from (1) through (4) outputs the final map of beam position error $\rho$ from the input direct exposure intensity $D$. Figure 12 summarizes the flowchart of our finalized charging model.

4. Fitting results

We obtained total 9 parameters ($\sigma$, $d_0$, $d_1$, $e_0$, $e_1$, $e_2$, $f_1$, $f_2$, and $f_3$) by the least square method to fit the experimental data. The fitting was done for each type of resist individually. The fogging radius $\sigma$ we obtained from the fitting was quite similar to the radius we usually obtain from CD measurement of fogging effect; hence it reinforced our fogging charging theory. In figure 13, we showed the comparison of experimental data and our modeling results and also their correlation plots for all three resists with 100% pad density. In figure 14, we updated the charts for all 12 conditions presented in figure 5 with our modeling results included. Figure 15 shows the summary of relative placement error 3 sigma with the bars of predicted residuals added.

The predicted residual was given by simply subtracting modeling results from the experimental data. In all cases, we obtained good agreements between the experimental data and our modeling results.

For resist A with 100% pad density, the expected reduction of the placement error reached above 80%, which was close to the upper limit of the reduction goal (~90%) suggested by the CDL result.

5. Conclusion

We established a good model to describe the charging effect on our EBM-6000 system. By applying our model to our grid correction
Figure 8. Calculation model of position response function.

Figure 9. Position response function to [nC] charge.

Figure 10. Comparison of placement error profile between experimental data and first charging model.
Continued from page 6.

system, we expect 40~80% reduction of the placement error due to charging effect to help meeting the requirements of photomask production in the hp 32nm node.

6. Acknowledgments
The authors would like to thank Professor Masatoshi Kotera at Osaka Institute of Technology and Dr. Victor Katsap at NuFlare USA for their valuable suggestions in understanding the resist charging mechanism.

7. References
Figure 13. Comparison and correlation plot of placement errors between experimental data and modeling results: pad density 100%.
Figure 14. Comparison of placement errors between experimental data and modeling results for all resists and densities.

Figure 15. Summary of relative placement error 3 sigma with predicted CEC residual.
Industry Briefs

Chrome: “Exiting stage left?”

Chrome, which has served the photomask industry well for decades, may gradually be displaced by a better metal: molybdenum silicide (MoSi). Franklin Kalk, CTO at Toppan Photomasks Inc. (Round Rock, Texas), said he knows of two semiconductor companies that plan to use MoSi for 32 nm logic production starting next year. At leading-edge design rules, MoSi “just works better than chrome, which is a pretty good reason to use it,” Kalk said. The composition of the MoSi alloy produces a sharper sidewall with less line edge roughness (LER).

Although MoSi has been used in phase-shift masks (PSMs), binary masks, thus far, have stuck with chrome.

However, the immersion lithography optics with numerical aperture (NA) >1 do not work as well with PSMs as with binary masks. “Polarization effects used in immersion lithography favor the conducting materials of binary masks, partly because phase-shift masks tend to have low-conductivity absorbers, which don’t lend themselves well to polarization effects,” Kalk said. More importantly, MoSi is easier to etch than chrome. For decades, wet etching was used with chrome, but as modern dry etchers came into use, the mask shops found chrome to be difficult to etch. “Moly-Si has a much stronger ionic component than chrome, so the etch step is less of a chemical process,” Kalk said. “Overall, moly-Si is a much easier material to deal with, with better defect qualities than chrome and better sidewall angles.”

The lower rate of defects means less time repairing masks, reducing the turnaround time needed to make a defect-free mask. Also, he said cleaning a mask with MoSi is no harder than with chrome. Brian J. Grenon, president of Grenon Consulting Inc. (Colchester, Vt.), said he has been advocating MoSi as a replacement for chrome absorbors for many years, and gave an entire seminar on the problems with chrome at Sematech in 2003. MoSi’s attributes include better CD control, improved image placement, more accurate metrology, easier inspection and higher resolution. MoSi “is basically a purer material that is easier to process,” Grenon said. “The basic reason is compositional, which has to do with the basic properties of the metal, allowing more robust process conditions. Dry etching is more precise because the film chemistry is less amorphous.”

Advanced Micro Devices Inc. (AMD, Sunnyvale, Calif.), is likely to be among the first companies to use MoSi, Grenon said, noting that AMD and Toppan, along with Infineon Technologies, are members of the Advanced Mask Technology Center in Dresden, Germany.

Kalk noted that Toppan and IBM have an agreement to work together on 32 and 22 nm mask technology, but declined to say which companies will be first to switch to MoSi.

He said two companies will begin prototyping late this year and move to volume use of MoSi masks in 2009 for 32 nm logic production.

The memory makers, which measure their design rules by the lithographic half-pitch, will consider MoSi masks for the 45 nm node. Toppan, which is wholly owned by Toppan Printing Co. (Tokyo), developed its MoSi process with Shin-Etsu Chemical Co. (Tokyo). In June, Toppan Printing announced that it was ready to begin volume production of 32 nm masks. After several years of collaborative work with Shin-Etsu, the MoSi process is ready for use, Kalk said. “No one is in production today, but we will next year for sure. We are working with a couple of captive mask shops as well, so not all the companies that use it will be customers of our commercial mask shops.” Asked if chrome will eventually become obsolete, Kalk took pause and then said, “I think yes, it will be. Frankly, there are a bunch of reasons why. Fundamentally, the material is being processed in ways it was never intended. Chrom is difficult to etch in a modern dry etch reactor. It is being used in ways where alternative materials can provide clear advantages, so it makes sense that we would replace it. Chrome has momentum. It has worked really well for 25-30 years. One way or another, it probably is on its last legs.”

World’s First 3-D Chip Process

By EE Times

The world’s first 3-D chip process is ready for licensing from the fabless semiconductor design house BeSang Inc. BeSang fabricated demonstration chips with 128 million vertical transistors for memory bit cells above their control logic. The chips were designed at the National Nanofab Center (Daejeon, South Korea) and Stanford Nanofab (Palo Alto, Calif.). BeSang said its process, which is protected by over 25 patent applications, will allow flash, DRAM and SRAM to be placed atop logic, microprocessor cores and SoCs.

BeSang claims it achieved 3-D by fabricating logic circuitry using a high-temperature process on the bottom and by fabricating memory circuitry using a low-temperature process on top of the logic. By placing logic and memory on different layers of the same 3-D chip, BeSang’s process packs in more die per wafer, which translates into lower costs per die.

“BeSang was founded five years ago to work on 3-D IC technology,” said Sang-Yun Lee, BeSang’s founder and CEO. BeSang “has introduced a single-chip 3-D IC process that is ready for commercialization. By using a low-temperature process and orienting vertical memory devices on top of logic devices, we make more dies per wafer, and that is how the cost per die goes down.”
Join the premier professional organization for mask makers and mask users!

About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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- Quarterly technical meetings in the Bay Area
- Reduced registration rates at BACUS Photomask Technology annual meeting
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