Using in-chip overlay metrology

Stefanie Girol-Gunia and Bernd Schulz, AMD Fab36 LLC & Co. KG, Wilschdorfer Landstraße 101, 01109 Dresden, Germany
Nigel Smith and Lewis Binns, Nanometrics Incorporated, York, UK

ABSTRACT

Overlay process control up to and including the 45nm node has been implemented using a small number of large measurement targets placed in the scribe lines surrounding each field. There is increasing concern that this scheme does not provide sufficiently accurate information about the variation of overlay within the product area of the device.

These concerns have led to the development of new, smaller targets designed for inclusion within the device area of real products.1,2 The targets can be as small as 1-3μm on a side, which is small enough to permit their inclusion inside the device pattern of many products. They are measured using a standard optical overlay tool, and then calibrated. However, there is a tradeoff between total measurement uncertainty (TMU) and target size reduction.1 Also the calibration scheme applied impacts TMU.

We report results from measurements of 3μm targets on 45nm production wafers at both develop and etch stages. An advantage of these small targets is that at the etch stage they can readily be measured using a SEM, which provides a method for verifying the accuracy of the measurements.

We show how the 3μm in-chip targets can be used to obtain detailed information for in-device overlay variability and to maintain overlay control in successive process generations.

1. Introduction

Each new process generation is less tolerant to layer-to-layer pattern overlay error. At the 45 nm node the maximum allowable overlay error for the most critical layers is expected to be 9 nm.1 Deployment of double patterning techniques in the future will drive it down to around 2 nm at or even before the 22 nm node.

Measurement of overlay error during manufacture is required to maintain good overlay control. Normal manufacturing practice requires the maximum uncertainty in the measurement to be at most 10% of the process tolerance. Hence the total measurement uncertainty (TMU) for critical layers must be 0.9nm or less for the 45nm node, and this will be reduced in the future to 0.2nm or less.

It is current practice to measure overlay using comparatively large (25x25μm) bar-in-bar (BIB) patterns printed within the scribe lines. Both the size and location of these targets give cause for concern, Continues on page 3.

Figure 1. Description of the box-in-frame (BIF) in-chip target layout used in this study.
Intel Mask Operation

Frank E. Abboud, Intel Corp.

In last February’s SPIE Advanced Lithography Symposium there was a definite surge in the number of technical papers and panel discussions focused on EUV and Imprint. Even the hallway chats, where the real technical exchanges take place, could not moderate such enthusiasm. I could not help but think about Double Patterning! I had just attended a day-long session on that topic at the last SPIE Photomask Technology Symposium; and if my memory serves me right, the topic was on the Friday Advance Mask Session. What did I miss? Have all the technical problems with Double Patterning and mask registration been solved? Maybe … but maybe not. This is what’s wonderful about our industry, once the problem is solved, in theory, then onto the next big thing. Well, there is a lot of engineering challenges to produce a repeatable, practical and sustainable manufacturing solution that is also cost effective. For the most part, Mask registration has been somewhat out of the limelight. Critical dimensional pattern fidelity and inspection have been consistently on the top of the priority list. Yes there was some push for better overlay and tool to tool matching for PSM applications, but really registration has been taken for granted especially with the introduction of Multipoint Alignment techniques in the last decade to average out outliers. I think the way we look at pattern placement accuracy is about to change and we better stay ahead of the curve. It really did not take much for me to realize the severity of the problem, once I sat down and started thinking about how the DP mask will be used. In prior lithography techniques the relative placement of features within a layer were contained to that layer only and as long as the pattern placement and overlay errors were small enough to maintained alignment in the Z plane over the reticle set, layer to layer connectivity was achieved. One can claim that “trim masks” are a form of double patterning, but I contest that the fundamental task was the Z plane alignment. In double patterning we move the problem on the wafer to the XY plane. Although, a good lithographer friend of mine promises that double patterning will not be used to define edges of the same feature, the need to maintain equidistant features made by two different masks in both X, Y and yet ensure that the Z plane alignment for all layers brings the topic of pattern placement accuracy is about to change and we better stay ahead of the curve. It really did not take much for me to realize the severity of the problem, once I sat down and started thinking about how the DP mask will be used. In prior lithography techniques the relative placement of features within a layer were contained to that layer only and as long as the pattern placement and overlay errors were small enough to maintained alignment in the Z plane over the reticle set, layer to layer connectivity was achieved. One can claim that “trim masks” are a form of double patterning, but I contest that the fundamental task was the Z plane alignment. In double patterning we move the problem on the wafer to the XY plane. Although, a good lithographer friend of mine promises that double patterning will not be used to define edges of the same feature, the need to maintain equidistant features made by two different masks in both X, Y and yet ensure that the Z plane alignment for all layers brings the topic of pattern placement accuracy fundamentals to the forefront of our mask efforts.

Significant advancements in writers and metrology tools in recent years were focused on two key fundamental error budget sources: local errors (<1 micron), and global errors (up to 150 mm). Each has its own challenges and idiosyncrasies. The local errors tend to be driven by the system architecture and how well the tool can coordinate the positioning of the stage, the beam and data path (image deposition in the writer case, or image capture in the metrology case). I will simply rely on the tool makers to do the best job possible to virtually eliminate such error or at least contain it to less than half a nanometer. The global errors tend to be driven by the effectiveness of the error correction modeling and compensation as it applies to long term stability, repeatability and traceability. Although at every compensation/correction step the error is small, the stack-up tolerances of the residual errors at the various stages of mask can throw the error budget into a non-converging loop. Hard to imagine that a 6.35 mm thick Quartz mask actually sags, depending on the method used by the tool maker to hold the mask. Compensation algorithms are well known (Bessel point) for sag compensation, however, meticulous attention to how the mask is held can avoid a good portion of the compensation (e.g., 3 point contact without clamping). Equally hard to imagine is the impact of pellicle mounting. All the hard work of ensuring flawless pattern placement can be completely undermined by the seemingly simple end-of-line operation of affixing the pellicle. How to compensate? Such error tends to be random and difficult to predict and model. All the money invested in the ultra flat blank is negated as the pellicle mount process un-doubtfully impacts the flatness of the finished substrate.

A great deal of collaboration will be needed to fully understand and contain the error sources that contribute to the global pattern placement errors. Collaboration, standardization and a better overall understanding of the mask handling through out the mask lifecycle of fabrication and usage process will go a long way in avoiding a never ending loop of error compensation that may be driven by residuals.

Although EUV and Imprint are appealing and exciting, especially in this early development stage, we need to channel some of our mask making efforts and enthusiasm toward solving the more immediate double patterning problem to achieve repeatable, reliable and cost effective manufacturing solution.
since both are too far from the ideal of measurement directly from the circuit pattern itself. The targets are traditionally measured by processing images from an advanced optical microscope.

Measurements made in the scribe lines are used to predict overlay variation within the active area of the device by fitting to a model of the stepper or scanner behavior. The best fit agreement between the data and the best-fit model is seldom better than 5nm, which consumes the entire anticipated process control target. Making measurements in inner scribe lines can help, but true knowledge of the in-device overlay control achieved requires measurement within the active areas as well.

BiB targets are large enough that the elements are effectively isolated when the image is formed. The typical lateral resolution of an overlay metrology tool is 800nm, and isolation is achieved by separating the bars by at least 2μm. If the various parts of the measurement target are brought too close together then they will interact during formation of the image in the measurement tool. These interactions will introduce an error into measurement using traditional algorithms because the assumption of image symmetry is not met. The effect can be reduced to some extent by enhancing the resolution of the imaging system, for example by increasing the numerical aperture (NA) of the imaging system. But such an increase would also increase the system aberration and hence the magnitude of tool induced shift (TIS), generally by more than the reduction in wafer induced shift (WIS) achieved. Because of the isolation requirements for accurate measurement using traditional techniques, the smallest targets that can be used are approximately 8x8μm in size [1], which requires a total region of 12x12μm to achieve 2μm separation from surrounding patterns. This is too large for inclusion in most devices.

Direct measurement within the device area is best performed by measuring from the device structures directly, but no method has yet been identified for doing this. Instead, interest has turned to “micro-targets” which are small enough to be included inside the device region. These targets are so small (3x3μm or less) that image symmetry changes rapidly with overlay offset. Overlay is linearly proportional to the image asymmetry.

No matter how small the target is, it will not be small enough for all possible applications (DRAM, for example), but a small target is more flexible than a larger one. We expect TMU for these targets to become worse as their size is reduced, but this can be addressed by using more targets as an alternative to making them larger. Using one or more small targets allows simple application to irregular spaces, which increases the number of cases where they can be used.

A part of the present work is concerned with the TMU that can be achieved using micro-targets. The rate of change of image asymmetry with overlay is also modified by process effects, and this must be taken into account in determining how to use micro-targets in practice. We show which measurement schemes will produce the best TMU, and by comparing that prediction with measurement uncertainty requirements we can determine how best to use these targets in advanced production applications.

2. EXPERIMENTAL

2.1 Target design
All targets used in this study have a common layout, referred to as “box-in-frame” (BIF) structure. The layout and characteristic dimensions of the BIF target layout can be found in figure 1. The outer dimensions of a single BIF target amount to 3μm by 3μm. The targets are placed in the chip layout with an additional clearance of 2 μm with respect to neighboring structures. One layer, usually the reference layer, is printed as a frame, made up of four single bars, and the second layer, usually the resist layer, is printed as a square contained within the bars. The open corners of the frame avoid rounding when it is printed.

The calibration of the target response towards OVL error is done by using a combination of targets with different programmed offsets, DX and DY (DX = DY), within each measurement location (“site”). Hence, each site contains a target array. The layout of the target array used in this study is described in section 2.2 and an explanation of the calibration method is given in section 2.5.

2.2 Target array in 45nm product wafers
The first set of experiments was carried out using 45nm poly gate and contact product wafers including the test array shown in figure

Figure 2. (a) Optical image of the full test target array from an etched 45nm poly gate product wafer, containing targets with programmed offsets of 30, 50 and 70nm in the top, middle and lower group, respectively. The BIF targets used in this study for etched poly gate are marked with a frame. (b) CDSEM images obtained from the same layer, showing one block of the test array and (c) a single BIF target. (d) Distribution of the test arrays in the field area. Each cross represents one array.
2a. For each site, this test array contains three groups of targets, each group having a different programmed offset: 30nm in the top, 50nm in the middle and 70nm in the bottom group. The BIF targets which were subject of this work are placed with a distance of 15 μm to each other, as marked in figure 2a (see dashed frame). The total number of sites per field amounts to 77. The distribution across the wafer field is shown in figure 2d.

Measurements were taken for the contact layer at the mask step as well as for the poly gate wafer after the etch step. The use of an etched layer was necessary to allow CDSEM correlation measurements, where otherwise the reference layer would be invisible due to resist coverage. The resist or etched layer is represented by the inner part of the BIF targets, i.e., by the box, while the underlying reference layer is represented by the surrounding frame.

Figure 2a shows an image of the etched poly gate layer from the optical microscope of the OVL tool, whereas figure 2b shows CDSEM images of the same layer. This illustrates the resolution limitation of the OVL tool, which in turn enables the asymmetry measurement methodology.

The CDSEM image of a single BIF target is displayed in figure 2c. It demonstrates that printing quality and the related quality after the subsequent etch step are very good. Further details, describing the printing quality of the targets as derived from CDSEM measurements, are given in section 2.6.

2.3 OVL measurements
All OVL measurements were carried out on Nanometrics Caliper élan tools, using a special in-chip measurement algorithm, which analyses target asymmetry as described in section 2.4.

At each in-chip site to be measured, individual measurements are taken from the targets of interest, i.e. the BIF targets with programmed offsets of 30, 50 and 70nm, respectively, at wafer rotation angles of 0° and 180°. Then, for each site and each angle, the three individual measurement values are converted into a single OVL error by applying the calibration method described in section 2.5.

The final step consists of calculation and removal of the TIS, a tool-specific error, at each site from the OVL data obtained at 0° and 180°. This corresponds to the practice which is used for OVL measurements of the well established scribe line targets.

For both OVL measurements at the mask and after etch, the repeatability was obtained from 5 dynamic measurement loops of one field with 77 sites as the pooled 3σ precision across all sites.

The OVL data for correlation to CDSEM was acquired on the etched poly gate wafer on four fields with 77 sites per field. The sampling plan is shown in figure 3a. For the same fields, additional measurements of the bar-in-bar (BIB) scribe line targets were obtained, which are located in the corners and in the center of the field. A linear scanner model was applied to the BIF and BIB data to yield the uncorrectable residuals.

Similarly, the contact wafer at the mask step was measured on 11 fields with 77 BIF sites and 5 BIB sites per field. The sampling plan is shown in figure 3b. The same linear scanner model was applied to this data to obtain residuals.

2.4 The in chip measurement algorithm
Previous papers have shown that for small in-chip targets like, e.g., the 3μm BIF, which cannot be fully resolved in an optical microscope anymore, the displacement of the square and the frame with respect to each other introduces asymmetry into the intensity of the image of the target along the axis of the displacement (“image asymmetry”). Further, it was found, that there is a linear relationship between image asymmetry and overlay error, so that the image asymmetry can be used as a measure of overlay error.

The asymmetry of the image, F, is the smallest value of the root-mean-square difference of intensities at equal distances about any point s, f(s), within the image:

\[
f(s) = \left( \frac{\int (I(s+x) - I(s-x))^2 \, dx}{x_2 - x_1} \right)
\]

As conversion of the asymmetry values into OVL errors requires knowledge of the linear relation, a number of targets with different programmed offsets must be in place to establish a calibration.

2.5 Measurement calibration
As described in previous papers, applying equation 1 to images modeled for changes in overlay offset, yields a linear response if no noise is in the signal. Noise causes the response to trail off for small overlay offsets because random differences about the center of symmetry will increase the calculated value for F. The simple solution to stay in the linear regime of the response curve is to program an offset into the design of the targets. Model results show that a range of 30-70nm is a suitable choice for the offsets, given that in 45nm processes the most critical layers will not be printed with overlay errors larger than 20nm.

The rate at which image asymmetry changes with overlay is referred to as the sensitivity of the measurement target. Sensitivity is influenced by the target layout itself as well as by process parameters such as film thickness and composition. Layout-wise, the gap value G2 (see figure 1) controls sensitivity. This value was fixed for the BIF targets which were subject of this study. Regarding process influences on the 45nm product wafers used, in some cases it can be observed, that the target sensitivity within a field is effectively constant but that from field to field small but significant changes can occur. This needs to be taken into account when the calibration scheme is determined.
In this work, where the device layout permitted three corresponding calibration targets to be printed at every measurement location, it is possible to calibrate each site separately. However, provided that a number of sites exhibit the same sensitivity, it is beneficial to use a calibration factor averaged across these sites, as the larger number of data points reduces the uncertainty in the calibration factor. We will show in the results section that for the wafers used in this study, it was justified to apply a calibration by field.

In applications with less available space there is the option to print sites with single targets and combine them with only a few calibration arrays, which could be placed in the scribe lines if necessary.

2.6 CDSEM measurements

Reference measurements on the BIF targets were carried out using an AMAT Verity2 CDSEM. This tool is referred to as “CDSEM 1”. To validate this reference method, a second CDSEM tool of another type, namely a Hitachi CG4000 CDSEM, was used for comparison. This tool is assigned “CDSEM 2”.

To obtain OVL data by using a CDSEM, for each target the gaps G21, G22, G23 and G24 (see figure 2.1) were measured, so that the OVL errors in X direction, OVL$_X$, and Y direction, OVL$_Y$, could be obtained as

\[
OVL_X = [0.5*(G24-G23)-DX] \quad \text{and} \quad OVL_Y = [0.5*(G21-G22)-DY].
\]

For each site, the OVL errors of the individual targets were then averaged to yield a pooled OVL value per site. These site values were used for the correlation of OVL and CDSEM data as well as for the correlation of CDSEM 1 to CDSEM 2.

To calculate the target precision (repeatability) of the CDSEM measurement, 1 field with 77 sites per field was measured in 5 dynamic loops and the precision was calculated as pooled 3$\sigma_{CDSEM}^2$ of all single gap measurements. The precision of the OVL data derived from the CDSEM gap measurement is then given by sqrt(0.5)* 3$\sigma_{CDSEM}$.
Both, the CDSEM measurement uncertainty as well as the printing accuracy add uncertainty to the OVL to CDSEM correlation. To investigate the printing quality of the outer frame, the precision for the measured gap values $G_2$ was obtained. For the X direction, $G_2 = 0.5(G_{23} + G_{24})$, and for the Y direction, $G_2 = 0.5(G_{21} + G_{22})$. Following the target design, $G_2$ should have a constant value. This yields information about the overall printing accuracy of the targets.

### 3. RESULTS

#### 3.1 Evaluation of the calibration method

Before OVL results can be obtained from in-chip measurements, the calibration method needs to be determined. Generally, several methods are possible, such as site-by-site, field-average or all-fields calibration. However, since it was found, that target sensitivity may vary from field to field, the latter was not considered for the data presented in this work. One metric we used for comparing the site-by-site and the field-average method was the quality of the correlation to CDSEM.

Figure 4 shows the influence of the calibration method on the distribution of OVL to CDSEM data per site for one field. The results of the site-by-site calibration (a) are compared to that of the field-average calibration. It can be seen, that the field-average method leads to a better correlation to CDSEM with offsets mainly in the range of -3nm to 3nm. In contrast, the range of the distribution after site-by-site calibration is approximately twice as large (see section 3.3 for details).

The other metric taken into account to find a suitable calibration method was the consistency of the TIS data. Table 1 shows the average TIS and TIS $3\sigma$ values obtained from 5 fields with 77 sites per field of the same etched poly gate wafer after site-by-site calibration as well as after average-field calibration. While the average TIS values are small and at the same level, the TIS range is significantly larger for the site-by-site method.

Both, the CDSEM correlation data and the TIS data, clearly indicate that the field-average calibration represents the best calibration method for this study. It involves averaging of the calibration slopes from all sites in the same field and applying the derived calibration factor to each site.

#### 3.2 Measurement precision

The repeatability of the optical OVL measurements on in-chip targets was determined for both the etched poly gate and the contact mask wafer, respectively. For the etched layer, the center field was measured on the overlay tool and on CDSEM 1 to obtain precision and in the case of the optical measurement also TIS repeatability. Optical data was cull to remove flyers (1.5% of sites) and sites, where not all three targets per group had been measured (8.6% of sites), so that the data is based on 69 sites. The gate wafer showed a $3\sigma$ repeatability of 1.7nm in X and 2.1nm in Y, while the contact wafer reached better results for the single field measurement with 1.1nm in X and 1.2nm in Y. In contrast, the TIS behaviour was found to be better on the gate wafer, as TIS average was lower and TIS $3\sigma$ yielded values of 0.8nm in X and 1.3nm in Y, compared to approximately 2nm for X and Y on the contact wafer.
Furthermore, the precision data was evaluated for all 11 fields of the mask layer, and some variation was found. 3σ precision of the individual fields varied between 0.7 and 2.4nm in X and between 0.9 and 3.0nm in Y. TIS 3σ values varied between 0.9 and 4.6nm in X, and between 1.2 and 5.2nm in Y. Hence, the overall performance of the contact wafer is worse than for the center field only as can be seen in table 2. This is mainly caused by a number of fields at the outer right part of the wafer (compare figure 9a), which are characterised by comparatively large overlay errors.

Also the 3σ repeatability of the CDSEM-based overlay data from the etched wafer was calculated for CDSEM 1. The precision was 0.6nm for both X and Y and clearly exceeds that of the optical in-chip measurement. Table 2 summarizes the results.

3.3 Correlation of in-chip OVL data to CDSEM data
The correlation plot of OVL data versus CDSEM 1 data for four fields of the etched poly gate wafer is displayed in figure 5. The OVL errors measured are in the range of approximately -10 to +15nm. A linear behavior is found for both X and Y data, and the slopes of the linear fits amount to 1.05 for overlay error in X and 1.09 for the error in Y. The correlation between optic and CDSEM measurements is in the range of approximately -3 to 3nm and exhibits a distribution which is similar to that shown in figure 4b, where only the center field was shown. No significant field-to-field variation was observed regarding correlation. Another way of expressing the agreement between the two data sets is as three times the standard deviation (3σ) of the differences, i.e., the scatter of the data around the line X=Y. The 3σ was 2.9nm in the X axis and 3.3nm in the Y axis.

Regarding the optical to CDSEM offset, there is a systematic shift of the curves to positive values for X and to negative values for Y. This behavior can be attributed to the CDSEM measurement. We have found that the way the edges are defined in the CDSEM algorithm directly impacts the magnitude of the systematic offsets. This phenomenon has also been reported in the literature for similar investigations of optical versus CDSEM measurements. It can also be seen that the correlation found between the CDSEM tools is significantly tighter than that observed between CDSEM 1 and optical data. This indicates that the agreement between CDSEM 1 and optical data is limited by the accuracy of the optical measurement.

Again, an offset can be seen between both measurements. As before, we attribute this behavior to the measurement algorithms of the individual CDSEM tools, which were not being matched to each other prior to measurement.

We investigated the printing quality by looking at the gap variations seen in the CDSEM measurement. We found a 3σ precision in the order of 5nm for the size of the gap across all fields sampled on the CDSEM tool. Simulation showed that this introduces a variation of up to 1% to the optical OVL measurement.

3.4 Model analysis
Gate wafer
A vector plot for the center field of the etched poly gate wafer is displayed in figure 7, comparing OVL errors obtained by optical in-chip measurement and CDSEM measurement. In general, similar patterns for CDSEM and optical data can be found (note, that there is a systematic offset which was revealed by the correlation plot shown in figure 5).

Figure 7 also contains the OVL error vectors measured on BIB targets in the four corners and in the inner scribe line of the field. There is a broad agreement between the overall behavior of the BIB results and the needs to be recognized, that there are no BIB and in-chip targets located in close proximity to each other. The distance between the two types of targets is in the range of 1-3μm, so that no direct correlation can be obtained.

To get an understanding of the agreement between overlay error as derived from BIB targets in the four corners of the scribe line and overlay error measured in the in-chip regime, a standard linear scanner model was applied to the BIB results and used to estimate the overlay at the in-chip measurement locations. A qualitative comparison between the raw in-chip data and the BIB-derived model prediction, based on the 4 fields which had been validated using the CDSEM, and one additional field, is displayed in figure 8a and b.

It is apparent that the in-chip overlay error variation, which is predicted by the scribe line measurement, does not correspond to the overlay error variation which was measured at the related locations.

Continues on page 8.
The in-chip overlay measurement reveals that the overlay error is consistent for certain areas within the field, but that there are variations between these areas. Thus, neither orientation nor magnitude of the measured overlay errors can be reproduced consistently by the linear BIB-derived model. The magnitude of the predicted errors is up to 10nm smaller than that measured.

Contact wafer
Measurements were carried out on the contact wafer at the mask step, using both BIB and in-chip methodologies. The wafer was misprocessed and exhibited a comparatively large range of OVL errors, which turned it into an interesting test vehicle for our investigations. The sampling plan for in-chip measurement, as shown in figure 3a, included 11 fields, and in each field 4 BIB measurements were made at the field corners, along with 77 in-chip measurements scattered throughout the active area. Measurements were carried out with 5 repetitions per site, and full TIS compensation, so that the TMU components are suppressed. Measurements of BIB targets were carried out on all fields.

A qualitative comparison between both data sets can be seen in figure 9a. It shows that there is an overall agreement between BIB and in-chip data, especially in close proximity to the BIB targets. However, in some fields the in-chip overlay errors are generally much larger than the corresponding BIB scribe line vectors. This applies mainly to the fields on the right outer edge of the wafer. For these fields it was also found that repeatability was worse than that, e.g., the center field. The root cause of this inconsistency is not yet understood.

A standard linear scanner model was applied to the full field BIB results to predict the overlay error at the in-chip measurement locations. The predicted model is shown in figure 9b. This model was subtracted from the raw in-chip data, yielding the residual overlay errors shown in figure 9c.

A qualitative comparison of the results reveals that there are significant differences between the BIB-derived predicted in-chip model and the measured in-chip overlay error in orientation as well as in magnitude of the vectors. After subtraction of that model, large residual overlay errors in the in-chip regime remain, ranging between 10 and 15nm for the fields in the wafer center, as depicted in figure 9d, and exceeding 20nm on some of the other fields (excluding the fields at the right wafer edge). Accordingly, the residual $3\sigma$ values for the in-chip regime, which remain after applying the BIB-derived linear model, are significantly higher than those found for the BIB scribe line data, as shown in table 3.
Both the raw in-chip data, and the residual data obtained by subtraction of the linear model prediction, show some systematic in-chip pattern variation, which cannot be modelled by the BIB-derived linear model. However, it is less pronounced on this wafer compared to the etched poly gate wafer.

4. DISCUSSION

In this study optical in-chip measurements were carried out on an etched poly gate wafer and a contact wafer at the mask step using 3μm overlay targets, and it was shown that this methodology is capable of measuring overlay error in the device area.

The relative accuracy of the optical measurement of the in-chip targets was validated using CDSEM measurements. The 3σ standard deviation between both data sets reached 2.9nm in X and 3.3nm in Y after applying the field-calibration method. As CDSEM to CDSEM correlation was found to be at a better level than optical to CDSEM correlation, and since the repeatability of CDSEM measurements was superior to the repeatability of the optical OVL measurement, the main source of uncertainty was attributed to the optical measurement rather than the CD measurement.

The impact of the target printing quality was checked, but was found to have only minor influence. In general, image noise is a contributor to TMU, which limits the relative accuracy that can be achieved with such small targets under the given measurement conditions.

Due to these limitations the in-chip overlay methodology described here can be regarded as a complementary method, which yields valuable information in addition to conventional overlay data. However, the sampling rate of OVL in-chip measurements is significantly higher than that used for scribe-line measurements, which again leads to an overall improvement of TMU again. The prerequisite for uniform and sufficiently high sampling across the field, which is a small target size allowing implementation into the device area, is well met by this type of OVL targets.

To get an understanding of the behavior of the in-chip OVL errors in relation to scribe-line OVL errors and the methods used to correct them, linear models from scribe line measurements of BIB targets were derived for both wafers under test. The latter represents the methodology which is commonly used for process control in the production environment to determine correction terms for scanners. However, applying the modeled data to the in-chip OVL errors showed, that the data obtained from the scribe line corners does not correlate well with the data obtained within the fields, as significantly higher residuals remained in the intrafield regime. The characteristic variations of the in-chip overlay errors across the field point to a possible dependence of overlay error on the device pattern. Indications for device pattern-dependant inchip overlay errors have also been found in previous studies.

The results clearly show the inconsistency of in-chip overlay variation with the view of a linear model and indicate that sampling within the in-chip regime as well as more advanced models are required to better describe and correct for intrafield overlay OVL errors.

Table 3. Summary of residual values for scribe line and in-chip regime, obtained by subtracting the BIB-derived linear model from the BIB data and from the in-chip data, respectively.

<table>
<thead>
<tr>
<th>Residual 3σ</th>
<th>BIB</th>
<th>In-Chip</th>
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<tbody>
<tr>
<td>X</td>
<td>11.6</td>
<td>19.5</td>
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<tr>
<td>Y</td>
<td>9.6</td>
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5. OUTLOOK

Having shown in the first step of our study, that in-chip OVL can be measured using the measurement methodology and target type described in this paper, further work is required to investigate the behavior of intra-field overlay errors. We found indications that in addition to known contributors to overlay, such as reticle errors or scanner aberrations, also dependencies of overlay error on the device pattern present at the location of the in-chip overlay target should be taken into account.

Regarding the quality of the in-chip target measurements, new generation optical OVL tools are expected to yield an improvement and at the same time allowing the target size to further decrease.

As far as space limitations in the device area are concerned, there is the option to combine single target sites as well as sites including all three calibration targets, to maintain dense sampling across the field or even increase the existing sampling density, thus maximizing the information that can be obtained about the OVL error patterns inside a field.

REFERENCES

Industry Briefs

- **Litho Guru Optimistic About Nanoimprint**

**Semiconductor International**

Ben Eynon, Director of Advanced Technology Development at Samsung and Associate Director of Lithography at Sematech, discussed Samsung’s evaluation of nanoimprint lithography at the SEMI Strategic Business Conference (Napa Valley, Calif.). "The resolution is there. It’s a matter of the defects and thoroughput," he said. Interestingly, nanoimprint actually improves on one of the metrics that extreme ultraviolet (EUV) struggles with: line edge roughness (LER) and linewidth roughness (LWR). After etching, features printed by step-and-flash imprint lithography actually produce smoother features than before the etch. Eynon showed impressive results and said that companies may choose to implement different lithography technologies depending on particular product mix. One of the challenges that EUV lithography has yet to overcome are weak links from ArF to EUV such as new photoresist, autofocus, pellicle, reflector, absorber, optics, debris mitigation, a vacuum processing environment, mask handling, mask haze, shadowing and chucking. Then, once EUV is established in high-volume manufacturing, taking it to the next level will involve the usual additions of high-numerical-aperture (NA) optics, phase-shift masks, optical proximity correction (OPC), etc. Among these, the top challenge is developing a source with adequate power - at least 100 W is necessary. One of the candidates for the high-index photoresist that Sematech is testing is hafnium oxide nanoparticles suspended in water - although the shelf life of this material is not encouraging. Mask blanks with 0.04 defects/cm² at 55 nm have recently been achieved, a big breakthrough according to Eynon. A new reticle inspection tool (M7360), priced at $10M, is allowing researchers to see even smaller defects than was possible with the previous-generation tool. In addition, a smoothing process has been developed - a deposition and etch process that can smooth, for instance, a 50 nm pit to 1 nm in dimension. "With smoothing we can get to the point where we don’t need completely defect-free masks, but can have a manageable level for manufacturing," Eynon said.

- **Haze, Still Misunderstood, Costing Industry $1B a Year**

**Electronic Media**

Arguably the single largest yield detractor in the semiconductor industry, costing the industry about $1B every year, micro-contamination is still very little understood or acknowledged, noted Brian J. Grenon of Grenon Consulting Inc. Haze, visible or printable crystalline structures that grow from the contamination, has been a significant issue for more than 10 years, and yet semiconductor manufacturers are still not on board with coming up with solutions. Haze is forming on wafers, photomasks and optical elements, micro-contaminants are being deposited by cleaning processes, from the environment, and introduced by the packaging.

Dominion Semiconductor was the first to report yield loss from ammonium sulfate haze around 1997, with the largest loss reported to date being $100M. The worst effects have been seen in Taiwan and Shanghai, China, where environmental factors figure prominently. The higher energy of the shorter-wavelength lasers and larger wafer sizes are aggravating the issue. Also, "the more you clean, the dirtier it gets," Grenon said, but it is difficult to get data on how many times masks are cleaned. Surfactants have been identified as a key ingredient to avoid in cleaning processes because of the haze. Wafer supplier MEMC Electronic Materials Inc. (St. Peters, Mo.) stopped using surfactants to clean the packages used to transport its wafers and extend the storage time for its wafers from 6 to 18 months.

Haze continues to grow over time. Time-dependent haze (TDH) is formed when the wafer is contaminated with water-soluble ions and organic molecules making it more hydrophobic. A change in humidity causes water to condense on the wafer surface followed by dissolution of the contaminants. The hydrophobic surface causes the water to form microscopic droplets, which evaporate and leave residual TDH defects. Without humidity, micro-contamination does not develop into haze. Ammonium sulfate, which caused the first reported haze, has become known as a micro-contaminant, so is largely under control. But the industry has since encountered new organic contaminants such as ammonium oxalate, created by carbon dioxide and water with ammonium in the air. At the same time, maskmakers are happy to take the reticles back for cleaning because it means more income for them. Fabs are now ordering three masks where they used to order two; After the first one develops haze, it goes back to the mask shop to get cleaned and re-pelliclized, the second mask goes into production, and the third is the backup. And some companies see haze as a happy occurrence because they’re in the business of providing contamination solutions.

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Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

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SPIE
International Headquarters
P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 888 504 8171 or +1 360 676 3290
Fax: +1 360 647 1445
customerservice@spie.org • SPIE.org

Shipping Address
1000 20th St., Bellingham, WA 98225-6705 USA

SPIE Europe
2 Alexandra Gate, Ffordd Pengam, Cardiff, CF24 2SA, UK
Tel: +44 29 20 89 4747
Fax: +44 29 20 89 4750
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