PHOTOMASK

BACUS—The international technical group of SPIE dedicated to the advancement of photomask technology.

EUV Lithography - Invited Paper

# Translating IC-centric photomask manufacturing to photonics-centric applications: Linking photomask processes to photonics waveguide performance

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## ABSTRACT

Silicon photonics is becoming a significant platform in high-bandwidth, low power device applications for HPC and cloud computing infrastructure. Its continuing push to displace incumbent copper and VCSEL technologies depends on the scaling potential of existing CMOS manufacturing processes. Central to this process is still the photomask, and its' ability to accurately render design intent. However, processes and quality metrics that have been developed for electronics-centric photomasks do not translate directly to the needs of photonics-centric photomasks. This may lead to unconventional or non-intuitive choices for data rendering (fracture), mask pattern tooling (laser vs e-beam). Standard metrology (CD Uniformity, Localized LER) may not capture the essential elements that correlate mask pattern fidelity with waveguide signal loss. There are likely limits to a "blind translation" of IC-centric metrics to photonics-centric metrics.

This paper will report on a collaborative effort to compare several photomask manufacturing approaches and their impact on photonics device performance (signal loss) for a common set of device structures. We will also explore the standard metrics applied to photomask quality and determine whether they correlate to waveguide performance, or whether different metrology approaches are required for vetting photonics-centric photomasks.

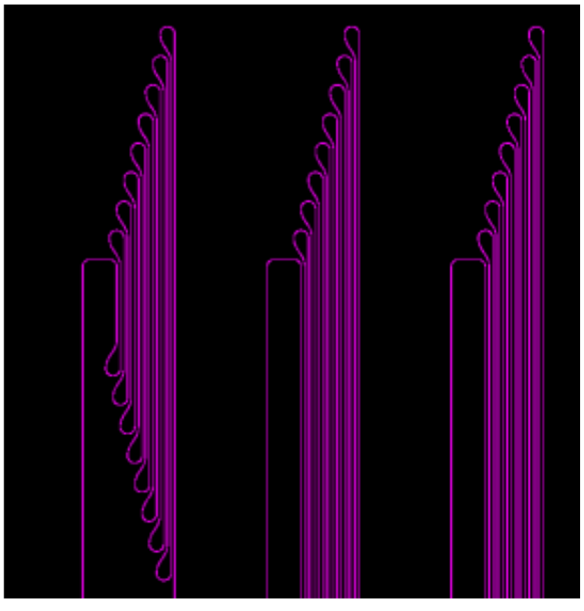

*Figure 1. "Racetrack" waveguide designs.*

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TAKE A LOOK INSIDE:



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# EDITORIAL

## Can't You Shrink It Anymore? Then, Let's Zoom!

### *Photomask Japan (PMJ) 2021 Summary*

**Naoya Hayashi,** Dai Nippon Printing Co., Ltd.

We are pleased that the concerns about the slowdown of Moore's Law have been dispelled by the practical application of EUVL.

On the other hand, COVID-19 has messed up our social life including the conferences! Although the academic society says that the conferences still keep more than half of their value without meeting in person, I haven't seen my friends for a year and a half! But we always look for countermeasures. Our chosen alternative is a virtual meeting system that makes full use of semiconductor device technology. Let's Zoom! This has greatly helped communication not only with academic and industry societies, but also with family and friends.

Due to the influence of COVID-19, last year's PMJ 2020 was canceled, and this time PMJ 2021 was held in a completely remote manner as a so-called "Digital Forum". We enabled the talks with live video presentations and Q & A, so we organized the program to be considerate of the time zone differences, running presentations from the US in the morning, those from the EU in the evening, and those from Asia in the daytime (JST).

The number of published papers, including invited ones, was 51, a decrease of 6 from the previous 2019 conference, but about half were submitted from outside Japan, and 9 were from academia, with submissions from a broad area. As for the content, there were many presentations of the latest EUV-related technologies, and the post-questionnaire also confirmed the high level of interest in those areas. On the other hand, the number of online participants was 292, a decrease of 100 from two years ago, suggesting that in-person participation is a major factor in motivation.

As an entertainment program, we delivered cherry blossom drone videos and PMJ movies presented by DNP and Toppan during breaks, as always!

Of course, the first Digital Forum left many challenges and takeaways, including:

- The first-time implementation of online functionality made infrastructure very costly.
- Since the "audience rating" can be monitored in real time, we found that "EUV High-NA" and "Inspection" sessions gathered the largest audiences.
- There is no participation from Europe other than the presenter, so I wonder if morning isn't the best time for Europeans....
- Participation in poster presentations has been sluggish, and it may be necessary to consider making them all oral.
- The resolution and stability of Zoom distribution is still an issue.
- Many people want a hybrid system for future events.
- Having a university professor as a person in charge worked well to promote participation from academia.

Photomask Japan 2022, the 28th Symposium on Photomask and NGL Mask Technology, will be held from Monday, April 25 through Wednesday, April 27, 2022, at PACIFICO Yokohama, Yokohama, Kanagawa, Japan.

- Abstract Due Date: November 30, 2021
- PMJ2022 will be held in person, but will continuously need to be carefully analyzed and discussed while confirming the possibility of international travel of people due to the pandemic and vaccination status of COVID-19.

Again, "Can't you shrink it anymore? Then let's Zoom!", and see you at Pacifico Yokohama, April 2022!

Photomask Forever!!

BACUS

N • E • W • S

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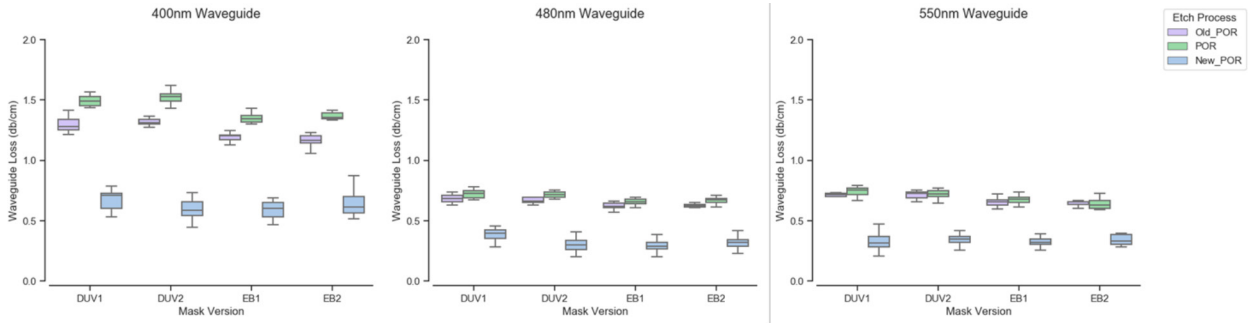


*Figure 2. Waveguide propagation losses across the four mask versions and three etch processes for (l-r) 400nm wide waveguides, 480nm wide waveguides, and 550nm wide waveguides.*

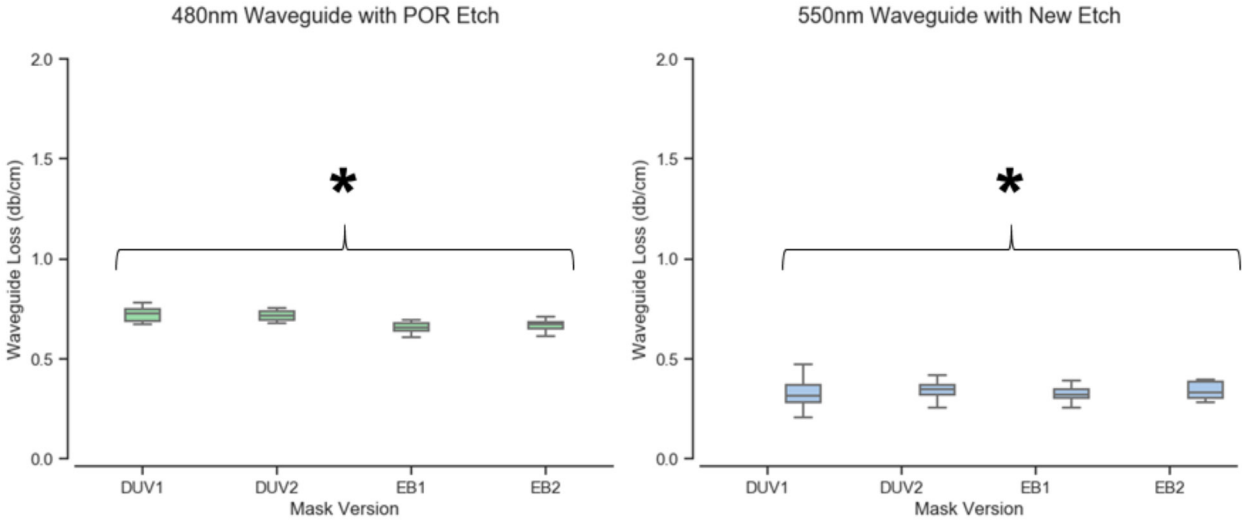


*Figure 3. Waveguide propagation loss for (left) 480nm wide waveguides fabricated with the current process of record etch across the four different mask versions and (right) 550nm wide waveguides fabricated with the "new" etch process. In both charts, there was no statistically significant difference between the four groups using a Tukey honest significance test (HSD) to a 95% confidence interval.*

## 1. Introduction

Silicon photonics is becoming a significant platform in high-bandwidth, low power device applications for High Performance Computing (HPC) and cloud computing infrastructure. Its continuing push to displace incumbent copper and VCSEL technologies depends on the scaling potential of existing CMOS manufacturing processes.[1-5] Central to the process is still the photomask, and its ability to accurately render design intent.

Critical to the construct of "photonic circuits" is the waveguide — a raised silicon track analogous to a metal track in a CMOS circuit. It is created in a similar manner — through litho-etch processes where a photomask is the source of the waveguide pattern. However, there are significant differences in how pattern fidelity affects the performance of an electrical path verses a photonic path. Digital IC has historically been most concerned about CD control, with emphasis online space metrology, and it is only recently that there has been a significant increase in interest online edge roughness metrics. In contrast, photonic waveguides are very sensitive to edge roughness, particularly sharp discontinuities with systemic periodicity. Additionally, photonic elements have curvature that is specifically defined for the wavelengths that are to propagate through the structure. This characteristic is a defining difference between photonic and electronic devices.

Early adoption of CMOS manufacturing processes for photonic applications were developed with quality specifications "ported" into the language of IC manufacturing, with minimum CD requirements dictating tooling and processes, both for photomask and wafer manufacturing. This seemed to be a reasonable assumption, given the much larger minimum feature sizes involved, ranging from 400nm to microns in line width.

However, the different sensitivities of photonic elements compared to electronic components require more than just "translation" for photomasks. These sensitivities may lead to unconventional or non-intuitive choices for data rendering (fracture) and mask pattern tooling (laser vs e-beam). Standard metrology (CD Uniformity, Localized LER) may not capture the essential elements that correlate mask pattern fidelity with waveguide signal loss. There are likely limits to a "blind translation" of IC-centric metrics to photonics-centric metrics.

## 2. Experimental

A silicon photonic waveguide was chosen as the baseline device to evaluate different photomask and wafer manufacturing processes. In particular, "racetrack" structures (typically used for waveguide propagation loss measurements) were chosen for both physical and optical characterization. (Figure 1).

Four photomasks were fabricated, to test different mask manufacturing processes and their impact on waveguide losses. All four were generated with standard data fracture practices for each tool involved. Existing metrology processes were used to validate the quality of the photomask (using standard IC quality specs).

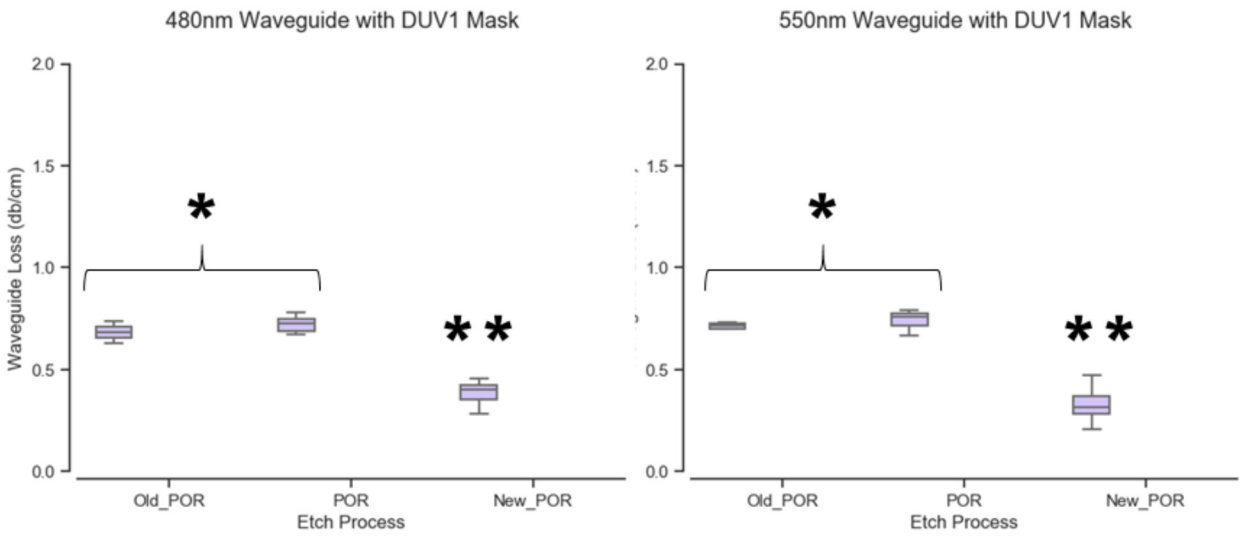


*Figure 4. Waveguide propagation loss for (left) 480nm wide waveguides fabricated with the DUV1 mask across the three different etch processes and (right) 550nm wide waveguides. In both charts, using a 95% confidence Tukey test, there was no statistically significant difference between the "Old POR" and the "POR" but the "New POR" did yield waveguides with significantly lower losses.*

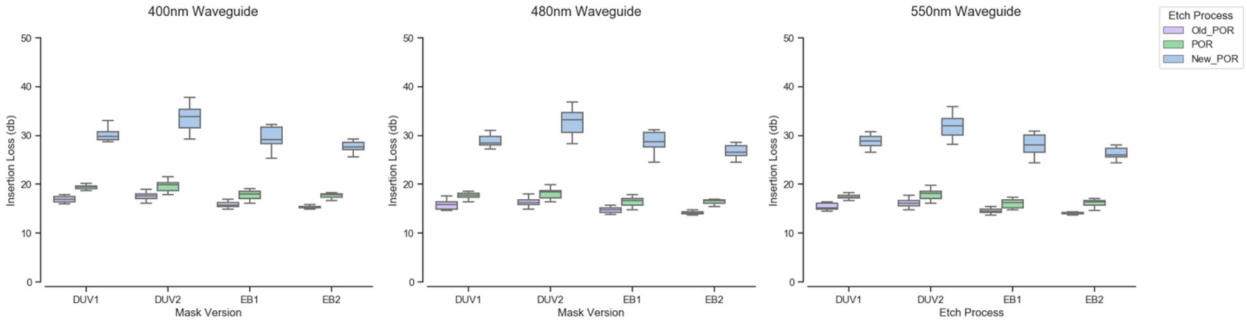


*Figure 5. Insertion losses across the four mask versions and three etch processes for (l-r) 400nm wide waveguides, 480nm wide waveguides, and 550nm wide waveguides.*

Mask 1: DUV laser mask, standard manufacturing process
Mask 2: DUV laser mask, standard manufacturing process (upgraded laser)
Mask 3: E-beam mask, standard manufacturing process
Mask 4: E-beam mask, enhanced process for advanced CMOS.

Standard QA metrology (CD targeting = 406.5nm reticle scale) using established production methods was obtained. Additionally, line edge roughness (LER) data was obtained on three linear racetrack "sites" corresponding to three different photonic waveguide widths used for performance testing. (Site 1 = 400nm wavelength, Site 2 = 480nm wavelength, Site 3 = 550nm wavelength).

Each of the four masks was used to expose test structures on a 300mm silicon-on-insulator (SOI) wafer using 193nm immersion lithography, similar to previously described work {REF}. Here, each quadrant of the wafer was exposed by one of the four masks in order to minimize wafer-to-wafer variability in the manufacturing process, while also capturing any within wafer (eg, center to edge) variability within each wafer quadrant. Three different wafers were fabricated using slightly different patterning processes: 1) standard reactive ion etch (RIE) or "Old Process of Record (POR)"; 2) RIE with simple over-etch ("POR"); and 3) RIE with sidewall post-treatments ("New POR").

After etching, in line metrology data was collected using an Applied Materials (Santa Clara, CA) VeritySEM 6i CDSEM, including both standard CD measurements, and various roughness measurements. The wafers were then deposited with enough silicon dioxide material to form a top cladding layer for the fabricated silicon waveguides.

Automated optical measurements were collected using a Keysight Technologies (Santa Rosa, CA) 81606A Tunable Laser Source and a N7745A Optical Multiport Power Meter. The optical power transmitted through 400nm, 480nm, and 550nm wide waveguides was collected from 8 different waveguide lengths from 1cm to 10cm long racetracks. The slope of a linear fit from these 8 different lengths is calculated as the waveguide loss (in db/cm) for each waveguide width, mask version, and etch process. The y-intercept of these linear fits is the insertion loss, which includes all other losses from the laser source to the detector, most significantly the coupling loss from fiber to wafer and wafer to fiber, and bend loss in the racetracks. These losses are assumed consistent across the different racetracks, and while they could vary from mask-to-mask or wafer-to-wafer, they are subtracted out to give the propagation loss on a die level.

## 3. Results

The overall waveguide loss results are shown in Figure 2. In general, the "New POR" waveguide etch process produces waveguides with lower loss across the waveguide widths tested and across the mask versions used to pattern the waveguides. The "Old POR" waveguide etch process was also consistently slightly better than the "POR" etch process.

In order to further examine the effect of mask fabrication on the performance of waveguides two subsets were studied more closely: "POR"

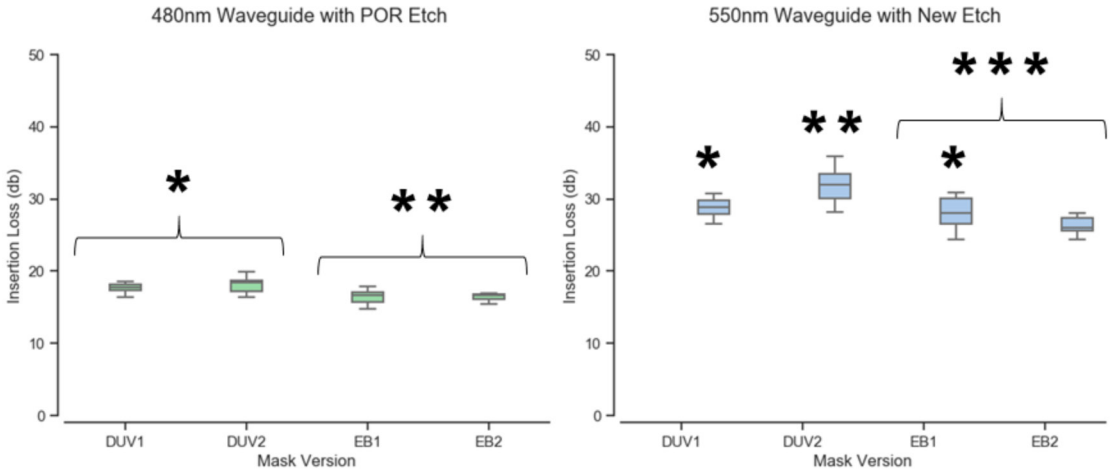


*Figure 6. Insertion loss for (left) 480nm wide waveguides fabricated with the current process of record etch across the four different mask versions and (right) 550nm wide waveguides fabricated with the "new" etch process. On the left chart, the losses from the ebeam masks were significantly lower than from the DUV masks, but there was no statistical difference between the DUV masks or between the ebeam masks. On the right chart, the losses from the DUV1 and EB1 masks were grouped; from the EB1 and EB2 masks were grouped, and from the DUV2 mask was not grouped with any other group. Again, the Tukey HSD method was used to the 95% confidence interval.*

**Table 1. Mask metrology results. All values are at wafer scale (1X).**

| Mask | Mask CD (1X) | | | | Mask LER (1X) | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Design CD Tgt (nm) | Mask Qual CD (nm) | Mask Delta to Tgt (nm) | 3Sigma (nm) | 400nm Waveguide LER, nm | 400nm Waveguide range, nm | 480nm Waveguide LER, nm | 480nm Waveguide range, nm | 550nm Waveguide LER, nm | 550nm Waveguide range, nm |
| DUV1 | 406.5 | 426.512 | -20.012 | 16.762 | 5.99 | 7.139 | 5.066 | 6.020 | 5.663 | 7.021 |
| DUV2 | 406.5 | 401.247 | 5.253 | 15.824 | 3.214 | 3.895 | 5.059 | 6.574 | 4.058 | 4.866 |
| EB1 | 406.5 | 399.395 | 7.105 | 5.188 | 3.471 | 4.862 | 2.678 | 4.025 | 3.901 | 5.856 |
| EB2 | 406.5 | 393.818 | 12.683 | 5.908 | 2.321 | 2.827 | 3.205 | 4.382 | 3.331 | 3.823 |

etch on 480nm waveguides, and "New POR" etch on 550nm waveguides. These etch and waveguide widths were chosen because they are the current and planned processes of records and standard waveguide widths for the fab, respectively.

Figure 3 shows these subsets of waveguide loss data. The "POR" 480nm wide waveguide propagation loss is not significantly different across the mask versions when examined with Tukey's Honestly Significant Difference (HSD) comparison test. In addition, the "New POR" 550nm wide waveguide propagation loss is also statistically insignificant across the four mask versions.

Instead, if a single masks versions (DUV1) is studied, the effect of the etch process for 480nm waveguides and 550nm waveguides is shown in Figure 4. Here the "New POR" is statistically significantly different from the "Old POR" and the "POR" etch processes. Therefore, it appears that the performance of straight waveguide structures is more dependent on the wafer fabrication process then it is on the mask fabrication process.

Separately, the insertion loss from these measurements is shown in Figure 5. Here, the "New POR" etch has the highest insertion loss across waveguide widths and mask versions, followed by "POR" and "Old POR". This is likely a function of the way the grating couplers are fabricated with the different etch processes. A grating, or vertical, coupler redirects light from the optical fiber in the test system into the waveguide, and then again out of the waveguide and back into an optical fiber for measurement. This insertion loss is also be a function of the waveguide bends that are within the test structures. Both the grating coupler loss and the bend loss are captured within the insertion loss and subtracted from the propagation loss. Without additional test structures and data collection it is not possible to determine with loss mechanism is responsible for the differences in insertion loss.

As before, we focus on the insertion loss from "POR" etched 480nm waveguides and "New POR" etched 550nm waveguides in Figure 6. Here, we do find some significantly different results. For the "POR" 480nm waveguide the DUV masks are significantly higher than the ebeam masks. For the "New POR" 550nm waveguide there are significant differences across the masks except for the EB1 mask which bridges the DUV2 and EB2 masks.

The mask metrology results are summarized in Table 1. As these mask processes were all developed to support the CD resolution requirements of ever shrinking CMOS designs, the CD uniformity improves significantly in going from the DUV laser to the ebeam mask POR. This was to be expected, and part of the interest of this study was to determine if CDU was as important to waveguide performance; or was there a different mask metric that should be captured and specified such as line edge roughness (LER) or correlation length (CL)? So first we need to determine if there is a significant waveguide performance difference with the different mask PORs. If there is, then can we determine what variable of the process or resulting mask feature is contributing to the WG performance difference? If there is no waveguide performance difference, then the more cost-effective mask POR can be used until advances in the wafer process are achieved, and this kind of testing can be repeated at that time.

Based on the data shown here, it does not appear that the improved CD uniformity from advanced CMOS-centric photomask fabrication translates to improved waveguide performance. If there is any improvement, it is within the error of the measurements and statistically insignificant. In comparison, improvements to wafer fabrication processes (POR vs New POR) do yield lower waveguide losses.

## 4. Discussion

Waveguide loss is governed by absorption (primarily a material property) and scattering. Scattering is a function of the roughness of the waveguide (top, bottom, sides) and any other materials in close proximity to the waveguide. Therefore, the only potential source of waveguide loss related to lithography is the sidewall roughness of the waveguide. It is plausible that the roughness or uniformity of the waveguide on the reticle could affect waveguide loss for waveguides that have moderately high losses to begin with; starting with a poor waveguide process could allow for mask patterning improvements to have an improvement on waveguide loss. However, here we use mature 193nm immersion lithography and advanced reactive ion etching, so the improvements from advanced CMOS-centric mask writing appear to be negligible compared to non-lithographic loss mechanisms such as the waveguide material, cladding material, or top/bottom roughness. In other words, non-lithographic contributions to waveguide loss appear to overwhelm patterning improvements when waveguide loss is already rather low.

Waveguides are straight lines and the propagation loss measurement used here subtracts out any other part of the test structure. Therefore, it is reasonable to think that mask manufacturing developed for very straight CMOS lines would yield straight photonic "lines". However, silicon photonics is renowned for its curved features. In a raster based patterning process such as mask making, curved features are a unique challenge and it is possible that the different types of masks studied here could have a significant impact on how curved photonic features are translated from design to the wafer. Most directly, curved waveguides are required to move light around the photonic chip, but other photonic devices (resonators, filters, switches, modulators, couplers, etc.) rely on non-Manhattan structures as well. Future studies should be undertaken to characterize what, if any, affect mask writing processes have on the translation of curved features. This can be done by repeating a similar experiment as described here, but with other performance metrics. Instead of focusing on waveguide loss, a follow-up study would focus on bend loss, coupling loss, resonance frequency, etc.

## 4. Conclusion

Waveguide propagation loss was chosen as a basic performance metric for photonic integrated circuits and used to compare mask manufacturing methods and waveguide fabrication processes. The four mask methods were nominally improvements over each other when applied to electronic integrated circuit production. No statically significant difference was observed across any of the mask types for waveguide propagation loss. While waveguide loss was not modulated by different mask versions, it was significantly improved by using different wafer fab processes. This suggests that, for waveguide loss at least, the wafer fab process has a bigger affect than the mask fab process. This is in spite of the fact that the mask versions perform better for IC-centric applications and even have improved line edge roughness. However, focusing on waveguide loss subtracts out any impact the mask processes may have on other photonic devices, namely curves where IC-centric mask manufacturing has not been optimized. Indeed, when the "insertion loss" for the waveguide loss test structure is analyzed there does appear to be some statistically significant differences across the mask types. Additional test structures are required to determine where these differences are derived from (eg, bends or grating couplers) and is an area of interest for future study.

## 5. Acknowledgements

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# Industry Briefs

## Bosch opens wafer fab of the future in Dresden

Bosch Press release

Dresden, Germany: Bosch is opening one of the world's most modern wafer fabs. Highly automated, fully connected machines and integrated processes, combined with methods of artificial intelligence (AI) will make the Dresden plant a smart factory and a trailblazer in Industry 4.0. In the virtual presence of Federal Chancellor Dr. Angela Merkel, EU Commission Vice-President Margrethe Vestager, and Saxony's Minister-President Michael Kretschmer, the high-tech facility was officially inaugurated on June 7, 2021.

https://www.bosch-presse.de/pressportal/de/en/bosch-opens-wafer-fab-of-the-future-in-dresden-230080.html

https://www.dw.com/en/bosch-is-the-new-star-in-silicon-saxony-microchip-cluster/a-57767731

## Rising demand from the semiconductor industry: Jenoptik plans to expand its optics manufacturing capacities – also in Dresden

Optics Manufacturing

As a result of the rising demand for optics and sensors for the semiconductor industry, Jenoptik intends to expand its manufacturing capacities and invest in a state-of-the-art manufacturing building and a new office complex at its Dresden, Germany, site. To this end, Jenoptik acquired a 24,000 sqm (260,000 sqft) plot of land in the Airportpark Dresden in May 2021.

https://www.jenoptik.com/press/pressreleases/2021/06/02/expanding-optics-manufacturing-capacities

## IMW Highlights 3D Architectures In-Memory Computing

Gary Hilson, EETimes

There's been a lot of discussions about how memories other than NAND flash could go three-dimensional, as well as how memory devices could best me stacked to deliver the speed, performance and thermal properties to meet the demands of high-performance workloads such as artificial intelligence and machine learning.

https://www.eetimes.com/imw-highlights-3d-architectures-in-memory-computing/

## IB Unveils World's First 2 Nanometer Chip Technology

Albany, N.Y.

IBM (NYSE: IBM) unveiled a breakthrough in semiconductor design and process with the development of the world's first chip announced with 2 nanometer (nm) nanosheet technology. It is projected to achieve 45 percent higher performance, or 75 percent lower energy use, than today's most advanced 7 nm node chips. The potential benefits of these advanced 2 nm chips could include: Quadrupling cell phone battery life, only requiring users to charge their devices every four days; slashing the carbon footprint of data centers, which account for one percent of global energy use; drastically speeding up a laptop's functions, e.g., assisting in language translation more easily, and contributing to faster object detection and reaction time in autonomous vehicles.

https://newsroom.ibm.com/2021-05-06-IBM-Unveils-Worlds-First-2-Nanometer-Chip-Technology,-Opening-a-New-Frontier-for-Semiconductors

See also:

TSMC 2nm https://www.eetimes.com/tsmcs-chip-scaling-efforts-reach-crossroads-at-2nm/

# Join the premier professional organization for mask makers and mask users!

## About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Listed as a Corporate Member in the BACUS Monthly Newsletter

**spie.org/bacushome**

## CALENDAR

### 2021

**The 36th European Mask and Lithography Conference, EMLC 2021**
22 June 2021
**Digital Event**
www.emlc-conference.com/en

**SPIE Photomask Technology + EUV Lithography**
26-30 September 2021
https://spie.org/conferences-and-exhibitions/puv

### 2022

**Photomask Japan**
25-27 April 2022
PACIFICO Yokohama
Yokohama, Kanagawa, Japan
www.photomask-japan.org

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**You are invited to submit events of interest for this calendar. Please send to lindad@spie.org.**