Deep sub-wavelength mask assist features and mask errors printability in high NA lithography

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ABSTRACT

As silicon processes scale toward the 45 nm node using conventional 0.25 magnification, widths of sub-resolution assist feature (SRAF) and printable defects on photomasks drop far below the ArF laser wavelength. Adoption of polarized illumination and higher numerical aperture (NA) could invalidate the scaling relations we used in the past to determine which small mask features or errors will print on wafers. Polarization interaction with small mask features may also plays a role in mask inspection. As mask features shrink below the wavelength, differences between the optical systems used for inspection and printing become more significant, and may affect the rules for disposition of inspection results. The data presented here combines experimental results from high NA imaging of sub-wavelength SRAF and defects, with rigorous calculation of their images based on vector diffraction. The printability of these deep subwavelength mask feature determines the requirements of optical model’s rigorousness for SRAF design rule and also mask defect inspection & repair capabilities.

1. Introduction

Under high NA immersion lithography, the dimensions of primary feature and their SRAFs on photomask are scaled down toward deep sub-wavelength regime. As the vectorial imaging effects increases significantly in high NA immersion lithography, the printability of mask defect and SRAF will depend on the composite effects of illumination vectors, Wood-Rayleigh resonance anomaly, mask material dependent 2-D feature proximity, optical proximity correction (OPC) features, mask topographic shadowing, effective mask glass trenching, and even pellicle membrane. The rule of thumb for defect printability threshold band for conventional masks will require thorough study to re-investigate the multi-parameter space in the high-NA imaging landscape. A rigorously defined mask defect control spec and mask inspection capability requirement are vital to the success of immersion lithography. Likewise, to enable a viable full chip process window tapeout, the sizing, filling and placement of SRAF in deep subwavelength regime also requires rigorous treatment of design layout to include all the optical, geometrical and materialistic elements in the entangled imaging system.

2. Simulation vs. experiment benchmark

To validate the computational model and its predictability, simulations performed with a Finite Difference Time Domain (FDTD) electromagnetic solver with 2 nm grid size are compared with experimental image measurements of the polarized off-axis illuminated gratings patterned on advanced photomasks. The measurements were performed on an immersion lithographic imaging test platform with 193 nm laser source on the AIMS™ 45i at Carl Zeiss SMT. A more detailed description of the imaging system can be found in Ref. The thru-pitch coherent curves of image contrast, maximum intensity and minimum intensity are benchmarked between the FDTD simulation and the imaging experiment. The main features are 1D unassisted space pattern. Owing to logistic restriction during the measurement, different illumination setting is used on different pitch. For the pitches at 2.5X to 6X of unassisted space CD, the illumination mode is linear polarized dipole in preferred state with inner edge of $\sigma = 0.8624$. 

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Driving Next-Generation Yield

J. Tracy Weed, Synopsys, Inc.

Outside our business lives we’ve all been driven: Driven to Tears (Police); Driven to Distraction (e-mail); Driven to Extremes (Michael Schumacher book). Business-wise we’re more likely driven by desire to succeed, to lower costs, improve accuracy, reduce defects, increase productivity and the one that seems to bring all of these into focus: driven by Moore’s Law to move from one technology node to the next. As we travel this path there seems to be one constant, the fact that we are continually forced to reexamine yield. What affects it, how to predict it and ultimately how quickly we can attain the yield necessary to support our ROI (return on investment) calculations?

In an effort to answer the difficult questions associated with attaining next-generation yield, Reed Electronics Group and Synopsys, Inc. sponsored the Next-generation Yield panel at SEMICON West 2007. Pete Singer, editor in chief of Semiconductor International magazine, and Ron Wilson, executive editor of EDN magazine, moderated the panel. Panelists included key executives from industry-leading companies at different points along the design-to-silicon value chain: Daniel Armbrust, VP, 300mm Semiconductor Operations, IBM Systems & Technology Group; Christopher Progler, CTO, Photronics; and Anantha Sethuraman, former VP, DFM solutions, Synopsys.

Progler seemed to have his finger on the pulse of the leading edge technology. Straight away, he pointed out that in order to improve yield, a meaningful connection must be made between what is imaged and the device performance. Progler highlighted the fact that the most successful designs are those that consist of more regular (very memory-like) patterns having fewer pitches and features. Given that the majority of the industry designs are not memory, Singer then asked how accurately the yield of a given design can be predicted. Armbrust stated that IBM has successfully predicted yield for 90 nanometer (nm) and 65 nm prototypes to within 10 percent. Progler indicated that the mask makers have much more difficulty predicting yield because they are not yet able to routinely determine if a given defect will print, or what the impact of the defect will be on the performance of a given device.

Sethuraman was also quick to point out that while strain engineering is being used to enhance device performance, understanding yield must include the ability to model, analyze and “repair” stress in order to address the variations in mobility and drive current. These variations can be as high 20 percent across a standard cell and range to 1.5 micron. Without the ability to account for these variations and feed them into the SPICE simulations, design variability will be far too high to provide meaningful yield.

So, what’s driving next-generation yield? To a large degree, issues resulting from the design / process interactions. This represents a significant shift from our focus on random defect reduction/control and drives a significant level of analysis and characterization. So please ...when driving next-generation yield, always look both ways for systematic and parametric yield issues. The yield you save could be your own.
Figure 1. Immersed image contrast, maximum and minimum intensity benchmark between FDTD simulation and imaging experiment. Here, IFS=92.5% is assumed in the simulation to match with the experimental condition.
and outer edge of $\sigma_{\text{out}}=0.98$. For the pitch at 2X of space CD (i.e. line: space=1:1), the illumination mode is linear polarized dipole in preferred state with $\sigma_{\text{in}}=0.686$ and $\sigma_{\text{out}}=0.98$. To match up with the experimental condition, the intensity of preferred state (IPS:=I_{\text{pol}}/I_{\text{tot}}) is set to 92.5% in the FDTD simulation assuming a tilted linear polarization from the preferred state. The mask absorber stack under study through out of this paper is composed of 18nm CrO on top of 30nm Cr film. Mask total process bias (measured CD - tape CD) of +10nm on mask space feature is accounted in the simulation. The images being measured in this study are at the interface of between water (refractive index $n=1.44$) and resist film ($n=1.70$) on wafer. With an approximately constant k1 factor of 0.28, where $k_1:=\text{NA} \times \text{half-pitch}/\lambda$; the calculated immersed image characteristic agreed well with the experimental results across the 3 cases of space feature under 0.28k1-scaled NA, as shown in Fig. 1.

3. **Mask defect and its proximity printability**

The printability of 1-D defect (or 1-D CD bias) on 1-D pattern under linear polarized dipole illumination in the preferred state is studied in this section by FDTD. Full matrix of 2-D and 3-D defect printability including 2-D OPC features is beyond the scope of this paper and will need to be explored extensively. To evaluate the direct impact from mask defects, IPS is assumed to be 100% in the simulated illuminator. The convolution of illumination polarization impurity and mask defect would only lead to worse mask defect printability owing to the inherent nature of image contrast degradation due to the polarization impurity. In Fig. 2, the MEEF (Mask Error Enhancement Factor) is generally ≤ 1 at focus on 80nm, 58nm and 45nm half pitch (hp) line-space patterns. A preliminary experiment result has indicated that the MEEF under the condition of IPS at 92.5% is about a factor of two compared with the simulated estimation when IPS=100%.

The lower than 1 or 2 of MEEF on primary pattern is not surprising as both the illumination shape and polarization orientation are aligned and optimized along with the mask pattern, where high contrast imaging at low k1 along the optimized direction is enabled. Noticeably, the image at defocus could have even lower MEEF of ~ 0.4 for the case of 58nm hp, and MEEF of ~ 0 at 45nm hp. This is explained with reference to Fig. 3, which shows images of 58nm hp under 0.93NA linear polarized dipole illumination. Out of focus, the image of the defective space splits due to nontelecentricity of the dipole illumination, and affects images of adjacent spaces instead of the one at the center of the pattern. The defect and mask CD error proximity printing through focus will need rigorous specification and mask quality control at high NA sub-wavelength tight pitch regime.

In Fig. 4, the characteristic of mask induced polarization, where degree of polarization is DoP=$(I_{\text{te}}-I_{\text{tm}})/(I_{\text{te}}+I_{\text{tm}})$, of both 0th and 1st diffraction orders indicates that the mask induced polarization has no significant dependency on 1-D mask error size. In comparing with Fig. 2, the mask error printability also appears no significant sensitivity to the mask induced DoP in either extra clear or extra Cr regime.

4. **Mask SRAF and its proximity printability**

The scaling of printability described in Section 3 is in general valid for 1-D mask defect or CD error deviation from target as well as for the case of 1-D edge biased OPC. When OPC features are detached from the primary patterns, as is widely called as SRAF, or “scattering bar”, the design rule of SRAF will need to ensure robust non-printability through focus and through dose under high NA optical system. The printability of 1-D SRAF on 1-D pattern under linear polarized dipole illumination addressed in this section is also studied by FDTD simulation.

In Fig. 5, example of through-focus image CD projected from 3:1 45X4=180nm mask feature has shown depth of focus (DoF) being improved by SRAF within 10% primary CD focus range, right before the SRAF is printed at defocus. Overall, larger size of SRAF on mask improves the imaging DoF of primary feature, as depicted in Fig. 6.

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Figure 2. Calculated mask defect printability and MEEF on 1:1 mask feature thru focus behaviors at 0.28k1 scaled pitches. Here the illumination is linear polarized dipole 100% in the preferred state with: $\sigma_{in}=0.86$ and $\sigma_{out}=0.98$. 
Before SRAF is printed within DoF and exposure latitude, DoF at optimal point has been improved by a factor of 1.7X at 58hp, 2.5X at 45hp, and 20X at 38p. The threshold being assumed here is the threshold chosen at target 1:1 line/space dense feature being imaged at its half pitch. The significantly small DoF of un-assisted primary 3:1 feature at 45nm and 38nm nodes is due to the marginal intensity threshold for CD targeting through focus. With the constant 0.28k1 NA scaled pitch, the ratio of optimal SRAF size to the primary feature size on mask is maintained about 50%. Other considerations, such as 2-D proximity effects, tighter duty ratio or guardband for process marginality, would reduce the design rule of SRAF below the 50% ratio to the primary feature size.

The nontelecentric image shifts noted in the discussion of Figure 3 can cause apparent printing of SRAFs out of focus, the worst condition being when the shifted image of the primary feature created by one pole of the dipole configuration coincides with the shifted image of an SRAF created by the other. Even without SRAFs, the opposing shifts can reverse the contrast of the image out of focus, as can be seen from Figure 5.

5. Summary

In summary, high NA immersion image measurement system has validated the FDTD model for the calculated immersed image characteristic at a constant 0.28k1-scaled pitch up to 1.4 NA. At these scaled pitches, 1-D mask error or 1-D OPC bias has generally MEEF ≤ 1 under linear polarized dipole illumination. Pattern orientation orthogonal to the illumination optimized direction will require design restriction and/or rigorous OPC. When focus-exposure is deviated from target, proximity printing from mask defect or OPC at dense pitch and SRAF is substantial and will require significant control of mask inspection and repair disposition as well as rigorous OPC algorithm and optical rule check. Mask induced polarization has no sensitivity to the 1-D mask sizing or error. With the constant 0.28k1 NA scaled pitch, the ratio of optimal SRAF size to the primary feature size on mask (before SRAF is printed at defocus and at out of target dose and before other full-chip patterning considerations) is scaled with approximately constant 50%. Finally, the intensity of preferred state (IPS) at the polarized illuminator plays a vital role in imaging contrast and thus lead to substantial impact to the printability of mask defect, traditional edge biased OPC and also printability of detached OPC features (i.e. SRAF). IPS could double the MEEF as being observed. As a consequence, along with the quality control of photomasks, IPS on illuminators of image based mask inspection, image based mask disposition tools as well as optical scanners will also be required tight quality control in the up and coming highly entangled imaging system for immersion lithography.

6. Acknowledgment

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data collection; as well as Jeff Farnsworth and Jun Kim at Intel for their advises.

7. References


5. D. Pettibone et al, “Wafer printability simulation accuracy based on UV optical inspection images of reticle defects”, Proc. SPIE Vol. 3677, 711, 1999; which identified defect printability threshold range of conventional masks is $0.08 < k_{\text{defect}} \leq 0.35$.


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Figure 4. Calculated mask induced polarization vs. various 1-D mask CD errors.
Figure 5. Calculated SRAF printability through focus and DoF improvement from SRAF on (line : space = 3:1) semiisolated primary space pattern. Here, IPS=100% is assumed. All scale here is micrometer at 1X.

Figure 6. Calculated DoF improvement from SRAF sizing for semi-isolated (line : space = 3:1) primary space pattern.
Industry Briefs

■ High Interest in Low-End Printable Electronics
   (Semiconductor International, July 2007).

Doubling transistor density does little to improve performance or cost of many emerging applications. RFID tagging requiring only 100’s of bits simplifies manufacturing and shipping logistics. A simple sensor array adheses to the skin of an airplane or a medical patient. Hikers and military units might appreciate a map with an embedded GPS indicator, especially if foldable and portable. Current technology is neither mechanically robust enough for full-scale electronic maps, nor cheap enough for disposable electronic tags. Printing systems measure their output in meters per minute and achieve costs per area as much as two or three orders of magnitude less than silicon CMOS. This is because printing is a low temperature, atmospheric pressure process, compatible with any substrate material.

Printable electronics demand functional inks with conducting, insulating, and semiconducting properties. While conventional printing methods cannot yet meet the resolution requirements of even simple electronic circuits (smallest printed features =10µm), but this limitation is not necessarily inherent in the technology. Rather, printing presses have not been asked to produce subvisible features before.

The most mature group of electronic inks are metallic inks used in both decorative and electronic applications. They consist of a suspension of metal particles in a solvent and create a conducting path with a higher resistance than a conventional wire, due to the gaps between particles. Larger metal features, like inductors, may be able to be milled from metal foil, with throughput up to 160 m/min. The second important component of printable circuits, the dielectric, faces a challenge opposite that of metallic layers. Thinner layers are desirable because they reduce the operating voltage of the device. Suitable dielectric materials are many different polymers. One common approach to the deposition of thin continuous dielectric films depends on self-assembled monolayers (SAMs) composed of molecules in which one end preferentially bonds to the substrate, while the other is repelled by it. Thus, the material coats the substrate with a uniform, aligned monolayer.

Very small feature sizes can be achieved, as the initial mold fabrication can use all the tools of maskmaking and other direct-write lithography methods. “Soft lithography,” as this stamping of SAMs is known, is potentially compatible with roll-to-roll processing. While it is hard to predict the market size for the printable electronics, it is not unreasonable to expect that it may be huge.

■ IMEC Sees Double Patterning as Next Step Towards 32nm

By Christoph Hammerschmidt, EE Times Europe/Munich, Germany (07/16/2007)

At Semicon West trade fair, Belgian research institute IMEC announced double patterning emerging as a probable intermediate solution for the 32 nm lithography.

IMEC CEO Luc Van de hove sees significant progress in the 32nm lithography during the past year.

In the area of double patterning, IMEC presently investigates challenges such as mask design split, cost-effective processes, and critical dimension (CD) and overlay control. The research institute has demonstrated the potential capability to achieve sub-3nm critical dimensions, which is one of the requirements for 32nm production. IMEC simulations have shown that a more uniform wafer CD distribution can be obtained by minimizing the mean difference between the CD populations.

IMEC is developing techniques to split full chip designs automatically, which will be required when the double patterning technique is to be used in production environments. In collaboration with EDA, IMEC researchers are investigating how double patterning will affect workflows and how designs can be made split-compliant.

In the immersion lithography, IMEC will extend its strategic partnership with ASML. While the current research is carried out on an ASML XT:1700i with a numerical aperture of 1.2, both parties now agreed to install a new XT:1900i with an NA of 1.35. The target of high-index immersion lithography is to drive the NA to a range of 1.55 to 1.6, to enable to extend the 193nm immersion lithography to the 32nm half pitch node. At least one fluid was found that seems to meet most criteria required for the technology.

According to IMEC, EUV is the only technique extendable to 22nm and beyond. IMEC worked on integrating the ASML alpha tool with Sn EUV source as well as the optics, fine-tuned for high resolution image and acceptance testing. The research program so far has been focusing on interference exposures for resist preparation, design tape-outs as well as EUV simulations.
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