Model-based mask verification

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1. ABSTRACT

One of the most critical points for accurate OPC is to have accurate models that properly simulate the full process from the mask fractured data to the etched remaining structures on the wafer. In advanced technology nodes, the CD error budget becomes so tight that it is becoming critical to improve modeling accuracy. Current technology models used for OPC generation and verification are mostly composed of an optical model, a resist model and sometimes an etch model. The mask contribution is nominally accounted for in the optical and resist portions of these models. Mask processing has become ever more complex throughout the years so properly modeling this portion of the process has the potential to improve the overall modeling accuracy. Also, measuring and tracking individual mask parameters such as CD bias can potentially improve wafer yields by detecting hotspots caused by individual mask characteristics. In this paper, we will show results of a new approach that incorporates mask process modeling. We will also show results of testing a new dynamic mask bias application used during OPC verification.

1. Introduction

Advanced semiconductor lithography technology nodes require tight CD control. Optical proximity correction, OPC, is used to compensate for lithography process limitations. OPC quality is highly dependent on the accuracy of the model used to simulate the transfer from polygons in the fractured mask data file to the shape remaining on the wafer after etch. Up to now, mask

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Interesting times

Impressions from SPIE Advanced Lithography 2008

Artur Balasinski, Cypress Semiconductor Corp.

We are at the crossroads of lithography development. This is fascinating. As usual in such situations, the scenarios offered by the optimists and the pessimists, are more polarized than ever. Let me assert: the pessimists are just differently abled optimists.

Optimists say: More Moore. Pessimists declare: No more Moore. Who is right?

Optimists say: EUV is catching on. There would be production tools released in 2009. Pessimists rebut: There are no masks and no photore sist. Yet, Intel engineers are optimistically designing to them. But they are pessimistically looking over their shoulders, why is everyone light-years behind them and not even trying to catch up.

A side note: NIL is nil with 4 wafers per hour. This candidate seems to have lost the primary, but some are still working on a re-vote by mail.

Optimists: Double patterning, the only non-exotic technology for 22 nm, is gathering steam. They happily note that there are not enough CAD tools to rework the layouts. EDA startups charge to the solutions expanding the cost model. Inverse lithography moves from folklore to mainstream. Interestingly, major pessimistic companies, which gave up on their own process development, are giving it a nod.

Pessimists ask: having enough problems ramping up 65 nm, why would one need to crank it down to 22 nm, where the cost of mask building, pattern generation, and defect inspection equipment, doubling for each generation, goes through the roof. Optimists say: yes, things are still accelerating and the mask shops are still with us. Pessimists say: actually, things are slowing down, it is not 2x but only 1.6x reduction per node, and we are actually loosing mask shops underway.

Optimists see a lot of new applications, both in memories and logic. The customers are still hungry for bytes and computing power. Pessimists are looking at the Concorde syndrome. The SST technology, a logical extension of speed and demand operated for 30 years before its optimistic business model folded. Such is probably the lot of every technology. Are we there yet?

Fortunately, there are also trends both optimists and pessimists embrace. Design for Manufacturability has found its mission, as a methodology to reduce device variability, identify and compensate systematic defects. No matter how device engineering would see it, past and future designs would benefit. The optimists cling to DfM as they march further down the nodes. The pessimists, who may see it as the art of survival, optimize and reduce cost with it. Going further in their pessimism, they may actually have no choice but to find new applications, and venture into new areas, by developing a different set of abilities. How about organic electronics? The masks may be back to the mylar foil, but when the electrically functional inks print thin film devices, we can make flexible displays, smart labels, animated maps and posters, active clothing. Not too shabby for a pessimistic scenario. May we live in interesting times.
manufacturing process imperfections have been accounted for in either the optical or resist models. Therefore, during model calibration, the lithography modeling system attempts to compensate for some effects using parameters that were not designed to fit the appropriate physics. This leads to limitations in model accuracy. To improve the accuracy of OPC lithography modeling we have designed and implemented a modified flow adding explicit mask modeling steps to the OPC lithography modeling process. To check the capability and the potential gain expected by this modified approach, this work is focused on the accuracy of mask process and CD uniformity (CDU) modeling.

2. Theory of Operation

The OPC verification process takes as input post-OPC data and uses lithography models to simulate the full chip resist image that will exist on the wafer after lithography. It then applies specific rules to determine potential wafer lithography hotspots by comparing simulation wafer contours to the pre-OPC lithography target data. The standard flow uses a scanner optics model to create an aerial image and then a wafer resist model to convert it to a resist contour. Our modified flow also starts from post-OPC data; it then uses a mask model to convert the post-OPC data into a mask contour. A mask CD uniformity model, derived from

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a specific mask, is then applied to take into account CD variation across the full mask. Then the standard flow is resumed, applying the scanner optics model to create an aerial image and the wafer resist model to convert it to a resist contour. Therefore, we have implemented a modified flow adding explicit mask modeling steps to the OPC lithography modeling process. This modified flow allows us to perform model-based mask verification.

3. Mask Process Modeling

This model simulates mask pattern proximity effects. Many e-beam mask error sources can be effectively modeled by a sum of Gaussian point spread functions with different ranges and magnitudes. Therefore, the Brion mask model includes several Gaussian functions convolved with mask patterns.

In addition, the mask model has linearity terms to simulate process errors at small feature sizes. These terms are sensitive to edge density instead of local pattern coverage alone (see Figure 1). Terms of a different implementation but with similar effects have been previously reported by Satake et al.

CD measurements on 1D/2D mask geometries along with mask SEM images can be used to calibrate the Brion mask model. Mask contours can then be generated on Brion’s Tachyon platform using the mask model and post-OPC patterns. These resulting contours can be used for mask process verification as well as input for wafer verification.

3.1 Mask Process Modeling Results

The predictive power of the mask models were verified through a number of criterion including the linearity, iso/dense, and corner rounding. Figure 2 shows the results of over 500 line/space measurements. These data show that the mask model predicts within 1% accuracy 93% of the time. The overall RMS error for the model on all gauges used was 0.84nm.

Accurate reproduction of corner rounding is also important so we used a stair-step design and tested the model’s ability at many different step sizes. Figure 3 shows the predicted mask contours overlaid onto SEM images of 3 different step sizes. The model has very good corner rounding prediction.

Figure 4 shows mask contours overlaid onto an SEM image of a production mask. Once again, the contours match well.

4. Mask CD Uniformity Modeling

After mask process modeling, there may still be long range mask CD variations. The sources of these variations are multiple (e.g. resist coating uniformity), including many that are not related to mask layout. Some are not well understood at this time. In order to account for these errors, another modeling capability has been developed to fit sparse mask CD measurements to a CD uniformity map. Since the underlying mask CD variation is expected to vary slowly across the mask, the algorithm makes trade-offs between fidelity to each measurement and the smoothness of the fitted map. This “smoothing” function is controlled by a model parameter $\lambda$. Figure 5 shows the results of smoothing the same set of data.
with different \( \lambda \) settings. Note that higher the \( \lambda \) values create a higher degree of smoothing.

The final generated CDU map can then be inserted for mask layout verification on the Tachyon platform. Additional hotspots due to mask CD variation may be detected.

### 4.1 Mask CD Uniformity Modeling Results

The mask CD uniformity capability was tested on both theoretical and actual CDU maps. Theoretical maps were used early in the development process in order to verify that the correct mask bias amplitude was being applied to the correct mask coordinates. Figure 6 shows a defect that was captured on a production design using a simulated CDU bias map. Further study verified that the applied bias amplitude and coordinates matched the CDU map.

The next step was to create CDU maps from production masks and use them in an overlay verification job. Figure 7 shows the resulting CDU maps from a 65nm design poly and active layers of the same set. The Brion Tachyon system is now able to take the pre and post OPC of these two layers and dynamically apply the bias maps to both layers simultaneously. The presence of both layers enables a set of “gate” detectors, which we used in order to measure the effects of using the CDU bias maps. Both the gate length and gate width detectors were set to 10% tolerance.

Table 1 shows the resulting defect counts for a small portion of the design. Applying the CDU bias maps added over 11,000 wafer hotspot defects. Due to the high quality of this particular mask set, the increase in gate width error due to mask CD uniformity continues on page 6.
was only 1.06%.
Certain other 65nm masks, not made by DNP, were checked during this study and they displayed a mask CD uniformity range above 10nm (see Figure 8).

5. Conclusion
With a new mask modeling technology, we have accurately predicted mask contours to within 0.84nm RMS error. We have also demonstrated that mask corner rounding can be well predicted throughout a wide variety of corner conditions.
This new mask modeling advance allows verifications where mask and wafer hotspots are identified before a mask is written. CDU bias maps generated from sparse or symmetrical CD SEM measurements can be modeled and fitted into a CDU map that can be used by the Brion Tachyon for model-based mask verification. These CDU maps are applied dynamically during the individual masks(s) wafer verification resulting in an overall increase in defect count and magnitude.

6. References

Table 1. Production mask defect counts with and without CDU bias.

<table>
<thead>
<tr>
<th></th>
<th>Total Defects</th>
<th>Gate Length Max Error</th>
<th>Gate Width Max Error</th>
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<tbody>
<tr>
<td>No Bias</td>
<td>128,084</td>
<td>-11.57%</td>
<td>11.75%</td>
</tr>
<tr>
<td>Both Poly and Active CDU Bias</td>
<td>139,783</td>
<td>-12.21%</td>
<td>12.81%</td>
</tr>
<tr>
<td>Delta</td>
<td>11,699</td>
<td>0.64%</td>
<td>1.06%</td>
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Figure 7. Actual CD uniformity maps used for the poly over active gate verification.
Figure 8. Example of a mask with 10nm CDU range.
Industry Briefs

■ Nanoimprint to get a Day in the Sun?

Semiconductor International

Molecular Imprints (MII) outlook is brightening up: they got Toshiba, Hewlett-Packard, Samsung, IBM and Seagate, an impressive list of customers. Recently, Sematech purchasing Molecular Imprints’ nanoimprint tool became the news of the day. The Step and Flash Imprint Lithography (S-FIL) machine is to demonstrate its feasibility for CMOS production at the 32 nm node and below.

For quite some time, there has been concern about defects, overlay, CD uniformity, and more. MII has made progress in these areas, and the work at Sematech’s Albany NanoTech signals increasing industry investment that could give the technology the final push to manufacturing. With Seagate’s hard disk drives as a challenge to Molecular Imprints, nanoimprint is becoming an imminent reality in the scaling efforts. The other next-generation lithography (NGL) technologies are not able to leverage this kind of learning that comes with practical experience in a big market.

Seagate and other disk drive companies use the Imprio 1100, which prints the whole disk at once. Therefore, they don’t have the tight overlay requirements of the CMOS. However, the disk drive industry is actally very synergistic to CMOS. There are many respects where the technology being demonstrated is quite awe-inspiring. Patterned media, where they can no longer use magnetic confinement, now has to etch the individual memory elements – every single bit on a magnetic disk. On a terabyte-size disk expected around 2010, that means 10 trillion sub-30 nm columns.

But regardless of the results the nanoimprint might be able to produce, it continues to face perception issues. The industry shrinks away at the mention of 1x technology, due to the expected high defectivity.

■ Projection Lithography Facing Challenges (What Else is New?)

Semiconductor International

Is the future projection lithography going to be optical or EUV, is a serious question and there are starkly differing views. Due to the “molten tin” sputtering from tin targets and flying through the EUV exposure systems, some are referring to them as deposition systems. But a key issue is not related to the technology and the challenges that it faces, but to its questionable economic models. Some hope that EUV as cost-effective solution would become a self-fulfilling prophecy: disregarding the absence of high-power source, defect-free mask and workable resist, they simply assume all the numbers that are needed to make EUV successful, and the model works.

But optical lithography does not face a particularly rosy outlook either. Double patterning, widely considered an extension of immersion lithography, doesn’t present a very friendly cost model, particularly for chipmakers producing fewer wafers per mask. It is perceived as only a one-generation extension of immersion lithography. By contrast, the EUV has presented a (believe it or not) plan to take it all the way down to the 11 nm node. High-index immersion as a means of extending optical lithography also does not help. For the high-index lens material (LuAG) needed for 1.70 NA imaging, the lens material absorption is at 0.05/cm, while it needs to be at 0.01/cm.

Companies like Toshiba, competing to push NAND flash as quickly and as far as they can, will grab hold of any technology that can promise a boost in resolution and continued scaling. But those solutions need to come sooner rather than later.
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Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

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spie.org/photomask

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