2022 CALL FOR PAPERS

SPIE. ADVANCED LITHOGRAPHY+ PATTERNING

27 February–3 March 2022
San Jose Convention Center
San Jose, CA

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1 SEPTEMBER 2021

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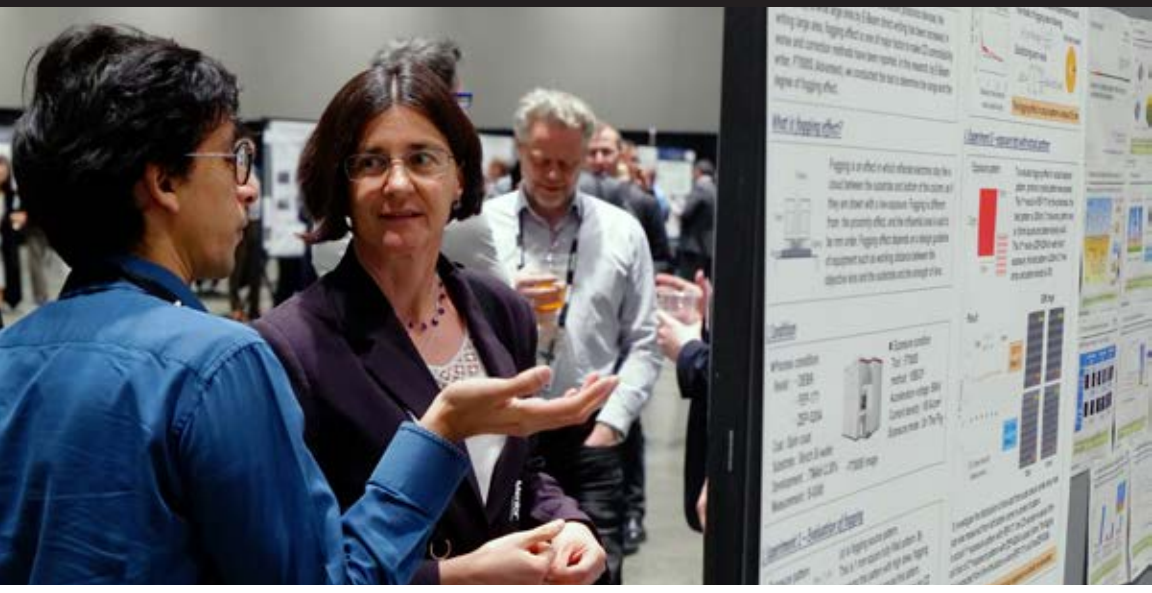
SPIE. ADVANCED LITHOGRAPHY+ PATTERNING

San Jose Convention Center
San Jose, California, USA

Conferences and Courses
27 February-3 March 2022

Exhibition
1–2 March 2022



Share your research and make important connections throughout the semiconductor industry

Present your work in optical lithography, metrology, or EUV. Share your latest advancements at the meeting where leaders come to network and solve lithography and patterning challenges. We look forward to gathering with you in San Jose.

Students attend for free

The Sponsored Student Grant aims to encourage student contributions to the Advanced Lithography + Patterning conferences through a program that pre-pays student registrations and gives travel/lodging reimbursements. This opportunity is open to any student wishing to attend the symposium.

Applicants must be students

- Only students may apply and must be enrolled for the full year beginning fall 2021 (Aug 2021-Jul 2022).
- Student authors will receive priority over student attendees, but student attendees are encouraged to apply.
- Preference may be given to those who have not received any previous grants from SPIE.

What does the scholarship cover?

- Registration fee
- Reimbursement towards travel and lodging*

Additional details to students:

- Authors with presentations will be given priority. Additional funding support for non-author students will be provided as funds are available.
- If the student is an author, then manuscripts must be received for proceedings on the specified due date.

For companies interested in sponsoring this grant, please email Aronm@spie.org for more information.

spie.org/al22call

Plan to participate

The SPIE Advanced Lithography Symposium has been the showcase for the latest advances in lithography and patterning technology for over four decades. The technology landscape keeps evolving to incubate more sophisticated and diversified information and computing technologies. The semiconductor technology sector, now in the More than Moore era, is facing more challenges that require holistic patterning solutions involving a higher level of interactions among process technologies, devices, and system design sectors. The 2022 Symposium will cover the full spectrum of the advances and challenges in state-of-the art lithography and integrated patterning technology through several topical conferences. Advances in the areas of nano- and micro-patterning for semiconductor IC device applications will be presented in sessions covering optical lithography, extreme-UV (EUV) lithography, computational patterning, metrology/inspection, patterning materials, etch/deposition technology, and system-design-technology co-optimization. As novel patterning and non-IC lithography technologies - such as heterogenous wafer packaging, IoT devices including micro-machines and microsensors, AR/VR devices, and FP Displays - have become more widely explored, related topics in these areas are also addressed.

To cope with the changes in the technology landscape and better serve as the premium platform for bringing together the lithography and patterning communities involved with semiconductor devices, micro-/nano-systems, AR/VR devices, displays and related fields, the 2022 Symposium is carefully restructured and renamed as the SPIE Advanced Lithography + Patterning (ALP) Symposium to emphasize the importance of these aspects. Specifically, this year's Symposium is structured into six conferences from the previous seven conferences. The motivation is to make each conference wavelength-agnostic and specialize on its own functional areas. The major change is the merging of the system and practice modules of the EUV and optical nanolithography conferences for advanced IC applications, while the non-IC applications module is moved to the novel patterning conference; the computational patterning module is merged with design technology co-optimization conference into a new computation-focused conference; and the material module is merged with the patterning material conference. Each of the six new conferences, as shown on the symposium web site, is organized by current practitioners of the art working together with organizing committees of experts in these fields. Joint sessions between the conferences will be aligned with several predefined application tracks: machine learning, stochastic effects, and overlay. This will offer attendees the opportunity to cover important topics common across these interest areas and minimize same topic presentation overlap.

Participants come from a broad array of backgrounds to share and learn about state-of-the-art advances of all aspects of patterning technologies. Through a series of provocative panel discussions and seminars, the symposium also probes current issues being faced as we extend current methods, move toward alternative approaches, and identify new ways to complement one technology with another. The Symposium also provides the unique and primary forum for meeting and interacting with a wide range of industry experts, researchers, academics, and key players working on patterning technology development. Attendance ensures that participants learn and share the latest developments in areas of central importance to many vital technology fields. We welcome your participation for the 2022 SPIE Advanced Lithography + Patterning Symposium, urge you to submit your abstracts to the appropriate conference as described in the individual calls for papers, and hope you will encourage your colleagues to do the same. Relevant topics for new technology groups, keynote talks, or panel discussions are also solicited.

2022 Symposium Chairs

Kafai Lai
Univ. of Hong Kong (USA)
Symposium Chair

Qinghuang Lin
LAM Research Corp. (USA)
Symposium Co-Chair

SPIE. ADVANCED LITHOGRAPHY+ PATTERNING

THE PREMIER EVENT FOR THE LITHOGRAPHY COMMUNITY

Contents

SPIE remains committed to advancing light-based research and meeting the needs of our constituents by providing you with an opportunity for sharing your work and connecting you with the global science and engineering community. We look forward to your participation.

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spie.org/signup

Optical and EUV Nanolithography XXXV (AL101)

Conference Chair: **Anna Lio,** Intel Corp. (USA)

Conference Co-Chair: **Martin Burkhardt,** IBM Thomas J. Watson Research Ctr. (USA)

Program Committee: **Steven L. Carson,** Intel Corp. (USA); **Will Conley,** Cymer, LLC (USA); **Andreas Erdmann,** Fraunhofer-Institut für Integrierte Systeme und Bauelementetechnologie IISB (Germany); **Nelson M. Felix,** IBM Corp. (USA); **Allen H. Gabor,** IBM Corp. (USA); **Kenneth A. Goldberg,** Lawrence Berkeley National Lab. (USA); **Paul Graeupner,** Carl Zeiss SMT GmbH (Germany); **Naoya Hayashi,** Dai Nippon Printing Co., Ltd. (Japan); **Soichi Inoue,** KIOXIA Corp. (Japan); **Young Seog Kang,** SAMSUNG Electronics Co., Ltd. (Korea, Republic of); **Bryan S. Kasprowicz,** HOYA, Inc. (USA); **Insung Kim,** SAMSUNG Electronics Co., Ltd. (Korea, Republic of); **Toshio Konishi,** Toppan Printing Co., Ltd. (Japan); **Ted Liang,** Intel Corp. (USA); **Chang-Moon Lim,** SK Hynix, Inc. (Korea, Republic of); **Luciana Meli,** IBM Corp. (USA); **Lawrence S. Melvin III,** Synopsys, Inc. (USA); **Hakaru Mizoguchi,** Gigaphoton Inc. (Japan); **Ken-Ichiro Mori,** Canon Inc. (Japan); **Patrick P. Naulleau,** Lawrence Berkeley National Lab. (USA); **Christopher S. Ngai,** Applied Materials, Inc. (USA); **Soichi Owa,** Nikon Corp. (Japan); **Vicky Philipsen,** imec (Belgium); **Moshe E. Preil,** KLA Corp. (USA); **Kurt G. Ronse,** IMEC (Belgium); **Daniel Sarlette,** Infineon Technologies Dresden GmbH (Germany); **Bruce W. Smith,** Rochester Institute of Technology (USA); **Akiyoshi Suzuki,** Gigaphoton Inc. (Japan); **Anna Tchikoulaeva,** Lasertec U.S.A., Inc. Zweigniederlassung Deutschland (Germany); **Edita Tejnil,** Mentor Graphics Corp. (USA); **Geert Vandenberghe,** imec (Belgium); **Claire van Lare,** ASML Netherlands B.V. (Netherlands); **Thomas I. Wallow,** ASML Brion (USA); **Obert R. Wood II,** GLOBALFOUNDRIES Inc. (USA); **Kenji Yamazoe,** TSMC North America (USA)

For over 50 years photolithography has been at the center of the growth of the semiconductor industry. The art of shaping matter with photons influences the way we live today and the drive into the future.

The need for more powerful chips and greater memory storage has driven the evolution of advanced lithography tooling, photomasks, processes, and systems. The advent of extreme ultraviolet lithography (EUV) at 13.5 nm and its introduction in high volume manufacturing (HVM) ensures the extendibility of lithography to tighter dimensions for the fabrication of more powerful devices and support the exponential growth of data management. Its use in conjunction with optical lithography (g-line, i-line, KrF, ArF) enables a wide range of resolution for new devices in an ever-increasing array of applications, like AI, IoT, silicon photonics, MEMS, etc.

Many opportunities for lithography innovation as well as challenges remain. Progress in optical lithography equipment and optical mask-less tools enable improved efficiency and throughput, and more flexible use cases, respectively. Success in HVM and further extension of EUV lithography depend on advances in exposure tools stability, throughput, defectivity, imaging and overlay. Innovation in photomasks technology and tooling is a key component to both optical and EUV extendibility, as well as for continued support of a growing demand of established processes. Process optimization and stochastics control dictate implementation schemes of multiple patterning and EUV.

The new Optical and EUV Nanolithography XXXV conference covers both EUV and Optical projection-based lithography systems, practices, and their applications in IC technology. It is the leading forum for scientists and engineers from around the world to present and discuss research on the advancement of lithography technologies.

We welcome technical and scientific papers in the following areas:

LITHOGRAPHY EQUIPMENT
- optical lithography equipment
- optical mask-less exposure tools
- optical and EUV tool design and innovation
- high-NA EUV imaging systems
- throughput, defectivity, and productivity
- imaging performance
- focus, dose, overlay control, and budgets
- aberrations, flare, and out-of-band light

SOURCES
- light sources for EUV and optical lithography systems
- power scaling of EUV sources
- efficiency and reliability
- source characterization
- EUV source collectors, cleaning, and lifetime

MASKS
- substrates and blanks
- patterned and blank mask inspection
- actinic, e-beam, and DUV inspection methods
- defect characterization, mitigation, and repair
- optical and EUV mask absorber materials and patterning
- mask process
- mask roughness
- pellicle development and platform integration
- mask architectures for higher numerical apertures
- mask writing techniques
- mask design fit to multi-beam mask writers

Continued

Optical and EUV Nanolithography XXXV (AL101) continued

PATTERNING

- optical system and mask-induced defect, electrical and yield signatures
- resolution enhancement techniques
- imaging simulations and source-mask optimization (SMO)
- optical and EUV lithography mixing
- EUV to Optical matching
- multi-patterning, 193i and EUVL
- edge placement control
- on-product overlay control
- EUV process optimization
- stochastics control

SYSTEMS FOR IOT, ADVANCED PACKAGING, AND HETEROGENEOUS INTEGRATION

- Equipment design and characterization for non-IC applications
- Light sources for non-IC applications
- Mask technology for non-IC applications

Students submitting papers to Optical and EUV Nanolithography XXXV will be considered for the ASML Best Student Paper. This award is given each year at this conference and recognizes extraordinary work achieved by students interested in the photolithography field, and strongly supports the contributions made to scientific advancement at the conference. The award includes a plaque along with a monetary award to help the student's future research activities.

DTCO and Computational Patterning (AL102)

Conference Chair: **Ryoung-Han Kim,** IMEC (Belgium)

Conference Co-Chair: **Neal V. Lafferty,** Mentor, a Siemens Business (USA)

Program Committee: **Jason P. Cain,** Advanced Micro Devices, Inc. (USA); **Lifu Chang,** MOSIS Integrated Circuit Fabrication Service (USA); **Dan J. Dechene,** IBM Thomas J. Watson Research Ctr. (USA); **Yuri Granik,** Siemens Industry Software Inc. (USA); **Harsha Grunes,** Intel Corp. (USA); **Srividya Jayaram,** Mentor, a Siemens Business (USA); **Sungwoo Ko,** SK Hynix, Inc. (Korea, Republic of); **Sachiko Kobayashi,** KIOXIA Corp. (Japan); **Kafai Lai,** The Univ. of Hong Kong (USA); **Ya-Chieh Lai,** Cadence Design Systems, Inc. (USA); **Lars W. Liebmann,** TEL Technology Ctr., America, LLC (USA); **Kevin Lucas,** Synopsys, Inc. (USA); **Larry Melvin,** Intel Corp. (USA); **Shigeki Nojima,** KIOXIA Corp. (Japan); **David Z. Pan,** The Univ. of Texas at Austin (USA); **Piyush Pathak,** Cadence Design Systems, Inc. (USA); **Michael L. Rieger,** Consultant (USA); **Vivek K. Singh,** Intel Corp. (USA); **Kunal N. Taravade,** Synopsys, Inc. (USA); **Chun-Ming Wang,** Western Digital (USA); **Lynn T. Wang,** GLOBALFOUNDRIES Inc. (USA); **Yayi Wei,** Institute of Microelectronics, Chinese Academy of Sciences (USA); **Chi-Min Yuan,** NXP Semiconductors (USA)

Design Technology Co-Optimization (DTCO) is the process to co-optimize the design and technology (i.e., manufacturing process and electronic design automation) to improve chip power, performance, area, and cost (PPAC) as the manufacturing process constraints continue to be an important consideration in semiconductor technology node definition, ramp, and scale manufacturing. Design for Manufacturability (DFM), Design for Yield (DFY), and computational patterning are used to improve the manufacturability, while reducing the error and cost during the design phase.

In past years, this conference has covered the topics of design interactions with computational patterning (e.g., OPC), lithography/etch processes, fill, CMP, and other integration process. Cost-of-ownership (CoO), yield, and reliability-related topics have been covered as well. This year's conference will also include broad computational patterning topics in areas of both Optical and EUV lithography. Like last year, papers should emphasize fundamentals of technical solutions rather than their commercial embodiments.

Topics of interest include, but are not limited to:

DESIGN TECHNOLOGY CO-OPTIMIZATION (DTCO) AND SYSTEM TECHNOLOGY CO-OPTIMIZATION (STCO)

- pattern-based design optimization
  - leveraging design-intent information (beyond layout) for manufacturing
  - propagating electrical design intent for RET/OPC and manufacturing optimization and verification
  - performance-power-manufacturability optimization
  - design for multi-patterning (MP) technology
  - layout style and lithography co-optimization (including optical source and design co-optimization)
  - standard cell, SRAM, and digital designs
  - design and technology booster co-optimization
  - design for novel patterning process
    - directed self-assembly (DSA) technology
    - interferometric lithography
    - novel subtractive and additive patterning techniques
- design optimization for technology
  - DTCO for Standard Cells and Memory
  - DTCO for Device and Integration
  - DTCO for tools
- STCO 3-D integration
  - 3-D packaging and integration
  - heterogeneous integration and its impact to design, DFM, OPC, and other fields
- design-to-manufacturing economics
  - cost-performance tradeoffs between design and manufacturing
  - design-to-manufacturing flow methodologies for productivity improvement, time-to-market, and cost reduction
  - new models for maximizing net return on investment in design and manufacturing.

DESIGN FOR MANUFACTURING (DFM), DESIGN FOR YIELD (DFY): TECHNOLOGY, IP, AND SYSTEM

- physical layout optimization
  - Design-rule development strategies and methodologies
  - layout optimization for systematic and random yield loss reduction
  - layout optimization for minimizing circuit variability
- design and verification methodologies using novel manufacturing models
  - design verification
  - hot spot detection
- manufacturing friendly circuit design styles and methodologies
- DFM for "more than Moore" applications (analog, RF, digital/SoC, etc.)
- deep learning and machine learning; data analytics for layout analysis and optimization or process modeling and control
- design-to-manufacturing methodologies for analog circuits, MEMS, and other microlithography applications

Continued

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DTCO and Computational Patterning (AL102) continued

COMPUTATIONAL PATTERNING (EUV & DUV)

- optimization and machine learning/AI approaches throughout mask manufacturing, SMO, OPC, etch, etc.
- new computational lithography consideration for anamorphic high-NA EUV, including stitching impacts on design and DTCO applications for mitigation
- new approaches for multi-patterning, decomposition, and interaction with design
- advances in modeling for accuracy and defect detection, including use in DTCO
- applications of new computation architectures such as quantum computing, TPU, etc.

DEEP LEARNING AND MACHINE LEARNING TECHNIQUES INTO DESIGN, LAYOUT OPTIMIZATION, AND COMPUTATIONAL PATTERNING

- machine learning based process, mask, design, and OPC methodologies & optimization

Special consideration will be given to papers that emphasize methodologies or applications used by chip manufacturers. Abstracts with a preview of results and conclusions supported by technical data are favored for oral presentation.

Metrology, Inspection, and Process Control XXXVI (AL103)

Conference Chair: **John C. Robinson,** KLA Corp. (USA)

Conference Co-Chair: **Matthew J. Sendelbach,** TEL Technology Ctr., America, LLC (USA)

Program Committee: **Ofer Adan,** Applied Materials Israel, Ltd. (Israel); **John A. Allgair,** BRIDG (USA); **Masafumi Asano,** Tokyo Electron Ltd. (Japan); **Bryan M. Barnes,** National Institute of Standards and Technology (USA); **Annalisa Bordogna,** STMicroelectronics SRL (Italy); **Cornel Bozdog,** Micron Technology, Inc. (USA); **Benjamin D. Bunday,** AMAG Consulting, LLC (USA); **Xiaomeng Chen,** Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); **Hugo Cramer,** ASML Netherlands B.V. (Netherlands); **Timothy F. Crimmins,** Intel Corp. (USA); **Shunsuke Koshihara,** Hitachi High-Technologies Corp. (Japan); **Yi-Sha Ku,** Industrial Technology Research Institute (Taiwan); **Byoung-Ho Lee,** SK hynix, Inc. (Korea, Republic of); **Myungjun Lee,** SAMSUNG Electronics Co., Ltd. (Korea, Republic of); **Philippe Leray,** IMEC (Belgium); **Narender Rana,** Western Digital Corp. (USA); **Christopher J. Raymond,** Onto Innovation Inc. (USA); **Daniel Schmidt,** IBM Thomas J. Watson Research Ctr. (USA); **Nivea G. Schuch,** ASELTA Nanographics (France); **Eric Solecky,** GLOBALFOUNDRIES Inc. (USA); **Alexander Starikov,** I&I Consulting (USA); **Alok Vaid,** GLOBALFOUNDRIES Inc. (USA)

Metrology-based analysis, identification, and control of error sources continue to enable rapid evolution of lithography and patterning. Metrology of exposure dose and focus supports ever-smaller process windows. Dimensional metrology in layouts facilitates resolution enhancement and validation of control. Extremely tight overlay is required for multiple patterning. Development of materials, equipment, and processing in EUV, direct-write, nanoimprint, directed self-assembly, etch, and deposition drive further innovation of metrology tools and applications.

This conference is the leading forum for the exchange of foundational information and discussion of novel concepts in patterning-related metrology, inspection, and process control. Consistent with the conference charter and goals, please submit original technical papers in these and related technology areas:

METROLOGY AND INSPECTION

- optical full-field and scanned microscopy, scatterometry, and interference microscopy
- novel measurement techniques with high-resolution optics, scatterometry, SEM, AFM, x-ray
- particle-beam scanned microscopy, materials characterization, and elemental analysis
- design rules, design compliance, hot spots, design-based metrology and inspection
- metrology for design rules and process margins, budgeting, and budget control
- metrology for lithography development, patterning model build, and validation
- metrology on photomasks, including pre-compensation, OPC, and phase shifting
- machine learning in metrology and inspection for capability and productivity
- hybrid metrology, including computational or virtual metrology
- parametric electrical testing and other device performance-based metrology
- applications in emerging patterning technologies including optical immersion and EUV lithography, direct-write, nano-imprint, and directed self-assembly
- applications in manufacturing of ICs, cell stacking, wafer bonding, TSV and 3D integration, displays, thin-film heads, MEMS, MOEMS, bio-arrays, lab on a chip, integrated optoelectronics and other micro- and nano-systems

CRITICAL DIMENSION, PATTERN PLACEMENT, AND OVERLAY

- 1D, 2D, and 3D metrology of CD and pattern placement, including within device layouts
- alignment, registration and overlay metrology, processing and metrology integration
- feature edge, edge profile and edge position, roughness of edge, width, and centerline
- optical, SEM, and AFM based in-die overlay on small targets and devices

MEASUREMENT SYSTEM MODELING AND SIMULATION

- physics and mathematical models of metrology process and detection methods
- physical characterization of both systems and samples, model parameters
- data analysis methods, library-based image analysis, and algorithms

CALIBRATION AND ACCURACY

- metrology quality, error diagnostics, and data culling
- measurement resolution and error, including precision and accuracy
- standards and reference materials, calibration methods, hybrid metrologies
- reference measurement systems and metrology comparisons
- tool fleet performance, maintenance, and matching

Continued

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Metrology, Inspection, and Process Control XXXVI (AL103) continued

PROCESS CHARACTERIZATION, CONTROL, PERFORMANCE, AND YIELD

- process metrology and monitors, segmentation, and reduction of variance
- metrology sampling, excursion detection, costs, device performance, and yield
- data analysis and visualization, modeling and fingerprint detection
- advanced process control, data feedback, and feed forward
- big data analysis and diagnostic methodologies, data management

DEFECT DETECTION, ANALYSIS, AND CONTROL

- detection and control of systematic, random, and low photon count stochastic pattern defects
- defect review, defect reduction, yield improvement, and effective data use
- artificial intelligence and machine learning applied to defect detection, analysis, and control
- environmental contamination, including impacts on processing and defects

PERFORMANCE LIMITS IN METROLOGY AND INSPECTION

- responses to commanded skews and cross-technology comparisons
- models of tool-sample interaction, noise, and error mechanisms

THE DIANA NYYSSONEN MEMORIAL BEST PAPER AWARD

The Diana Nyyssonen Memorial Best Paper Award for the best paper of the Conference on Metrology, Inspection, and Process Control recognizes the most significant current contribution to the field, based on the technical merit and persuasiveness of the oral presentation, as well as on the overall quality of the paper published in conference proceedings. The Diana Nyyssonen Memorial Award consists of an SPIE citation and an honorarium.

Award Sponsored by

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THE KAREL URBÁNEK BEST STUDENT PAPER AWARD

The Karel Urbánek Best Student Paper Award recognizes the most promising contribution to the field by a student, based on the technical merit and persuasiveness of the paper presentation at the conference. The Karel Urbánek Best Student Paper Award consists of an SPIE citation and an honorarium.

To be eligible, the leading author and presenter of the paper must be a student. To establish eligibility, the principal author's bio submitted with the abstract must state the academic status and the institution, as well as the advisor's name and contact information.

Award Sponsored by

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THE VLADIMIR UKRAINTSEV AWARD FOR COLLABORATIONS IN METROLOGY

The newly established Vladimir Ukraintsev Award for Collaborations in Metrology recognizes the most significant publication on inter-disciplinary explorations of metrology accuracy, round robin studies, dissemination of best-known methods, and other industry collaborations. The recipient will be determined by the Metrology, Inspection, and Process Control program committee based on the recipient's potential to influence the industry by his or her oral or poster presentation and conference proceedings paper. The Vladimir Ukraintsev Award for Collaborations in Metrology, when awarded, will be presented at the subsequent year's conference.

Award Sponsored by

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SAVE THE DATE

Abstracts Due:
1 September 2021

Author Notification:
6 December 2021

The contact author will be notified of acceptance by email.

Manuscript Due Date:
2 February 2022

PLEASE NOTE: Submission implies the intent of at least one author to register, attend the conference, present the paper as scheduled, and submit a full-length manuscript for publication in the conference proceedings.

Novel Patterning Technologies 2022 (AL104)

Conference Chair: **Eric M. Panning,** Intel Corp. (USA)

Conference Co-Chair: **J. Alexander Liddle,** National Institute of Standards and Technology (USA)

Program Committee: **Alan D. Brodie,** KLA Corp. (USA); **Tito L. Busani,** The Univ. of New Mexico (USA); **Richard A. Farrell,** Facebook Inc. (USA); **Naoya Hayashi,** Dai Nippon Printing Co., Ltd. (Japan); **Daniel J. C. Herr,** The Univ. of North Carolina at Greensboro (USA); **Tatsuhiko Higashiki,** KIOXIA Corp. (Japan); **Erik R. Hosler,** PsiQuantum Corp. (USA); **Stephen M. Kuebler,** Univ. of Central Florida (USA); **Chi-Chun Liu,** IBM Corp. (USA); **Hans Loeschner,** IMS Nanofabrication GmbH (Austria); **John G. Maltabes,** Applied Materials GmbH & Co. KG (USA); **Laurent Pain,** CEA-LETI (France); **Ivo W. Rangelow,** Technische Univ. Ilmenau (Germany); **Douglas J. Resnick,** Canon Nanotechnologies, Inc. (USA); **Ricardo Ruiz,** Lawrence Berkeley National Lab. (USA); **Martha I. Sanchez,** LytEn, Inc. (USA); **Chandrasekhar Sarma,** Intel Corp. (USA); **Gurpreet Singh,** Intel Corp. (USA); **Seung Chul Song,** Qualcomm (USA); **Ines A. Stolberg,** Vistec Electron Beam GmbH (Germany); **Hsinyu Tsai,** IBM Research - Almaden (USA); **Wei Wu,** The Univ. of Southern California (USA)

New solutions to meet current and future patterning challenges are critical to extend scaling, complement existing approaches, and enable functional patterning for emerging and convergent applications, e.g., More-than-Moore. The Novel Patterning conference brings together expertise from a diverse group of industry/academia leaders within and outside the semiconductor field. This conference is an opportunity to present new ideas as well as learn more about the core challenges in advanced patterning.

The Novel Patterning conference showcases novel lithography and patterning techniques that provide solutions for semiconductor IC nodes, wafer-level packaging, and non-IC related and adjacent technologies, e.g., health care, communications, energy, etc., such as MEMS/NEMS, MOEMS, displays, photonics, metamaterials, and micro/nanofluidics. Approaches, including roll-to-roll, 3D printing, DNA-based and colloidal self-assembly, and additive manufacturing, are welcome. Contributions are also sought which describe hybrid approaches employing a combination of lithographic aerial imaging and patterning processes such as self-aligned pitch division, tone-reversals, selective depositions, directed self-assembly, including novel approaches that demonstrate the feasibility of the bio-inspired assembly of functional nanomaterials, etc.

APPLICATION AREAS FOR NOVEL PATTERNING TECHNOLOGIES

- functional nanopatterning materials and emerging IoT applications
- novel patterning for semiconductor 7nm IC nodes and beyond
- MEMS/NEMS, MOEMS, and microsystems
- metasurfaces and metamaterials
- photonic and/or phononic crystals
- micro/nanofluidics, lab on a chip or other bio-applications
- digital micro-mirror arrays
- multi-beam writing of masks and master templates
- semiconductor wafer-level packaging and fan-out
- bioelectronics and genomics/proteomics
- photovoltaics and related energy applications
- large-area display/flat-panel displays
- roll-to-roll/web format device manufacturing
- micro LED array fabrication
- nanopatterned sensors, waveguides, antennas
- building blocks for defect-tolerant computing
- smart resists and self-healing materials
- tools/materials to improve existing scanner performance
- quantum computing devices and qubit-technologies
- 3D integration and materials
- neuromorphic and emerging memory patterning
- atomistic nanoelectronic devices.

TECHNOLOGY AREAS FOR NOVEL PATTERNING APPLICATIONS

DIRECT WRITE OR MASKLESS LITHOGRAPHY AND PATTERNING TECHNOLOGIES

- electron or ion charged-particle beams
- optical beams
- STED, multi-color/multi-photon direct write
- resistless e-beam or ion beam direct patterning
- beam-directed nucleation, ion-beam deposition
- material ablation or material transformation reactions
- ink-jet
- scanning probe lithography, dip-pen printing, tip-based patterning
- interference, plasmonic or nearfield/evanescent wave lithography
- micromirror optical lithography
- 3D metal or ceramic sintering.

PROCESS-BASED LITHOGRAPHY AND PATTERNING

- directed self-assembly
- nanoimprint lithography
- selective deposition
- self-aligned or pitch division process integration techniques
- colloidal self-assembly and DNA patterning
- 3D patterning

In the spirit of facilitating exchange of knowledge, we strongly encourage contributions that provide a background to the technology, details on latest results and a clear indication of the limitations/opportunities for future development.

Submit your abstract today: **spie.org/al22call**

Advances in Patterning Materials and Processes XXXIV (AL105)

Conference Chair: **Daniel P. Sanders,** IBM Research - Almaden (USA)

Conference Co-Chair: **Douglas Guerrero,** Brewer Science, Inc. (USA)

Program Committee: **Gilles R. Amblard,** SAMSUNG Austin Semiconductor LLC (USA); **Ramakrishnan Ayothi,** JSR Micro, Inc. (USA); **Robert L. Brainard,** SUNY Polytechnic Institute (USA); **Ryan Callahan,** FUJIFILM Electronic Materials U.S.A., Inc. (USA); **James F. Cameron,** DuPont Electronics & Imaging (USA); **Sonia Castellanos Ortega,** Inpria (USA); **Joy Y. Cheng,** Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); **Ralph R. Dammel,** EMD Performance Materials Corp. (USA); **Anuja De Silva,** Lam Research Corp. (USA); **Danilo De Simone,** IMEC (Belgium); **Roel Gronheid,** KLA-Tencor/ ICOS Belgium (Belgium); **Masahiko Harumoto,** SCREEN Semiconductor Solutions Co., Ltd. (Japan); **Clifford L. Henderson,** Univ. of South Florida (USA); **Craig D. Higgins,** GLOBALFOUNDRIES Inc. (USA); **Christoph K. Hohle,** Fraunhofer-Institut für Photonische Mikrosysteme (Germany); **Scott W. Jessen,** Texas Instruments Inc. (USA); **Jing Jiang,** Applied Materials, Inc. (USA); **Yoshio Kawai,** Shin-Etsu Chemical Co., Ltd. (Japan); **Qinghuang Lin,** Lam Research Corp. (USA); **Nobuyuki N. Matsuzawa,** Panasonic Corp. (Japan); **Warren Montgomery,** Irresistible Materials Ltd. (USA); **Mark H. Somervell,** Tokyo Electron America, Inc. (USA); **Jason K. Stowers,** Inpria Corp. (USA); **Raluca Tiron,** CEA-LETI (France); **Rick Uchida,** Tokyo Ohka Kogyo America, Inc. (USA); **Thomas I. Wallow,** ASML Brion Technologies (USA); **Rudy J. Wojtecki,** IBM Research - Almaden (USA); **Aiwen Wu,** Entegris, Inc. (USA)

The Advances in Patterning Materials and Processes conference is the leading forum for scientists and engineers from institutes, material as well as equipment vendors, and end-users around the world to present and discuss research on the chemistry, physics, and performance of photoresists as well as other patterning materials and processes. Evolutionary and ultimately revolutionary innovations will continue to be required in resist materials and patterning processes in order to achieve the combination of resolution, edge roughness, and sensitivity required for future technology nodes. This conference welcomes submissions of original papers that emphasize recent advances in high-performance patterning processes and materials and their integration in established, maturing, emerging, and new lithographic technologies.

Original technical papers are solicited, but not limited to the following topics:

PATTERNING MATERIALS, PROCESSES, AND APPLICATIONS

- photoresists for EUV and 193nm (immersion) lithography
- photoresists for other wavelengths: electron beam or other maskless lithography, 248nm, i-line, and g-line
- novel development techniques: positive and negative tone (PTD, NTD) resists and developers, solvent, aqueous, or dry development processes
- multi-layer patterning materials: underlayers for reflection control, planarization, pattern transfer, and process enhancement
- selective deposition and surface modification of organic and inorganic materials: chemistry, processing, and materials science, bottom up approaches
- self-assembling materials (DSA): chemistry and materials science, processing, and ancillary materials
- materials and processes used in vertical integration of novel devices, stacked structures, nanosheets, nanotubes, solvent based or dry processes
- materials for packaging and SOC/SIP integration

PROCESSING AND PROCESS CONTROL

- single and multiple patterning
- resist smoothing, rectification, trim and shrink, and tone inversion
- applied processing, including filtration, defect control, and pattern collapse mitigation
- materials challenges related to etch, process control, and metrology
- new processing techniques and applications, especially self-aligned and additive strategies

SIMULATION AND MODELING

- resist fundamentals and assessment of patterning and materials scaling limits
- variability, stochastics, and defectivity
- design for or simulation of new processes and applications
- AI and ML approaches to materials design, characterization, patterning, and process control

Consistent with the conference's charter and goals, authors are required to provide a description of chemical and physical principles as well as sufficient chemical structural detail in presented work. Submissions which do not reveal sufficient chemical details so as to add value to the readers or are principally of a commercial nature may not be accepted for presentation and publication.

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AWARDS

Each year the SPIE Patterning Materials and Processes Conference recognizes the outstanding oral, poster, and student submissions from the prior year's conference via three distinguished awards:

C. GRANT WILLSON BEST PAPER AWARD IN PATTERNING MATERIALS AND PROCESSES

The C. Grant Willson Best Paper Award in Patterning Materials and Processes recognizes the best oral paper presented the previous year. Candidate papers are nominated and selected by the SPIE Patterning Materials conference committee. Judging criteria include the technical originality, completeness, relevance, quality of oral presentation, and quality of proceedings manuscript. Invited keynote talks are not eligible. The award consists of a certificate and a cash honorarium ($1,000).

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JEFFREY BYERS BEST POSTER AWARD IN PATTERNING MATERIALS AND PROCESSES

The Jeffrey Byers Best Poster Award in Patterning Materials and Processes recognizes the best poster presented the previous year. Candidate posters are nominated and selected by the SPIE Patterning Materials conference committee. Judging criteria include the technical originality, completeness, relevance, quality of poster presentation, and quality of proceedings manuscript. The award consists of a certificate and a cash honorarium ($750).

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The Hiroshi Ito Student Award in Patterning Materials and Processes recognizes the best student paper presented the previous year. Candidate papers are nominated and selected by the SPIE Patterning Materials conference committee. To be eligible, the primary and presenting author must be a student or post-doc at the time of the conference. Judging criteria include the technical originality, completeness, relevance, quality of presentation, and quality of proceedings manuscript. Both oral and poster submissions are eligible; however, the award will not be given to a submission that is a concurrent winner of the Willson or Byers Awards. The award consists of a certificate and a cash honorarium ($1,000).

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Abstracts Due:
1 September 2021

Author Notification:
6 December 2021

The contact author will be notified of acceptance by email.

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2 February 2022

PLEASE NOTE: Submission implies the intent of at least one author to register, attend the conference, present the paper as scheduled, and submit a full-length manuscript for publication in the conference proceedings.

Advanced Etch Technology and Process Integration for Nanopatterning XI (AL106)

Conference Chair: **Julie Bannister,** Tokyo Electron America, Inc. (USA)

Conference Co-Chair: **Nihar Mohanty,** Oculus VR, LLC (USA)

Program Committee: **Catherine B. Labelle,** Intel Corp. (USA); **Efrain Altamirano-Sánchez,** IMEC (Belgium); **John Arnold,** IBM Thomas J. Watson Research Ctr. (USA); **Keun Hee Bai,** SAMSUNG Electronics Co., Ltd. (Korea, Republic of); **Maxime Darnon,** LN2 CNRS (Canada); **Sebastian U. Engelmann,** IBM Thomas J. Watson Research Ctr. (USA); **Eric A. Hudson,** Lam Research Corp. (USA); **Kaushik A. Kumar,** Tokyo Electron Ltd. (Japan); **Qinghuang Lin,** IBM Thomas J. Watson Research Ctr. (USA); **Ru-Gun Liu,** Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); **Jake O'Gorman,** Hitachi High Technologies America, Inc. (USA); **Erwine Pargon,** CNRS/LTM (France); **Nicolas Posseme,** CEA-LETI (France); **Ricardo Ruiz,** Lawrence Berkeley National Lab. (USA); **Yuyang Sun,** Mentor Graphics Corp. (USA); **Richard S. Wise,** Lam Research Corp. (USA); **Anthony Yen,** ASML US, LP (USA); **Ying Zhang,** NAURA (USA)

The revolution in microelectronics over the last 50 years of Moore's Law has been led by exponential increases in dimensional scaling of logic and memory semiconductor devices. Dramatic innovations in optical and now extreme ultraviolet lithography in conjunction with novel process integration strategies have been the driving force behind much of the success of dimensional scaling. Plasma-based pattern transfer innovations have formed a major backbone for those integration strategies that in collaboration with wavelength and numerical aperture scaling have avoided the physical limits as defined by the Rayleigh criterion.

This new paradigm in scaling defines the patterning era, utilizing innovative plasma processing techniques and novel process integration to dramatically extend the achievable pattern design, dimension and fidelity. Plasma-based processes including both etch and deposition are key to an overall patterning strategy to create new opportunities in "complementary patterning" for the basic elements common to all patterns (lines, spaces, holes). Novel integration strategies take the basic elements to next level by enabling more complex structures with high fidelity.

This increasing interdependence of lithography technologies, photoresist technologies, plasma etch, and deposition technologies has created new opportunities in materials, integration, and the co-optimization of plasma-based patterning with lithography and process control. Historically distinct from optical imaging, the new role of these plasma-based techniques and process integration in defining critical features on device has driven a need for more intelligent process control and automated development.

ORIGINAL AND OVERVIEW TECHNICAL PAPERS ARE SOLICITED ON, BUT NOT LIMITED TO, THE FOLLOWING TOPICS:

- novel developments in plasma-based patterning techniques: EUV-based patterning, self-aligned spacer techniques (SAxP and mandrel/spacer design), optical lithography patterning, complementary patterning and optical/EUV tradeoffs, self-aligned structures, on product overlay, edge placement error mitigation strategies, and cost modeling of the proposed patterning schemes
- novel discoveries of plasma-material interactions: plasma-photoresist interactions, LER/LWR/stochastics mitigation, MOL/BEOL (low-k) material interactions, novel substrate material handling (SiGe, III-V, C, nonvolatile memory) etc.
- etch challenges for 3D memory and logic architectures
- defect reduction or yield enhancement techniques by dry or wet process solutions
- new etch methodologies and their application to patterning processes, e.g.: atomic layer etching (ALE), low Te processing, high aspect ratio pattern definition, selective deposition
- patterning control through advanced process solutions: in-situ process control, process simulations, etch-aware OPC, edge place error (EPE) etc.
- machine-learning-based methodologies for process or equipment development for patterning
- novel integration strategies for pattern fidelity improvement, new design enablement, etc.
- advanced patterning, process, and selective deposition tools and processes for novel etch-pattern transfer applications
- applications of novel patterning transfer techniques to improve mask variability
- novel holistic (litho, etch, and deposition) patterning solutions for logic and memory applications
- advanced patterning solutions for emerging product applications including but not limited to: AR/VR, neuromorphic computing, quantum computing, power semiconductors (GaN, others), IoT devices, photonic devices, MEMS, MOEMS, other "more than Moore devices" and derivative technologies (RF, analog or mixed signal)

Special consideration will be given to papers that emphasize issues which are cross-disciplinary in nature.

Abstracts with a preview of results and conclusions supported by technical data are favored for oral presentation.

TECHNICAL PROGRAM Available November 2021

The comprehensive advance technical program will list conferences, paper titles, and authors in order of presentation. The program will outline of all planned special events and hotel and registration information.

REGISTRATION

All participants, including invited speakers, contributed speakers, session chairs, co-chairs, and committee members must pay a registration fee.

Fee information for conferences, courses, a registration form, and technical and general information will be available on the SPIE website in November 2021.

HOTELS

Opening of the hotel reservation process for Advanced Lithography is scheduled for November 2021. SPIE will arrange special discounted hotel rates for attendees that will be available when housing opens. Please do not call SPIE for information. The SPIE website will be kept current with any updates.

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If government and/or company clearance is required to present and publish your presentation, start the process now to ensure that you receive clearance if your paper is accepted.

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Find important requirements for visiting the USA on the SPIE Advanced Lithography + Patterning website. There are new steps that ALL visitors to the USA need to follow. Online at: spie.org/visa

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- 100-word summary for the program
- Keywords used in search for your paper (optional)
- Some conferences may indicate additional requirements in the call for papers

Note: Only original material should be submitted. Commercial papers, papers with no new research/development content, and papers with proprietary restrictions will not be accepted for presentation.

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- Final placement in an oral or poster session is subject to Chair discretion.

Contact information

For questions about submitting an abstract, or the meeting, contact the Contact the Program Coordinator. For questions about your manuscript, contact **AuthorHelp@spie.org.**

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1 September 2021

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6 December 2021
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SPIE International Headquarters
PO Box 10
Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290 / Fax: +1 360 647 1445
help@spie.org / www.SPIE.org

SPIE Europe Office
2 Alexandra Gate
Ffordd Pengam, Cardiff, CF24 2SA UK
Tel: +44 29 2089 4747 / Fax: +44 29 2089 4750
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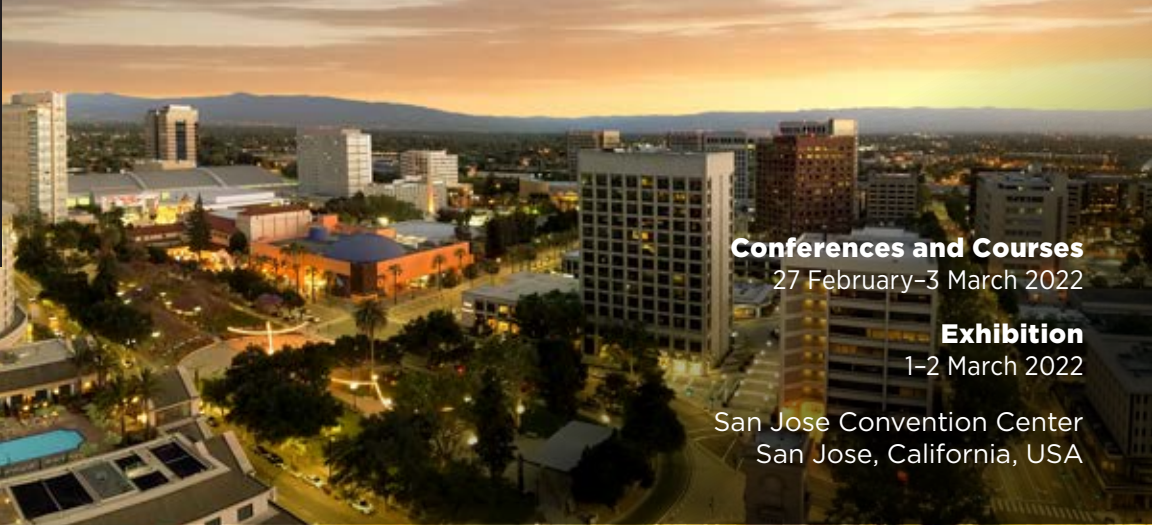

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