Advanced Lithography 2020

Technologies for lithography R&D, devices, tools, fabrication, and services.

Conferences and Courses: 23–27 February 2020
Exhibition: 25–26 February 2020
San Jose, California, USA

CUTTING-EDGE RESEARCH
WORLD-CLASS SPEAKERS
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FOCUSED TECHNICAL TOPICS

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SPIE is the international society for optics and photonics, an educational not-for-profit organization founded in 1955 to advance light-based science, engineering, and technology. The Society serves nearly 264,000 constituents from 166 countries, offering conferences and their published proceedings, continuing education, books, journals, and the SPIE Digital Library in support of interdisciplinary information exchange, professional networking, and patent precedent. SPIE provided more than $4 million in support of education and outreach programs in 2019.
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Gain knowledge from the experts and apply it directly to your daily work.

- Learn from the best. This is your opportunity for direct instruction from legends in the semi/litho industry, many of whom are pioneers in their fields
- Course topics are aligned with current industry needs and trends
- Earn CEUs for professional continuing education requirements

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Information for Course attendees:
www.spie.org/education/course-attendees

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SPIE is accredited by the International Association for Continuing Education and Training (IACET) and is authorized to issue the IACET CEU.

ADVANCED LITHOGRAPHY COURSES

SUNDAY 23 FEBRUARY 2020

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<thead>
<tr>
<th>Course Code</th>
<th>Course Title</th>
<th>Time</th>
<th>Member</th>
<th>Student Member</th>
<th>Non-Member</th>
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<tr>
<td>SC101</td>
<td>Introduction to Microlithography: Theory, Materials, and Processing</td>
<td>8:30 AM - 5:30 PM</td>
<td>$610</td>
<td>$322</td>
<td>$730</td>
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<tr>
<td>SC111</td>
<td>Lithography Process Control (Levinson)</td>
<td>8:30 AM - 5:30 PM</td>
<td>$655</td>
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<td>SC885</td>
<td>Principles and Practical Implementation of Multiple Patterning (Dusa, Hsu)</td>
<td>8:30 AM - 5:30 PM</td>
<td>$610</td>
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<tr>
<td>SC888</td>
<td>EUV Lithography (Bakshi, Ahn, Naulleau)</td>
<td>8:30 AM - 5:30 PM</td>
<td>$845</td>
<td>$416</td>
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<tr>
<td>SC992</td>
<td>Lithography Integration for Semiconductor FEOL &amp; BEOL Fabrication (Lin, Zhang)</td>
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<tr>
<td>SC1099</td>
<td>Chemistry and Lithography (Okoroanyanwu)</td>
<td>8:30 AM - 5:30 PM</td>
<td>$710</td>
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<td>SC1100</td>
<td>Scatterometry in Profile, Overlay and Focus Process Control (Cramer, Turovets)</td>
<td>8:30 AM - 5:30 PM</td>
<td>$345</td>
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<tr>
<td>SC1132</td>
<td>Computational Basis for Advanced Lithography Techniques (Li)</td>
<td>8:30 AM - 12:30 PM</td>
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<td>SC1133</td>
<td>Advanced concepts in Metrology Toolset Stability and Matching (Solecky, Adan)</td>
<td>8:30 AM - 12:30 PM</td>
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<td>SC1158</td>
<td>Metrology of Image Placement (Starikov)</td>
<td>8:30 AM - 5:30 PM</td>
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<td>SC1264</td>
<td>Machine Learning for Lithography (Shiely)</td>
<td>8:30 AM - 5:30 PM</td>
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<tr>
<td>SC1263</td>
<td>Stochastic Lithography (Mack, Petersen)</td>
<td>8:30 AM - 5:30 PM</td>
<td>$610</td>
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MONDAY 24 FEBRUARY 2020

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<tr>
<td>SC1030</td>
<td>Interaction of Physical Design and Lithography (Yuan)</td>
<td>1:30 PM - 5:30 PM</td>
<td>$345</td>
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THURSDAY 27 FEBRUARY 2020

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<td>SC861</td>
<td>Practical Photoresist Processing (Dammel)</td>
<td>8:30 AM - 12:30 PM</td>
<td>$345</td>
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PRICE KEY:
Member / Student Member / Non-Member
INTENDED AUDIENCE
Process engineers, technicians, scientists, and managers new to the field of microlithography, and those who want to understand the physical and chemical principles that are the basis for resist function.

INSTRUCTOR
Murrue Bowden is President of Electronic Materials & Processing (EMP) Consulting, which he founded in 2002. He has an extensive background in resist materials for microelectronic applications with over 30 years of experience in research and research management at Bell Laboratories and Bell Communications Research (Belcore) where he was associated with the development of several commercial electron-beam resists, most notably PBS. He joined Arch Chemicals in 1997 as Director of R&D for the Microelectronic Materials division and in 2003 moved to Stevens Institute of Technology in Hoboken, NJ as Director of the Executive Master’s programs in Technology Management (MSTM/EMBA) in the School of Business. He retired from Stevens in 2014 to focus on his consulting aspects. Murrae has won numerous awards for his contributions to microlithography, most recently the 2015 Photopolymer Science and Technology Outstanding Achievement Award sponsored by the Japan Society of Photopolymer Science and Technology.

Ralph Dammel has been actively involved in x-ray, e-beam, 157 nm, 193 nm, DUV, i- and g-line resist research since 1986. Beyond photoresists, his research interests include anti-reflective coatings and other performance enhancing materials, Directed Self Assembly, novel carbon materials, and other performance materials. He is currently employed as Chief Technologist for the Performance Materials Division of Merck KGaA, Darmstadt, and is based in Philadelphia, PA.

ATTENDEE TESTIMONIAL
Very informative course with a condensed, valuable information. Instructors did an amazing job to explain the dense topics in a very clear way.

Interaction of Physical Design and Lithography

SC1030
Course Level: Introductory
CEU: 0.4 $345 Members | $194 Student Members | $410 Non-Members USD
Monday 1:30 pm to 5:30 pm
This course provides attendees with a basic knowledge of physical design and its interaction with lithography. Physical design covers a sequence of steps from logic synthesis, power planning, clock tree synthesis, placement, routing, timing closure, cell library creation and technology library creation. How each step is done has an impact on circuit layout and lithographic patterning. This is especially true when multiple patterning technology began to be adopted at 20nm and below.

Based on the feedback of course attendees from previous years, we restrict the primary scope of physical design to four key topics: standard cells, placement, routing and timing closure, that are most relevant to lithographers. In this course, we will devote approximately 2/3 of the time to introducing the concept of physical design, and 1/3 of the time on its interaction with lithography. Also, the instructor will try to cover the physical design aspects relevant to the DPTCO papers to be presented in the conference later in the week.

LEARNING OUTCOMES
This course will enable you to:
• decode a chip design into basic building blocks such as logic, memory, IO, etc
• describe the basic concept of placement, routing and timing closure in the design flow, and how standard cells are inserted into a design
• explain the terminology (e.g., placement-induced litho hotspot, litho-aware routing, timing closure for multiple patterning) commonly used in the design-lithography world
• describe the basic interaction and trade-offs (e.g., large via enclosure vs routing resource) between physical design and lithography
• explain how multiple patterning affects standard cell design, placement, routing and timing closure
• interpret the presentations and literatures, related to physical design, to be presented in the conference

INTENDED AUDIENCE
This course is intended for lithography, OPC and mask engineers who want to learn physical design and its interaction with lithography. The attendees are expected to have a basic understanding (1-2yr experience) of how lithographic processing or OPC works. The attendees are not required to have prior training on physical design.

INSTRUCTOR
Chi-Min (Chi) Yuan PhD has been involved in physical design, OPC and lithography throughout his 20+ years in the industry, mostly through hands-on experiences. He obtained his PhD degree in Electrical and Computer engineering from Carnegie Mellon University. After graduation, he worked in IBM East Fishkill as a lithography engineer. He joined Motorola Austin and was assigned to SEMATECH to manage part of the phase shift mask program. Later, he led a process integration team to develop lithography processes in Motorola APRDL. He joined Precision Semiconductor Mask Corp. as a marketing director. In 2000, he joined Freescale (later acquired by NXP) Austin and led an engineering team to develop OPC technologies. Since 2007, he has been working in the areas of design enablement, physical design and design for manufacturing.

The course price includes the hand-out from the instructor.

ATTENDEE TESTIMONIAL:
Very thorough, easy to follow explanation of theory.
Chemistry and Lithography

SC1099

Course Level: Advanced
CEU: 0.7 $710 Members | $362 Student Members | $830 Non-Members USD
Sunday 8:30 am to 5:30 pm

This course, based on the next edition of the book with the same title, explores the chemical basis of advanced lithography, which in all its essential aspects is about chemical transformations that are designed to print a relief image of an object on a flat surface. The object may be a mask containing patterns of integrated circuit devices; the flat surface may be a silicon wafer coated with photo- or radiation-sensitive resist, which upon exposure and development, or imprinting (as in the case of imprint resists), is transformed into the relief image of the mask. Underlying these transformations are distinct chemical reactions that are mediated by electrons. By drawing on fundamental, theoretical and experimental studies of molecular processes in advanced lithography, we will deconstruct lithography into its essential chemical principles. We will examine and show how electrons mediate the photo- and radiation chemistry of exposure processes of resists (be they organic, organometallic, polymeric or inorganic), as well as exposure tool sources (be they mercury arc lamp, laser, electron beam, ion beam, or plasma); colloid chemistry of resist formulation and dissolution (be it for positive tone or negative tone development), wafer and mask cleaning processes; electrochemistry of mask absorber corrosion, electrostatic discharge, and electromigration; surface chemistry of wafer and mask priming, along with thin film interfacial effects; materials chemistry of resists, exposure tool optics, and masks; environmental chemistry of the exposure environment (be it water, air or vacuum), as well as of resist poisoning; process chemistry and modeling of wafer and mask making lithographic unit operations, including substrate priming, coating, exposure, pre- and post-exposure baking, development, and post-exposure stabilization processes; inorganic and organometallic chemistry of mask defect formation and repair, of mask contamination from inorganic salt (haze) crystal growth, carbon deposition and oxidation; and polymer chemistry of directed block copolymer self-assembly.

LEARNING OUTCOMES

This course will enable you to:
• explain the chemical basis of advanced lithography
• deconstruct lithography into its essential chemical principles
• describe the molecular processes in lithography
• identify and describe the chemical reactions associated with each lithographic unit operation
• describe the role of electrons in mediating the chemical transformations associated with each lithographic unit operation
• model lithographic unit operations and the overall lithographic process
• explain directed block copolymer self-assembly chemistry and the significance of Flory-Huggins parameter.

INTENDED AUDIENCE

Scientists, engineers, and technicians who wish to learn more about the chemical basis of lithography are the intended audience. To benefit most effectively from this course, participants should have completed at least a bachelor’s program in chemistry, physics or engineering.

INSTRUCTOR

Uzodinma Okoroanyanwu is research associate professor in the department of polymer science and engineering of University of Massachusetts at Amherst in U.S.A. His research interests are broadly geared toward developing printed, flexible, and wearable electronics. He is also the founder and chief executive officer of ALLNANO LLC, a research and development company that specializes in developing and commercializing printed, flexible, and wearable electronic instruments and technologies used in molecular diagnostics, as well as in energy storage and environmental monitoring. He worked previously at Advanced Micro Devices, where he spent 12 years conducting research on advanced lithography and on organic polymer memories, and at GLOBALFOUNDRIES, where he spent 4 years conducting research on advanced lithography. He has published extensively on lithography science and technology and on electronic applications of polymers. His most recent books include Molecular Theory of Lithography, Chemistry and Lithography. A holder of 37 U.S patents, he was educated at The University of Texas at Austin, from

ATTENDEE TESTIMONIAL:
Well delivered. A lot of material covered.

### Scatterometry in Profile, Overlay and Focus Process Control

**SC1100**

**Course Level:** Introductory  
**CEU:** 0.4 $345 Members | $194 Student Members | $410 Non-Members USD  
**Sunday 1:30 pm to 5:30 pm**

Scatterometry is an optical method to measure profile characteristics of repetitive features printed on a wafer. These profile characteristics are related to process control parameters for monitoring and control applications. This course explains the basic principles of scatterometry, including HW, measurements methodologies and algorithms. Multiple examples of scatterometry application for process monitoring and control in R&D and high volume semiconductor manufacturing are discussed. A primary goal of the course is to reveal the capabilities and limitations of scatterometry and the consequences for the application space. This course explains the basic principles of scatterometry and its application for process monitoring and control in high volume semiconductor manufacturing. A primary goal of the course is to reveal the capabilities and limitations of scatterometry and the consequences for the application space.

### LEARNING OUTCOMES

This course will enable you to:

- describe the principles of OCD Profile metrology, Diffraction Based Overlay and Focus
- distinguish the various hardware implementations (spectroscopic vs. angular resolved scatterometry and ellipsometry vs. reflectometry)
- summarize the different measurement methodologies (full reconstruction vs. single parameter measurement)
- explain the growing value of scatterometry in monitoring and control applications
- review recent trends in scatterometry and possible future developments

### INTENDED AUDIENCE

This course is intended for metrology, process and application engineers who (intend to) work with scatterometry tools or scatterometry based control applications in a wafer fab. Undergraduate training in engineering or science is assumed.

### INSTRUCTOR

**Hugo Cramer** has been working in the field of CD metrology and applications for over 15 years. Currently he is Senior Systems Engineer for metrology applications at ASML, The Netherlands. Hugo is member of one of the conference Program Committees of the SPIE Advanced Lithography symposium. He is (co) author of several patents and publications. Hugo Cramer studied Physics at the Technical University of Eindhoven (NL) and received his PhD in Electrical Engineering from the Technical University of Twente (NL).

**Igor Turovets** is a Senior Scientist in the CTO “path-finding” group at Nova Measuring Instruments, a leading innovator and key provider of metrology solutions for advanced process control for semiconductor manufacturing. Igor has been working in the field of semiconductor process and metrology for over 20 years, focusing on OCD applications.

ATTENDEE TESTIMONIAL:
Good! High, deep knowledge of IC fab process and metrology tech.
Lithography Process Control
SC111
Course Level: Intermediate
CEU: 0.7 | $655 Members | $40 Student Members | $775 Non-Members USD
Sunday 8:30 am to 5:30 pm
The class connects lithographic science to process control, and appropriate statistical methods useful for lithographers are introduced. Specific topics include:
- Statistical process control, focusing on aspects particular to lithography
- Efficient measurement sampling plans for achieving desired accuracy
- Cause-and-effect diagrams in the context of lithography
- Control issues specific to critical dimensions
- Control issues specific to overlay
- Control issues specific to EUV lithography
- Edge placement errors
- Yield issues specific to lithography
- Metrology for lithographic applications
- Automatic process control
- Control of operations

LEARNING OUTCOMES
This course will enable you to:
- apply statistical process control to situations in lithography
- generate optimized measurement plans
- apply cause-and-effect diagrams to situations in lithography
- control linewidths, overlay and lithography-induced defects
- identify sources of process variation specific to EUV lithography

INTENDED AUDIENCE
Lithography engineers and managers who already have a background in lithography science and need to improve skills in process control.

INSTRUCTOR
Harry Levinson has worked for nearly four decades in the field of lithography. He has published numerous articles on lithographic science, on topics ranging from thin film optical effects and metrics for imaging, to overlay and process control, and he is the author of two books, Lithography Process Control and Principles of Lithography. He holds over 70 US patents. Dr. Levinson is an SPIE Fellow, previously chaired the SPIE Publications Committee, and served on SPIE’s Board of Directors. In recognition of his contributions to SPIE, Dr. Levinson received the Society’s 2014 Directors’ Award. He has a BS in engineering from Cornell University and a PhD in physics from the University of Pennsylvania.

Material level is intermediate. Some advanced topics are introduced.

Computational Basis for Advanced Lithography Techniques
SC1132
Course Level: Intermediate
CEU: 0.4 | $345 Members | $194 Student Members | $410 Non-Members USD
Sunday 8:30 am to 12:30 pm
This course provides attendees with a definition and underling concepts of Computational Lithography, which is comprised of lithographic modeling and advanced pattern correction techniques. It is designed to build the communication of exposure tool engineers, lithography process engineers, metrology engineers and OPC/RET/SMO engineers to improve lithography process in an integrated sense. You will become familiar with the Computational Lithography framework and understand how the evolution of simple models and advanced pattern correction techniques to nowadays’ complicated yet powerful tools. An understanding of the fundamentals will allow lithographers to achieve optimum mask pattern for more robust lithography. This course will focus on both the imaging modeling and pattern correction methodology for novel patterning techniques such as Extreme UV (EUV), Directed Self-Assembly (DSA) and self-aligned multiple patterning. The unique computational features (Rigorous simulation, Mask decomposition, OPC, SMO, stochastic effect mitigation) of these novel techniques will be contrasted with traditional DUV lithography. A review of the emergence of Machine Learning based computational Lithography techniques targeted to improve efficiency for full-chip application will be given. The course concentrates on the physics and working principles, as well as methodologies, to develop the new computational infrastructure. Some basic issues in Design Technology Co-Optimization with respect to EUV, DSA etc. are also discussed.

LEARNING OUTCOMES
This course will enable you to:
- describe the framework of Computational Lithography
- describe rigorous modeling and resource-limited modeling specific to EUV, DSA and self-aligned multiple patterning
- apply imaging characteristic specific to EUV and corresponding OPC/SMO/RET requirements
- explore cost-effective lithography solutions such as DSA and its potential to provide full chip computational solution
- review status of Machine Learning application on computational lithography and VLSI design
- explain Design Technology Co-optimization issues specific to these advanced lithography techniques

INTENDED AUDIENCE
This material is intended for practicing engineers or anyone who needs to learn basic principles and how to model, simulate and apply pattern correction for better RET and process robustness. Lithography process engineers, metrology engineers, OPC engineers, and those working on computational lithography will find this course valuable. A basic understanding of photolithography technique will maximize your benefit from this course.

INSTRUCTOR
Kafai Lai Ph.D. is a Fellow of SPIE, OSA, a senior member of IEEE and a Senior Scientist in the IBM T.J. Watson Research Center. He has been involved in optical imaging modeling and lens characterization, exposure tooling analysis, OPC model improvement, and lithography/RET development. Source Mask optimization and recently Design Technology Co-Optimization in mainstream lithography, and advanced lithography techniques such as EUV and DSA, and recently on semiconductor photonics, for over 24 years. He has given numerous invited/keynotes talks and 3 different short courses at different international lithography & nano-patterning conferences. He is the overall co-chair of the SPIE Advanced Lithography Symposium 2019-2020 and the conference chair of the 2012-2015 SPIE Optical Microlithography Conference. Kafai has also been the symposium chair for the CSTIC conference in Shanghai 2009-2019. He serves as the editor for many proceedings and journals published by SPIE, OSA, ECS, IEEE, JAO. He has delivered 3 different SPIE short courses around the world during different SPIE conferences.

Advanced concepts in Metrology Toolset Stability and Matching
SC1133
Course Level: Intermediate
CEU: 0.4 | $345 Members | $194 Student Members | $410 Non-Members USD
Sunday 8:30 am to 12:30 pm
The course covers advanced concepts for metrology toolset stability and matching. It will cover many critical topics that together maximize fleet performance. This is especially important given the shift to new device architectures (finfet, 3D Flash, DRAM and advanced memory) that are challenging metrology toolsets in ways not seen before. A number of advanced concepts will be covered. Review best known methods for gauge study analysis and metrics. Appropriately setting up tool control chart limits for long term stability fleet matching based on requirements not historical data. Leveraging real time normalized product data to decrease Mean Time To Detect (MTTD) tool drifts. Recipe portability matching and monitoring to catch other issues that will affect lot cycletime. The concepts discussed are applicable to any metrology toolset such as CD-SEM, overlay, thin film, AFM, etc. and most of these concepts are also applicable to defect toolsets.

THIS PROGRAM IS CURRENT AS OF NOVEMBER 2019.
LEARNING OUTCOMES
This course will enable you to:

• identify the metrology challenges involved in development and process control of new device (finFET, 3D NAND) and advanced patterning technologies
• describe the traditional metrics and methodologies used as building blocks to assess the performance of a homogeneous and heterogeneous metrology toolset
• operate on a new and improved set of metrics and methodologies inspired from limitations in the traditional metrics and methodologies and derived from the new device and patterning challenges
• define success criteria for qualifying and ensuring long term stability of the metrology toolset
• apply these metrics and methodologies to help speed up development cycles of learning and improve process control and cycle-time in chip manufacturing
• explain the fundamental components of measurement uncertainty
• set control limits for toolset monitoring using requirements instead of historical data and leverage to drive continuous improvement
• distinguish what normalized product is and how it can be used to decrease MTTD of tool drifts
• explain and monitor the aspects of the metrology toolset than can affect the recipe performance across the fleet
• classify the fundamental aspects of cost of ownership and tradeoffs associated with fleet management

INTENDED AUDIENCE
Scientists, engineers, technicians, or managers, from academia, and patterning groups in the fab, who wish to learn more about metrology, measurement uncertainty, and process control fundamentals, and how to manage and maintain a metrology toolset. Beyond the fundamentals, new metrics and methodologies are introduced enabling metrology for upcoming inflictions of 3D FinFET and 3D flash (VNAND, TCAT, BiCS) device. Undergraduate training in engineering or science is assumed.

INSTRUCTOR
Eric Soleyck is the lead manufacturing metrology engineer at IBM. He also works on continuous improvement for numerous key fab deliverables. One of his main responsibilities improving the New Product Introduction fab business process. Eric is an active member of the metrology inspection and process control steering committee. Eric has published more than 20 papers in the field of metrology toolsets and fleet matching and holds more than a dozen and a half patents. He holds a Masters of Science in Microelectronics from Rensselaer Polytechnic Institute.

Ofer Adan is the head of patterning control and technology at Applied Materials. He also assistant chair for the Metrology, Inspection, and Process Control for Micro lithography XXXIII . Member of SPIE advanced lithography steering committee for the metrology inspection and process control conference. Recipient of 2010 Diana Nyssen memorial award from SPIE for the best paper on metrology. Ofer is an author of more than 30 papers, and several patents in the field of metrology. He holds his MSc. in electronic materials engineering from Ben Gurion University.

Stochastic Lithography
SC1263

Course Level: Intermediate
CEU: 0.7 $610 Members | $322 Student Members | $730 Non-Members USD
Sunday 8:30 am to 5:30 pm

Moore's Law has been changing the world for over 50 years, and advances in lithography have been a (the) major factor in its success. The success of lithography scaling, however, may cause the undoing of Moore's Law as smaller features become susceptible to stochastic variations such as linewidth roughness, local critical dimension uniformity, and stochastic defects. This course will look at how stochastic variation during lithography affects semiconductor devices, how to measure stochastic variations, the major causes of stochastic variation, and what stochastic will mean for the future of lithography scaling.

1. Introduction to Line-Edge Roughness (LER) and Linewidth Roughness (LWR): LER Experimental Results, Device Effects, LER Trends
5. Future Work

LEARNING OUTCOMES
This course will enable you to:

• explain the use of the power spectral density for the frequency characterization of roughness
• explain the role of noise in biasing the measurement of roughness, and the various techniques for removing this bias
• identify when the continuum model for lithography is appropriate, and when a stochastic model is required
• use the mathematics of the Poisson distribution to describe basic stochastic phenomenon such as photon and chemical concentration shot noise
• list the major sources of stochastic variation and what can be done to limit their effects

INTENDED AUDIENCE
Scientists, engineers, technicians, or managers who wish to learn more about the impact of stochastics on lithography for semiconductor manufacture. Undergraduate training in engineering or science is assumed, as is some existing familiarity with the basic practices of lithography.

INSTRUCTOR
Chris Mack developed the lithography simulation software PROLITH, and founded and ran the company FINLE Technologies for ten years. He then served as Vice President of Lithography Technology for KLA-Tencor for five years, until 2005. In 2003 he received the SEMI Award for North America for his efforts in lithography simulation and education and in 2009 he received the SPIE Frits Zernike Award for Micro lithography. He is a fellow of SPIE and IEEE and is also an adjunct faculty member at the University of Texas at Austin. In 2012 he became Editor-In-Chief of the Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3). In 2017 he cofounded Fractilia, where he now works as Chief Technical Officer developing metrology solutions for the measurement of roughness.

John Petersen is a current SPIE Fellow and a past SEMATECH Fellow with 35-years of experience in advanced lithography where he’s published more than sixty-eight papers, given numerous invited talks, taught many professional classes and holds eight patents in optical lithography and microscopy. John joined Texas Instruments in 1980, Shipley Company in 1983 and SEMATECH in 1996. In late 1998 he formed Petersen Advanced Lithography and is a co-founder of Periodic Structures where he is researching and developing the existing familiarity with the basic practices of lithography.

Machine Learning for Lithography
SC1264

Course Level: Advanced
CEU: 0.7 $655 Members | $340 Student Members | $775 Non-Members USD
Sunday 8:30 am to 5:30 pm

This course provides background on supervised learning applied to micro-lithography. A primary goal of the course is to illustrate supervised learning, inference, and validation workflow to practitioners of micro lithography, using datasets and problems with which they are familiar. Example applications will include photore sist models and inverse lithography models. Example
model types include linear classifiers, multilayer perceptrons and deep neural networks. Training methodology will utilize prepared datasets with Jupyter notebooks.

LEARNING OUTCOMES
This course will enable you to:
- define machine learning and artificial intelligence, and their distinction
- explain the supervised learning process
- articulate a machine learning problem statement for resist modeling and inverse lithography
- demonstrate how to load data into a machine learning framework
- operate TensorFlow to train a photoresist model and inverse lithography model
- utilize TensorFlow serving to make predictions with a photoresist model and inverse lithography model
- judge ML model performance, and explain bias, variance, and overfitting
- contrast the capabilities and limitations of different ML model forms
- modify ML model architectures and observe changes in outcomes

INTENDED AUDIENCE
Engineers who wish to understand how ML techniques can be adapted to achieve industry-relevant tasks. Lithographers considering the applicability of ML techniques to their domains. Managers seeking to increase familiarity with ML to assist in decision-making for future research, training or investment.

INSTRUCTOR
James Shiely has been developing machine learning tools and lithography models for nearly two decades as one of the main technologists for the Proteus tools at Synopsys. He currently holds 14 lithography-related patents, has contributed to 37 publications and is a contributor to an upcoming book about machine learning in computer-aided design. Dr. Shiely earned a Ph.D. at Duke University and is a member of SPIE and IEEE. He is currently Engineering Director at Synopsys.

2020 Changes: Course has been extended from a half-day to a full-day.
Attendees will need to bring their laptops to access a limited cloud compute infrastructure, to imitate the live Jupyter notebook session of the instructor to perform experiments.

Metrology of Image Placement
SC1158
Course Level: Introductory
CEU: 0.4 $350 Members | $196 Student Members | $415 Non-Members USD
Sunday 1:30 pm to 5:30 pm
This course explains basic principles of metrology of image placement for applications to registration, alignment, and overlay in IC manufacture. Starting with IC Design Rules, and device pattern size and placement as their basis, this course outlines a systematic approach to dimensional metrology. Device pattern variation in mask-making, lithography imaging, image recording, and image transfer, and down-stream wafer processing, are discussed leading to requirements of dimension metrology and control. Expectations in metrology of image placement are examined in the context of semiconductor design and manufacturing paradigm: device invariance in transformations of symmetry and translation, universal coordinate system, and absolute scale being the foundation of IC design. These attributes, built into IC design, are maintained in production by the use of isoplanatic lithography systems, dimensionally stable masks, stages, and wafers, control of coordinate systems and, of course, spatially uniform semiconductor processing. The key performance metrics for metrology of image placement are defined, and illustrated, in applications to improving robustness and accuracy in production environment. Systematic quantitative validation of those expectations for metrology systems and targets used, with complementary validation means and measurement technology, establish the foundation for certifiably accurate metrology of image placement and comprehensive control of overlay in IC manufacture.

LEARNING OUTCOMES
This course will enable you to:
- classify device pattern dimensions in terms of pitch, width or critical dimension (CD), centerline (CL), and layer-to-layer overlay (OL), and be able to participate in their physical definition for any process and layer as required by Design Rules (DRs) for device performance and yield
- comprehend the complementary roles of CD and CL in the yield-limiting two-layer DRs for edge-to-edge overlay (a.k.a. separation, extension, overlap, enclosure etc.)
- justify the need for DR budgeting, variance segmentation, and control of components of variance
- distinguish applications environments in metrologies of pitch, critical dimension, and placement and understand how those expectations shape the metrology tools and practices
- define data analyses required, correctable vs. residual error, be ready for hands-on data analysis
- review image- and diffraction-based approaches to metrology of image placement, expectations of metrology operability and performance, including precision, matching, and accuracy
- establish the grounds for metrology error diagnostics and data culling, symmetry and redundancy based performance metrics, being different from, for example, error of response or residual of fit
- explain the utility and the limitations of tool-induced shift (TIS) and wafer-induced shift (WIS) measurement performance metrics, mechanisms that drive them and how to reduce the impact
- become familiar with SEMI standards and terminology, technology- and company-specific measurement targets, target imaging, signal acquisition and processing, metrology applications

INTENDED AUDIENCE
Scientists, engineers, technicians, and managers in semiconductor and semiconductor equipment manufacturing who wish to learn about overlay control in IC manufacture, including technologies, issues, and methods in alignment, registration, and overlay metrology, with their expectations and applications environments, design and process interactions, integration, quality assurance, continuous improvement.

INSTRUCTOR
Alexander Starikov Independent Consultant, has been developing lithography, alignment and overlay metrology for more than two decades, first at IBM Microelectronics in Fishkill, NY and then at Ultratech Stepper and Intel Corp. on the West Coast. His innovations in rule- and model-based OPC, lithography process monitors, alignment and overlay metrology have been widely adopted, with TIS/WIS performance metrics industry standard. He earned a Ph.D. in Physics from the University of Rochester, Rochester, NY. Dr. Starikov is a Fellow Member of SPIE.

ATTENDEE TESTIMONIAL:
Alexander Starikov was very well versed in the materials. He was amazing in managing the content delivery.

Practical Photoresist Processing
SC616
Course Level: Introductory
CEU: 0.4 $345 Members | $194 Student Members | $410 Non-Members USD
Thursday 8:30 am to 12:30 pm
Photolithography is the technique underlying all integrated circuit manufacture. To a large extent, the minimum feature size and the performance of ICs is determined by the resolution achievable in this step. Also, the process yield has a strong impact on a Fab’s economy. The troubleshooting of photomask performance is therefore a key concern to every micro lithography engineer. However, this requires a highly interdisciplinary understanding of many areas, from photochemistry to polymer science to optics, that are usually not taught in a unified way in most educational curricula. In this course, photoresist processing is examined by walking the lithographic sequence, beginning with the wafer preparation and ending when the resist feature has been prepared for dry etching. Both classic near-UV DNQ/novolak resists as well as chemically amplified systems (248 and 193 nm as well as
ADVANCED LITHOGRAPHY COURSES

EUV will be covered. The chemical changes occurring in photoresists during the different process steps will be discussed. Pitfalls and tradeoffs will be pointed out at every step and correlated to the underlying properties of the photoresist materials. The aim of the course is to give micro lithography engineers a practical basis from which to begin the detective work involved in identifying the root cause of a processing problem.

LEARNING OUTCOMES
This course will enable you to:
• identify the basic chemical makeup of photoresist materials
• explain the role of the individual components in achieving overall resist performance
• solve problems in resist processing by reducing them to their chemical root cause
• weigh the performance increase of advanced processing schemes against added process complexity
• evaluate and compare different lithographic materials for their suitability-to-task

INTENDED AUDIENCE
This material is directed to engineers, scientists and managers who work with photoresist materials. Some chemical background is helpful but not required.

INSTRUCTOR
Ralph Dammel has been actively involved in x-ray, e-beam, 157 nm, 193 nm, DUV, i- and g-line resist research since 1986. Beyond photoresists, his research interests include anti-reflective coatings and other performance enhancing materials, Directed Self Assembly, novel carbon materials, and other performance materials. He is currently employed as Chief Technologist for the Performance Materials Division of Merck KGaA, Darmstadt, and is based in Philadelphia, PA.

ATTENDEE TESTIMONIAL:
Great content, super knowledgeable speaker, awesome sense of humor. Ralph Dammel

Principles and Practical Implementation of Multiple Patterning
SC885
Course Level: Intermediate
CEU: 0.7 $610 Members | $32 Student Members | $730 Non-Members USD
Sunday 8:30 am to 5:30 pm

This course provides attendees with a basic working knowledge of the fundamentals and implementation principles of what industry calls with a generic name “double patterning” but in reality it is a multi-patterning technology. This course will tackle the interdisciplinary characteristics of the multipatterning processes examining several pitch division techniques, from double to triple, quadruple or even more split steps, with focus on the key technology components, such as, but not limited to, (a) resolution and lithography options, (b) layout, ground rules and split compliance, (c) process and material, that are combined to create an electrically functional device layer from multiple patterning implementations. We will discuss single to multiple patterning pitch-split practical implementations adding complementary and combinatorial techniques based on pitch-divided gratings connected with a cut and/or a block masking layer. The course presents the lithographic and patterning alternatives of various pitch-split techniques, for example, LithoEtch, Lic and multiple SelfAligned spacer film depositions, like SAPD and SAQP. It will underline the interactions between layout style, split compliance, layer polarity, feature bias defined by split process characterics and will draw attention to the constraints to integrate the pitch-split patterning steps into a complete CMOS process flow. In addition, the course provides information on the materials and material combinations used in multiple patterning processes illustrated by relevant industry developments to increase the structural robustness of pitch divided high aspect ratio features and the anti-spacer / cut mask less approach. Special attention is given to the unique characteristics of multiple patterning metrology and process control, in particular to model overlay effects into comprehensive CDU budgets supporting the tight process tolerances of the scaling nodes. The course examines the CDU and overlay budget contributors and defines basic requirements for metrology tools performances to support multipatterning.

We will illustrate multipatterning utilization on today’s 3D transistors architecture, FinFet and Nanowires, applied on FEOE and BEOL layers, with unidirectional gratings and cuts or blocks that are needed to create the 2D layout intent. The course offers comprehensive analysis of the combinatorial multiple patterning flows, LE^n, SADP, SAQP with associated cut or block masking layers based on the new Edge Placement Error, EPE, metric, assessing pattern quality for manufacturability. Practical and useful examples from critical device layers of memory and logic devices are included throughout, with particular consideration on how multiple splits operate on device sequential layers using computational lithography optimized splits. The course includes extensive references of relevant publications on double/ multiple patterning processes.

LEARNING OUTCOMES
This course will enable you to:
• evaluate the reasons to consider multiple patterning and understand the tradeoffs
• define imaging alternatives with their associated wafer patterning processes supporting various multiple patterning options for each critical layer of a device
• learn the double-to-multiple patterning process flows and assess how, when and which split patterning technique to use and what are the primary process materials and stacking
• examine generic and representative device layouts and explain how to split bright and darkfield polarity layers
• utilize design split algorithms and their criteria to mitigate color conflicts with special attention on odd-cycle, 3-color layout conflicts
• perform computational lithography calculations on split layers to co-optimize the split solution based on entangled PV-bands, overlay and design rules
• address the challenge of implementing combinatorial multiple patterning, and break down the EPE budget and trade-off between CD and overlay tolerances
• define and use an appropriate figure of merit to evaluate the cut /block mask patterning quality
• describe primary error sources characteristics to double and multiple patterning processes
• identify the process control commonalities / differences between LE^n (n=2) and spacer defined selfaligned techniques
• infer overlay and etch contributions into a pattern control budget
• analyze process control requirements based on a spatial fingerprint of overlay and CDU distributions
• implement double/multiple patterning processes on real logic and memory devices
• apply various double/multiple patterning alternatives to support shrink roadmap

INTENDED AUDIENCE
This material is intended for anyone who needs to learn how to develop and implement double to multiple patterning techniques, including combinatorial patterning processes into an existing CMOS flow. Lithography, process and metrology-control engineers, and those who develop design rules and design circuit layout, specify mask requirements and work in process integration will find this course valuable.

INSTRUCTOR
Mircea Dusa has been involved in semiconductor technology development and advanced lithography for over 40 years. Currently, he is an IMEC Fellow, working on patterning developments through integration of atomic layer processing techniques. During his career, he worked on development of mask, lithography tools and processes, metrology and control techniques. He has been particularly active in investigating pitch split techniques implementation to meet resolution requirements beyond single exposure resolution limits. Prior to IMEC, he worked 20 years for ASML on co-optimization of exposure tools with lithographic eco-system components, and led multi patterning developments, by means of complementary and combinatorial lithography processes. Mircea is an ASML and SPIE Fellow and chaired SPIE’s Advanced Lithography Symposium and Optical Microlithography Conference. He holds 27 patents and authored over 220 papers in the field of lithography and process control.
Stephen Hsu is the imaging product engineering group lead with ASML Brion. During the course of his career, Stephen has been working on all aspects of advanced lithography development over 29 year including: overlay/alignment optimization/control strategy, stepper/scanner characterization, reticle inspection, SMORET product development. In the past 19 years, he has been working on developing resolution enhancement technique (RET) solutions including: sub-resolution assist features (SRAF), Optical Proximity Correction (OPC), and DUV/EUV Source mask optimization (SMO) and work with customers worldwide to implement these in foundries and IDM as practical low k1 patterning solutions. Presently he is focusing on sub-5 nm node imaging and patterning technology development, including using advanced SMO techniques for EUV and EUV high-NA lithography. EUV scanner matching and computational mirror heating control products. Stephen has been regularly invited by SPIE to teach the “Principles and Practical Implementation of Multiple Patterning” short course for the past 11 years. He taught the “Principle and Practical implementation of Microlithography and Resolution enhancement techniques (RET)” internal short course at multiple sites in ASML. Stephen is an ASML and SPIE Fellow. He has authored more than 120 papers in lithography, RET and holds 32 patents related to advanced lithography and resolution enhancement techniques.

EUV Lithography
SC888

Course Level: Intermediate
CEU: 0.7 $845 Members | $416 Student Members | $965 Non-Members USD
Sunday 8:30 am to 5:30 pm

This course provides attendees with a full overview of the fundamentals, current status, and technical challenges of EUV Lithography. Topics covered include EUV Sources, EUV Source Metrology, EUV Optics, EUV systems and patterning, and EUV Mask. We will begin with an overview of the history of EUVL and cover EUV sources, EUV source metrology and EUV optics. Next is a discussion of EUVL systems and patterning. We cover the fundamental components of EUV systems and address similarities and differences to optical lithography systems. This section also covers patterning issues including flare, LER, and resist performance. We continue with an exploration of EUVL Mask technology issues such as design, materials including reflective multilayers, process and metrology. Finally we conclude with a Status Review of EUVL. Course material will be drawn from the accompanying texts EUV Sources for Lithography and EUV Lithography.

LEARNING OUTCOMES
This course will enable you to:
• learn the history and basics of the development of EUV Lithography
• learn the basics of the different EUV source types and the current technical challenges of EUV source technology
• learn the fundamentals of EUV source metrology and source power measurements
• learn the fundamentals of EUV multilayer optics
• learn the fundamentals of EUV systems and patterning and understand the key components in EUV systems and the current technical challenges
• learn the fundamentals of EUV mask technology and understand the current technical challenges
• learn the current status and technical challenges of EUV Lithography for supporting high volume computer chip manufacturing

INTENDED AUDIENCE
This material is intended for anyone who is involved in the development of EUV Lithography and/or other emerging lithography techniques, needs to understand the current technology status of EUV Lithography, and is interested in learning the fundamentals of this leading patterning technology for the 32 nm node and beyond. Those who are responsible for the development of the roadmap for lithography in manufacturing and making technology decisions will find this course valuable.

INSTRUCTOR
Vivek Bakshi is the president of EUV Litho, Inc. an organization he has formed in 2007 to promote EUV Lithography via consulting, publications, education and workshops. Previously he was a Senior Member of Technical staff in the Lithography Division of SEMATECH. He has edited four books on EUV Lithography: EUV Sources for Lithography(SPIE Press, 2006), EUV Lithography (SPIE

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**LEARNING OUTCOMES**

**INSTRUCTOR**

Qinghuang Lin is Director of Technology Development Center at ASML, San Jose, California. Previously he was a Research Staff Member, a Senior Manager and an IBM Master Inventor at IBM T.J. Watson Research Center. For more than 20 years, he has held positions in photoresist development, advanced lithography, BEOL materials & integration, 3D integration and semiconductor technology trends. He has served as an associate editor of Journal of Micro/Nanolithography, MEMS and MOEMS (JMM). He has taught SPIE short courses for more than 10 years.

Ying Zhang is a vice president of Patterning Integration at Semiconductor Products Group (SPG), Applied Materials, Inc. His responsibilities include path-finding, developing and implementing next-generation plasma source, chambers, and systems for etching and key integrated solutions into high volume manufacturing at advanced technology nodes. Prior to joining Applied, Dr. Zhang was a director with TSMC where he managed plasma etching and wet clean for 28 nanometer development and ramp-up to high volume manufacturing. He previously was at IBM’s T.J. Watson Research Center and led the development of dry etch and metallization technologies for multiple advanced nodes and exploratory novel device prototyping beyond the CMOS era. Dr. Zhang received a Ph.D. in physics. He has been recognized with various corporate awards, participated in more than 40 presentations and 100 publications, and holds over 100 issued patents.

**ATTENDEE TESTIMONIAL:**

Good job! The course materials are extensive and full of details. I particularly like the good examples of integration progress. Many talented ideas.
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