Advanced Lithography 2018

CALL FOR PAPERS

Submit abstracts by 28 August 2017

25 February–1 March 2018
San Jose Marriott and San Jose Convention Center
San Jose, California

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Share your research and make an impact in the semiconductor industry

Present your work in optical lithography, metrology, or EUV. Share the latest advancements at the meeting where leaders come to network and solve lithography and patterning challenges in the semiconductor industry.

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Plan to Participate

The SPIE Advanced Lithography Symposium has been the showcase of the latest advances in lithography and patterning technology for over four decades. The 2018 symposium will cover the full spectrum of the advances and challenges in state-of-the-art lithography technology through several topical conferences. Advances in areas of nano- and micro-patterning for semiconductor IC device application will be presented in sessions devoted to optical lithography, extreme-UV (EUV) lithography, metrology/inspection, patterning materials, etch/deposition technology, and process/technology optimization. As novel patterning and non-IC lithography technologies have become more widely explored, related topics in these areas are also addressed.

The Advanced Lithography Symposium continues its role in bringing together the microlithography communities involved with semiconductor devices, micro-/nano-systems, and related fields. Participants come from a broad array of backgrounds to share and learn about state-of-the-art design, tools, materials, metrology, and process integration. Through a series of provocative panel discussions and seminars, the symposium also probes current issues being faced as we extend current methods, move toward alternative approaches, and identify new ways to complement one technology with another. The Symposium also provides the unique and primary forum for meeting and interacting with a wide range of industry experts, researchers, academics, and key players working on patterning technology development. Attendance ensures that participants learn and share the latest developments in areas of central importance to many vital technology fields.

We welcome your participation for the 2018 SPIE Advanced Lithography Symposium and urge you to submit your abstracts to the appropriate conference as described in the individual Calls for Papers, and be sure to encourage your colleagues to do the same. Relevant topics for new technology groups, keynote talks, or panel discussions are also solicited.

Symposium Chair: Bruce W. Smith
Rochester Institute of Technology (USA)

Symposium Co-Chair: Will Conley
Cymer—An ASML company (USA)

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CALL FOR PAPERS

Extreme Ultraviolet (EUV) Lithography IX (AL101)

Conference Chair: Kenneth A. Goldberg, Lawrence Berkeley National Lab. (USA)
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Program Committee: Markus Bender, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); Jos P. Benschop, ASML Netherlands B.V. (Netherlands); Robert L. Brainard, SUNY CNSE/SUNYIT (USA); Martin Burkhart, IBM Thomas J. Watson Research Ctr. (USA); Deniz Elizabeth Civay, GLOBALFOUNDRIES Inc. (USA); Daniel Corliss, IBM Corp. (USA); Yasin Ekinci, Paul Scherrer Institut (Switzerland); Allen H. Gabor, GLOBALFOUNDRIES Inc. (USA); Emily E. Gallagher, IMEC (Belgium); Florian Gstrein, Intel Corp. (USA); Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan); Eric Hendrickx, IMEC (Belgium); Soichi Inoue, Toshiba Corp. (Japan); Bryan S. Kasprzowicz, Photronics, Inc. (USA); Insung Kim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Seong-Sue Kim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Ted Liang, Intel Corp. (USA); Chang-Moon Lim, SK Hynix Inc. (Korea, Republic of); Anna Lio, Intel Corp. (USA); Lawrence S. Melvin III, Synopsis, Inc. (USA); Hiroaki Morimoto, Toppan Printing Co., Ltd. (Japan); Patrick P. Naullleau, Lawrence Berkeley National Lab. (USA); Christopher S. Ngai, Applied Materials, Inc. (USA); Shinji Okazaki, Gigaphoton Inc. (Japan); Eric M. Panning, Intel Corp. (USA); Jan Hendrik Peters, bmbg consult (Germany); Moshe E. Preil, KLA-Tencor Corp. (USA); Kurt G. Ronse, IMEC (Belgium); Tsutomu Shoki, HOYA Corp. (Japan); Akiyoshi Suzuki, Gigaphoton Inc. (Japan); Anna Chilkouleva, Lasertec U.S.A. Inc. Zweigniederlassung Deutschland (Germany); Thomas I. Wallow, ASML Brion (USA); Obert R. Wood II, GLOBALFOUNDRIES Inc. (USA)

2017 saw a coalescence of opinion among the prospects for EUV implementation as dramatic increases in EUV source power and patterning performance were achieved. In 2018, chip-makers will be focused on driving EUVL technology further toward meeting HVM productivity and yield targets for the 7-nm node, and utilizing the full design entitlement of current EUV imaging. Nevertheless, a number of critical technology challenges remain. For example: meeting productivity and performance targets for HVM; improving mask yield, inspection, review, and repair infrastructure, and weighing pupil-fill options; simultaneously improving resist resolution, sensitivity and LER, and understanding the impact of stochastics on yield. Looking beyond the 7-nm node, progress will require innovative approaches in EUV sources, for both higher power and availability, continued development of mask architecture and imaging materials, and consensus on the creation of imaging systems and masks for higher numerical apertures or magnifications. Despite decades of work, new advances in all EUV research areas demonstrate that improvements are always possible, toward the moving target of commercialization and timing.

The Extreme Ultraviolet Lithography conference continues to be the leading forum for scientists and engineers from around the world to present and discuss research on the advancement of EUV lithography technologies. This conference welcomes submissions of original papers that emphasize recent advances in the many areas related to EUV lithography technologies, and efforts toward commercialization.

Technical and scientific papers advancing the state of the art in EUV Lithography in the following areas are solicited:

PATTERNING
- integration learning and yield
- resolution enhancement techniques
- EUV impact on design optimization
- in-fab inspection and control
- double-patterning EUVL
- imaging simulations and source-mask optimization
- cost of ownership
- extendibility and future of EUV lithography.

MASKS
- substrates and blanks
- aerial imaging, patterned and blank mask inspection
- absorber materials and patterning
- mask roughness
- flare-reduction technologies
- reticle-handling solutions
- pellicle development and platform integration
- architectures for higher numerical apertures.

EXPOSURE TOOLS
- imaging performance
- focus, dose, and overlay control
- aberrations, flare, and out-of-band light
- optics design and fabrication
- multilayer coatings
- high-NA or anamorphic imaging systems.

SOURCES
- power scaling
- efficiency and reliability
- source characterization
- source collectors, cleaning, and lifetime
- new concepts and pupil-fill technologies.

EUV RESISTS
- resolution
- line-edge roughness and stochastic mitigation
- sensitivity improvement
- patterning stacks and etch transfer
- emerging organic and inorganic materials and novel chemistries.

LIFETIME
- environment control
- surface contamination and cleaning
- capping layers
- particle contamination, mitigation and removal.
Novel Patterning Technologies 2018 (AL102)

APPLICATION AREAS FOR NOVEL PATTERNING TECHNOLOGIES
- novel patterning for semiconductor 7nm IC nodes and beyond
- semiconductor wafer level packaging and fan-out
- bioelectronics and genomics
- photovoltaics and related energy applications
- disk drives and patterned media
- large-area display/flat-panel displays
- roll-to-roll/web format device manufacturing
- bioelectronics and LEDs
- photonic crystals and metamaterials
- negative-refractive-index materials
- nanopatterned sensors, waveguides, antennas
- building blocks for defect-tolerant computing
- smart resists and self-healing materials
- tools/materials to improve existing scanner performance.

TECHNOLOGY AREAS FOR NOVEL PATTERNING APPLICATIONS
Direct Write or Maskless Lithography and Patterning Technologies
- electron or ion charged-particle beams
- optical beams
- STED (2-color) direct write
- resistless e-beam or ion beam direct patterning
- beam-directed nucleation, ion-beam deposition
- metal or ceramic powder sintering
- material ablation or material transformation reactions
- ink-jet
- scanning probe lithography, dip-pen printing, tip-based patterning
- interference, plasmonic or nearfield/evanescent wave lithography
- micromirror optical lithography
- 3D metal or ceramic sintering.

Process Based Lithography and Patterning
- directed self-assembly
- nanoimprint lithography
- selective deposition
- self-aligned or pitch division process integration techniques.

In the spirit of facilitating exchange of knowledge, we strongly encourage contributions with background on the technology, details on latest results and limitations/opportunities for future development.

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Pavan Chandra Konda presented “Scheimpflug multi-aperture Fourier ptychography: coherent computational microscope with gigapixels/s data acquisition rates using 3D printed components” at SPIE Photonics West 2017. Authored by Pavan Chandra Konda; Jonathan M. Taylor; Andrew R. Harvey; doi: 10.1117/12.2251884; CID 100760R.
Metrology, Inspection, and Process Control for Microlithography XXXII (AL103)

Conference Chair: Vladimir A. Ukwintsev, Gorvo” (USA)

Conference Co-Chair: Ofer Adan, Applied Materials (Israel)

Program Committee: John A. Allgair, International Consortium for Advanced Manufacturing Research (ICAMR) (USA); Masafumi Asano, Toshiba Corp. (Japan); Benjamin D. Bunday, GLOBALFOUNDRIES Inc. (USA); Jason P. Cain, Advanced Micro Devices, Inc. (USA); Hugo Cramer, AMI, Netherlands B.V. (Netherlands); Timothy F. Crimmings, Intel Corp. (USA); Daniel J. C. Herr, The Univ. of North Carolina at Greensboro (USA); Chih-Ming Ke, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan);

Shunsuke Koshihara, Hitachi High-Technologies Corp. (Japan); Yi-Sha Ku, Industrial Technology Research Institute (Taiwan); Byoung-Ho Lee, SK hynix, Inc. (Korea, Republic of); Harendra Rana, Western Digital Corp. (USA); Christopher J. Raymond, Nanometrics Inc. (USA); John C. Robinson, KLA-Tencor Corp. (USA); Martha I. Sanchez, IBM Research - Almaden (USA); Matthew J. Sendelbach, Nova Measuring Instruments Inc. (USA); Richard Silver, National Institute of Standards and Technology (USA); Eric Solecky, GLOBALFOUNDRIES Inc. (USA); Alexander Starikov, I&I Consulting (USA); Alok Vaid, GLOBALFOUNDRIES Inc. (USA)

Metrology-based analysis, identification, and control of error sources continue to enable rapid evolution of optical microlithography. Metrology of exposure dose and focus supports ever-smaller process windows. Dimensional metrology in layouts facilitates resolution enhancement and validation of control. Extremely tight overlay is required for multiple windows. Dimensional metrology in layouts facilitates resolution enhancement and validation of control. Extremely tight overlay is required for multiple windows.

The conference is the leading forum for the exchange of foundational information and discussion of novel concepts in patterning-related metrology, inspection, and process control. Consistent with the conference charter and goals, please submit original technical papers in these and related technology areas:

**METROLOGY AND INSPECTION**
- optical full-field and scanned microscopy, scatterometry and interference microscopy
- novel measurement techniques with high-resolution optics, scatterometry, SEM, AFM
- particle-beam scanned microscopy, materials characterization, and elemental analysis

- design rules, design compliance, hot spots, design-based metrology and inspection
- metrology for design rules and process margins, budgeting, and budget control
- metrology for lithography development, patterning models build and validation
- metrology on photomasks, including pre-compensation, OPC, and phase shifting
- machine and deep learning application in metrology and inspection for capability and productivity
- parametric electrical testing and other device performance-based metrology
- applications in emerging patterning technologies including optical immersion and EUV lithography, direct-write, nano-imprint, and directed self-assembly
- applications in manufacturing of ICs, cell stacking, wafer bonding, TSV and 3D integration, displays, thin-film heads, MEMS, MOEMS, bio-arrays, lab on the chip, integrated optoelectronics and other micro- and nano-systems.

**CRITICAL DIMENSION, EDGE PLACEMENT AND OVERLAY**
- 1D, 2D, and 3D metrology of CD and pattern placement, including within device layouts
- alignment, registration and overlay metrology, processing and metrology integration
- edge profile and edge placement, roughness of edge, width, and centerline
- optical, SEM, and AFM based in-die overlay on small targets and devices.

**MEASUREMENT SYSTEM MODELING AND SIMULATION**
- physics and mathematical models of metrology process and detection methods
- physical characterization of both systems and samples, model parameters
- data analysis methods, library-based image analysis, and algorithms.

**CALIBRATION AND ACCURACY**
- metrology quality, error diagnostics, and data culling
- measurement resolution and error, including precision and accuracy
- standards and reference materials, calibration methods, hybrid metrologies
- reference measurement systems and metrology comparisons
- tool fleet performance, maintenance, and matching.

**PROCESS CHARACTERIZATION, CONTROL, PERFORMANCE, AND YIELD**
- process metrology and monitors, segmentation and reduction of variance
- metrology sampling, excision detection, costs, device performance, and yield
- data analysis and visualization, process control, feedback and feed forward
- big data analysis and diagnostic methodologies.
DEFECT DETECTION, ANALYSIS, AND CONTROL
• detection and control of pattern defects and across-wafer process variation
• defect review, defect reduction, yield improvement, effective data use
• environmental contamination, including impacts on processing and defects.

PERFORMANCE LIMITS IN METROLOGY AND INSPECTION
• responses to commanded skews and cross-technology comparisons
• models of tool-sample interaction, noise, and error mechanisms.

THE DIANA NYYSSONEN MEMORIAL BEST PAPER AWARD
The Diana Nyyssonen Memorial Best Paper Award for the best paper of the Conference on Metrology, Inspection, and Process Control for Microlithography recognizes the most significant current contribution to the field, based on the technical merit and persuasiveness of the oral presentation, as well as on the overall quality of the paper published in Conference Proceedings. The Diana Nyyssonen Memorial Award consists of an SPIE citation and an honorarium.

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THE KAREL URBÁNEK BEST STUDENT PAPER AWARD
The Karel Urbánek Best Student Paper Award recognizes the most promising contribution to the field by a student, based on the technical merit and persuasiveness of the paper presentation at the conference. The Karel Urbánek Best Student Paper Award consists of an SPIE citation and an honorarium.

To be eligible, the leading author and presenter of the paper must be a student. To establish eligibility, the principal author’s bio submitted with the abstract must state the academic status and the institution, as well as the advisor’s name and contact information.

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“...you get to meet so many professional people that have the same interest in the lithography field. You can discuss so much about the latest technologies.”

– 2017 Author

Save the date

ABSTRACTS DUE: 28 August 2017

AUTHOR NOTIFICATION: 23 October 2017
The contact author will be notified of acceptance by email.

MANUSCRIPT DUE DATE: 29 January 2018

PLEASE NOTE: Submissions imply the intent of at least one author to pay registration, attend the meeting, make their presentation as scheduled, whether poster or oral, and submit a 6-page minimum manuscript for publication in the conference Proceedings of SPIE in the SPIE Digital Library.
Advances in Patterning Materials and Processes XXXV (AL104)

Conference Chair: Christoph K. Hohle, Fraunhofer Institute for Photonic Microsystems (Germany)

Conference Co-Chair: Roel Gronheid, KLA-Tencor/ ICOS Belgium (Belgium)

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The limits of optical lithography have been extended, in no small part, by innovative materials and processes that expand and improve on fundamental resist progress to provide high-resolution, robust, and cost-effective technologies for both mass production and development of future device generations. Evolutionary and ultimately revolutionary innovations continue to be required in patterning processes and resist materials to achieve the combination of resolution, edge roughness, and sensitivity required for future materials and processes. The Advances in Patterning Materials and Processes conference is the leading forum for scientists and engineers from institutes, material as well as equipment vendors, and end-users around the world to present and discuss research on the chemistry, physics, and performance of photoresists as well as other patterning materials. This conference welcomes submissions of original papers that emphasize recent advances in high-performance patterning processes and materials and their integration in established, maturing, emerging, and new lithographic technologies. Original technical papers are solicited, but not limited to the following topics:

MATERIALS, PROCESSES AND APPLICATIONS
- photoresists for EUV lithography
- photoresists for 193nm (immersion) as well as for lithography at longer wavelengths
- positive and negative tone materials and processes (PTD, NTD)
- chemistry, processing and materials science of self-assembling materials (DSA)
- topcoats: contamination and reflection control
- underlayers: reflection control, pattern transfer, process enhancement and multilayer integration
- patterning materials and processes for electron-beam and nanoimprint lithography (NIL)
- chemistry, processing, and materials science of selective deposition as an enabler for patterning.

PROCESSING AND PROCESS CONTROL
- single and multiple patterning
- implant processing
- resist smoothing, rectification, trim and shrink
- tone inversion materials
- applied processing, including defect control and pattern collapse mitigation
- materials challenges related to etch, process control and metrology
- new processing techniques and applications, especially self-aligned strategies
- materials for photonic applications, NEMS, MEMS and MOEMS
- thick films for SOC/SIP integration.

SIMULATION AND MODELING
- resist fundamentals
- materials chemistry and processing
- assessment of patterning and materials scaling limits
- variability, stochastics, and pattern formation
- design for or simulation of new processes and applications.

Abstracts, that are addressing overlapping topics with adjacent conferences of the SPIE Advanced Lithography symposium (e.g. EUV, DSA, Etch) may be arranged in appropriate joint sessions.

Consistent with the conference’s charter and goals, authors are required to provide a description of chemical and physical principles as well as sufficient chemical structural detail in presented work. Submissions which do not reveal sufficient chemical details so as to add value to the readers or are principally of a commercial nature may not be accepted for presentation and publication.
Optical Microlithography XXXI (AL105)

Program Committee: Will Conley, Cymer, An ASML company (USA); Andreas Erdmann, Fraunhofer-Institut für Integrierte Systeme und Bauelementetechnologie IIISB (Germany); Carlos Fonseca, Tokyo Electron America, Inc. (USA); Bernd Geh, Carl Zeiss SMT Inc. (USA); Yuri Granik, Mentor Graphics Corp. (USA); Harsha Grunes, Intel Corp. (USA); Young Seog Kang, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Sachiko Kobayashi, Toshiba Corp. (Japan); Kafai Lai, IBM Corp. (USA); Kevin Lucas, Synopsys, Inc. (USA); John S. Petersen, Periodic Structures, Inc. (USA); Mark C. Phillips, Intel Corp. (USA); Daniel Sarlette, Infineon Technologies Dresden (Germany); Xuelong Shi, Shanghai Integrated Circuits Research & Development Ctr. (China); Bruce W. Smith, Rochester Institute of Technology (USA); Kauhiro Takahashi, Canon Inc. (Japan); Geert Vandenberghe, IMEC (Belgium); Reinhard Voelkel, SUSS MicroOptics SA (Switzerland); Da Yang, Qualcomm Inc. (USA); Uwe D. Zei�ner, Fraunhofer-Institut für Angewandte Optik und Feinmechanik (Germany)

Many innovations, the integration of new technologies and the continuous improvement of manu-facturing techniques for lithographic equipment have enabled optical projection lithography to stay the primary lithographic technology for semiconductor manufacturing for about 40 years. After the intro-duction of high NA ArF immersion technology, the progress of optical lithography is mainly related to the holistic optimization of lithographic systems and processes, and to an improved image and process control. In addition to resolution, edge placement error (EPE) control and high quality photomasks are required to support the application of material-driv-en resolution enhancements including double or mul-tiple exposure/patterning and directed self-assembly (DSA). The successful use of optics to provide via-ble working solutions for future technology nodes will require fundamental integration of all aspects of the patterning process. Optical projection lithogra-phy will keep its dominating role in semiconductor manufacturing. However, cost-effective solutions and appropriate combinations with other lithograph-ic techniques, including DSA, extreme ultraviolet li-thography (EUV) and multiple-e-beam direct-write (MEBW) have to be identified to support the further scaling of semiconductor products.

Optical lithography is also used in many other ar-eas of micro- and nanofabrication, including power semiconductors, silicon photonics, flat panel dis-plays, MEMS, NEMS, microfluidics and biosensors. Al-though the required feature size is significantly larger than for high-end IC-fabrication, these applications come with other requirements such as special pro-file shapes, non-Manhattan layouts, extreme overlay and CD-uniformity requirements, extremely high topography, unbalanced pattern densities etc. Many of these applications use alternative optical exposure techniques ranging from mask proximity printing, gray tone techniques, interference lithography and Talbot imaging to innovative laser direct write tech-niques such as multi-wavelength and STED-inspired lithography for 3D patterning.

This conference welcomes abstract submissions cov-ering topics that are advancing the field of optical nano- and microlithography for IC-fabrication and other areas of micro- and nanofabrication. Submis-sions on alternative exposure techniques and non-IC applications will be considered for joint sessions on “Advanced Lithography and Patterning for Emerging Markets”. Additional joint sessions of the SPIE Ad-vanced Lithography symposium will address overlapping topics between optical lithography and design for manufacturing, materials and metrology.

Specific topics of this conference include, but not limited to:

**PUSHING THE LIMITS OF OPTICAL LITHOGRAPHY**
- optical lithography at k1 < 0.3 options
- multiple exposure and multiple masking techniques including requirements and challenges of cut-masks
- novel illumination and mask types
- novel materials and processes to break optical diffraction limit
- alternative imaging methods: STED-inspired techniques, multi-color lithography, negative index and plasmonic lenses
- layout regularization and optimization to extend the limits of optical lithography
- design compliance towards multiple patterning such as SANP or LE¬n
- complementary lithography with DSA, e-beam, EUV, imprint to extend resolution for optical lithography.

**LITHOGRAPHIC IMAGING FUNDAMENTALS AND PROCESS INTEGRATION**
- multiple masking in manufacturing: results and issues
- process integration of resolution enhancement methods, CD shrink and multiple patterning techniques
- image and process analysis and assessment: Characterization and minimization of CD and overlay variation; EPE requirements in the context of multiple patterning
- simulation of full systems and process components including rigorous modeling of optical, resist and mask effects
- mask effects on imaging, including mask-induced focus shifts and aberrations
- negative-tone processes and related modeling techniques
- LER reduction and analysis.

Continued next page
Computational Lithography
- Predictive modeling and verification
- Fast 3D mask and wafer topography models
- 3D resist and etch modeling for OPC
- Advanced pattern correction, OPC and verification
- Advanced pattern matching for hotspot detection
- Source mask pupil optimization (SMO) and inverse lithography technology (ILT)
- Advanced mask decomposition algorithms
- Multi-layer aware OPC, verification and hotspot detection
- Model-based retargeting and layout modification to compensate process effects
- Machine learning application and data mining methodology.

Lithography Tools and Subsystems
- Exposure tools and tracks that support multiple exposure processes
- Overlay control down to 2nm and below, including effects of grid matching
- Overlay mark optimization towards product feature placement
- OPO (On Product Overlay) improvement
- Tool control for OPC stability and matching through multiple layers integrated OPC and tool control
- Design and materials issues for imaging
- Advances in system design and integration
- Novel advances in system self-metrology
- Exposure tool and source developments
- Illumination metrology and control, including polarization
- Evaluation and characterization of lens performance
- Metrology systems for set-up, adjustment, and control
- Environmental health systems and contamination control.

Lithography Costs
- High-throughput tools and processes
- Productivity and cycle time improvement, advanced process control (APC)
- Process simplifications including “freezing” alternatives
- Product layout and cost considerations.

Optical Lithography Systems for Non-IC Applications
- Silicon photonics and communications
- Flat panel and display applications
- MEMS, NEMS, and microfluidics
- Biological applications: biosensors and 3D skeletons for stimulation of cell growth
- Optical micro- and nanostructure fabrication
- Data storage applications such as HDD and patterned media
- Flexible electronics and organic electronics
- Lighting, PV and solar cells nanopatterning
- Micro-stereolithography
- Holographic applications
- Plasmonic applications
- Alternative exposure techniques.

Best Student Paper Award
Students submitting papers to AL105 (Optical Microlithography) and AL101 (EUV Lithography) will be considered for the Cymer Scientific Leadership Award for Best Student Paper. This award is given each year at this conference and recognizes extraordinary work achieved by students interested in the microlithography field, and strongly supports the contributions made to scientific advancement at the conference. The award includes a plaque along with a monetary award to help student’s future research activities.

All candidates for the Cymer award, including those who are placed as an oral presentation, are asked to present their work on a poster during the poster session for the Optical Microlithography conference.

If you are/have a student author or co-author that is making the presentation in the Optical Microlithography conference or EUV lithography, please send your tracking number to Will Conley at: will_conley@cymer.com.

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Design-Process-Technology Co-optimization for Manufacturability XII (AL106)

Conference Chair: Jason P. Cain, Advanced Micro Devices, Inc. (USA)

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Process-driven constraints to design have been a reality for multiple generations of semiconductor manufacturing, and design for manufacturability has become a widely adopted spectrum of tools and methods. This conference, aimed at technical and management professionals engaged with the interface between integrated circuit design and manufacturing, invites articles that examine novel approaches for design and process integration aimed at “more Moore” enablement, fast turn-around, cost-effectiveness, and high-yielding integrated circuit (IC) creation. Contributions should emphasize fundamentals of technical solutions rather than their commercial embodiments. Submissions in design-for-manufacturability, circuit and yield characterization, and other interdisciplinary studies, including but not limited to those based on electronic design automation (EDA), are welcome.

Topics of interest include, but are not limited to:

**DESIGN FOR MANUFACTURING**
- physical layout optimization for advanced or novel patterning methodologies
- design and verification methodologies using novel manufacturing models
- layout optimization for systematic and random yield loss reduction
- layout optimization for minimizing circuit variability
- manufacturing friendly circuit design styles and methodologies
- DFM for “more than Moore” applications (analog, RF, digital/SoC, etc.)
- deep learning and data analytics for layout analysis and optimization.

**DESIGN-AWARE MANUFACTURING**
- leveraging design-intent information (beyond layout) for RET/OPC application
- propagating electrical design intent for RET/OPC optimization and verification
- performance-power-manufacturability (speed-leakage-RET) optimization.

**DESIGN AND MANUFACTURING CO-OPTIMIZATION**
- design for multipatterning (MP) technology
- design for directed self-assembly (DSA) technology
- design for interferometric lithography and novel subtractive and additive patterning techniques
- design-rule development strategies and methodologies
- layout style and lithography co-optimization (including optical source and design co-optimization) for standard
- cells, SRAM, and digital logic design
- design-to-process simulation and calibration
- design-to-manufacturing methodologies for analog circuits, MEMs, and other microlithography applications.

**DESIGN-TO-MANUFACTURING ECONOMICS**
- cost-performance tradeoffs between design and manufacturing
- design to manufacturing flow methodologies for productivity improvement, time-to-market, and cost reduction
- new models for maximizing net return on investment in design and manufacturing.

Special consideration will be given to papers that emphasize methodologies for using manufacturing information in the design flow. Abstracts with a preview of results and conclusions supported by technical data are favored for oral presentation.

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The increasing interdependence of lithography technologies, photoresist technologies, and plasma etch technologies has created new opportunities in materials, integration, and the co-optimization of plasma based patterning with lithography and process control. Looking beyond, semiconductor process and manufacturing knowledge in nanopatterning is now enabling new areas such as IoT and neuromorphic computing.

Original and overview technical papers are solicited on, but not limited to, the following topics:

- novel developments in plasma based patterning techniques: EUV-based patterning, self-aligned spacer technologies (SAXP and mandrel/spacer design), DSA, nanoimprint, optical lithography patterning, complementary patterning, self-aligned structures, on product overlay, edge placement error mitigation strategies and cost modeling of the proposed patterning schemes
- novel discoveries of plasma–material interactions: plasma-photoresist interactions, LER/LWR evolution, EUV resist interactions, MOL/BEOL (low-k) material interactions, novel substrate material handling (SiGe, III–V, C, nonvolatile memory) etc.
- etch challenges for 3D memory architectures
- novel litho–etch interactions found in HVM
- defect reduction or yield enhancement techniques by dry or wet process solutions
- new etch methodologies and their application to patterning processes: atomic layer etching (ALE), low Te processing, etc.
- patterning control through advanced process solutions: in-situ process control, process simulations, etch aware OPC, edge place error (EPE) etc.
- advanced patterning, process, and selective deposition methods for novel etch-pattern transfer applications
- novel holistic (litho, etch, and deposition) patterning solutions for logic and memory applications
- etch and deposition processing solutions for emerging product applications including but not limited to: neuromorphic computing, quantum computing, power semiconductors (GaN, others), IoT devices, photonic devices, MEMS, MOEMS, other “more than Moore devices” and derivative technologies (RF, analog or mixed signal).

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All participants, including invited speakers, contributed speakers, session chairs, co-chairs, and committee members must pay a registration fee. Fee information for conferences, courses, a registration form, and technical and general information will be available on the SPIE website in November 2017.

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