Silicon-on-insulator technology enables next-generation radiation image sensors

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The fabrication process can reduce multiple scattering effects and decrease pixel size, paving the way for improved x-ray, charged particle, and neutron detectors.

Combining a radiation sensor and an intelligent large-scale integrated circuit on a monolithic chip has long been desired in many fields, such as nuclear and high-energy physics, astrophysics, medical imaging, and materials science. Such detectors need two kinds of silicon (Si) crystals: a thick, high-purity layer for efficiently detecting radiation and a thin one with many dopants for implementing high-performance devices.

Existing radiation imaging devices are mainly built from two different chips—a sensor and readout electronics—and these two are bonded with bulky metal bumps. Thus, unwanted materials cause multiple scattering, and the bump size limits the pixel size. In addition, high false capacitances limit the readout speed and signal-to-noise ratio.

To improve the imaging device quality, we used silicon-on-insulator (SOI) technology. We employed bonded SOI wafers, which are composed of low-resistivity Si on top for readout electronics, and high-resistivity Si (called a handle wafer or substrate) at bottom for the sensor. The two layers are bonded with thin silicon dioxide (SiO$_2$), referred to as buried oxide (BOX). We implanted ions of boron (p+) and phosphorous (n+) into the substrate after removing part of the top Si and BOX materials in each pixel. We then formed contacts to connect the sensor with the readout electronics of the SOI layer.

Figure 1 shows the basic structure of the SOI radiation image sensor. This approach has many advantages. For instance, eliminating the mechanical bump bonding reduces multiple scattering contributions and reduces potential pixel size. In addition, SOI processes are generally tolerant to radiation. Finally, transistors formed on the wafer have less parasitic capacitance compared with conventional bulk complementary metal oxide semiconductor (CMOS) processes, helping increase circuit speed and reduce power consumption.

Research and development of radiation imaging sensors started in 2005 at KEK in collaboration with OKI Semiconductor Company Limited, which provided the fully-depleted CMOS SOI process. To reduce costs, we used a multi-project wafer (MPW), sharing the process masks with other users. KEK organized MPW runs twice in 2008, and more than 15 designs were fabricated in each process (see Figure 2).

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<th>Figure 1. The silicon-on-insulator (SOI) sensor’s basic structure. The thickness of the top silicon layer and BOX is ~40nm and 200nm, respectively. The sensor can be thinned from 700µm to tens of microns, depending on the application. SiO$_2$: Silicon dioxide. NMOS: N-type metal oxide semiconductor. PMOS: P-type metal oxide semiconductor.</th>
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We developed several transistor test chips and image sensors. In the first MPW run, we successfully fabricated an integration-type imaging sensor with 32×32 pixels, and confirmed the readout electronics’ basic performance.\(^\text{1,2}\) In the second run, we

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increased the chip size to $5 \times 5\, \text{mm}^2$ and the number of pixels to $128 \times 128$. We obtained x-ray images with the prototype (see Figure 3). The smallest pixel size designed so far is $10 \times 10\, \mu\text{m}^2$. It will be used for beam monitors in high-energy experiments, as well as x-ray applications for materials science that require a fast readout system. We also developed a counting or digital imaging sensor. It performs well with laser light, x-rays, and charged particles. These sensors can be used for x-ray imaging applications requiring a strong x-ray intensity and wide dynamic range, and for high-energy charged particle trackers under severe radiation circumstances.

The next step is to improve sensor quality. The most recent submission—in February 2009—combined 15 designs from Japan, the US, and Europe. The process completed in May and all chips will be tested. In this process, we used a new implantation method that aims to reduce the back-gate effect, which affects the transistor threshold voltage. We are also investigating 3D integration techniques that bond multiple SOI wafers vertically. We plan to increase the number of yearly MPW runs. Our primary goal is to apply the sensor to high-energy physics and x-ray research applications.

Figure 2. Photograph of a multi-project wafer (MPW) wafer after processing. Each one included 15 user designs. OKI: OKI Semiconductor Company Limited. LBNL: Lawrence Berkeley National Laboratory. JAXA: Japan Aerospace Exploration Agency. FNAL: FermiLab. Univ. of Hawaii: University of Hawaii.

Figure 3. An image of a metal mask with the number ‘07’ cut into it, obtained with a $128 \times 128$ pixel SOI imaging sensor and an 8keV x-ray.

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**References**