Critical dimension metrology: perspectives and future trends

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3D-metrology is becoming mandatory for nanofabrication in the production environment.

Every flowchart in micro- and nanofabrication includes several critical dimension (CD) metrology steps to guarantee device performance. To measure pattern density in highly-controlled processes such as lithography, plasma etching, and materials deposition, engineers traditionally employ electron- or photon-based techniques. Most common in semiconductor manufacture are scatterometry, an optical diffraction-based method, and scanning electron microscopy (CD-SEM), a secondary electron emission-based technology. Although both are eminently repeatable, fast, and useful in terms of cost per measurement, will they remain state-of-the-art with the advent of ever smaller nanodevices?

Indeed, as dimensions and architectures move towards sub-32nm node, CD metrology, both for production process monitoring and process development, must cope with challenges presented by the latest materials, the new process flowcharts like the double patterning approach for lithography, and novel architectures such as 3D-multiwires field-effect transistor (FET) devices (see Figure 1).

Therefore, accuracy of measurement at the nanometer scale in all axes (x, y, and z) represents the advent of a non-negligible factor in the race to downsize device dimensions, as illustrated in Figure 2. For the conventional complementary metal-oxide semiconductor (CMOS) device with vertical gate and channel underneath, the single most important parameter is the bottom CD value (CD1 as indicated in Figure 2a). However, for nanowire FET devices, a full set of parameters must be tightly controlled as described in Figure 2b, with in-line metrology including alignment, thickness, critical dimensions, and length.

In addition to a multiple set of morphological outputs for future nanodevices, feature edge roughness will play a key role in the quality of device performance and in the ramp-up time for pilot lines. Indeed, as illustrated in Figure 3, as we are

Figure 1. Architectures (with source, gate, and drain terminals as indicated) for field-effect transistor devices are shown in (a) and (b). Scanning electron microscope (SEM) view of a multifingers trigate device is shown in (c) and a SEM cross-section view of a multi-nanowire transistor after release of the nanowires in (d).

Figure 2. Image (a) by transmission electron microscopy shows a conventional complementary metal-oxide semiconductor gate. Image (b) by SEM shows a multi-nanowire field-effect transistor. Δa: alignment. t: thickness. CD: critical dimension.

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moving down to sub-32nm devices, the linewidth roughness (LWR) parameter that corresponds to the $3\sigma$ CD variation along the line is becoming ever more critical, specifically for devices in which the nanowire represents the channel that must remain optimally smooth in order to obtain best performance (Maximum $I_{ON}$).

Photon- or electron-based CD metrology techniques, such as scatterometry and CD-SEM, are not able to satisfy industrial requirements for controlling fabrication of nanowire devices. They lack necessary accuracy when applied to complicated material stacks—to transistors, that is, manufactured with new and more complex constituents. We believe that 3D atomic force microscopy (3D-AFM) is currently the only capable technique able to measure and control this kind of device fabrication (see Figure 4). Over the past five years, we have worked in partnership with a tool supplier (Veeco) and probes supplier (Team Nanotec Gmbh) to further develop 3D-AFM,$^4$–$^8$ which is now capable of managing in-line process control of nanowire FET devices as illustrated in Figure 4.

Figure 4. Principle of 3D atomic force microscopy (3D-AFM) indicates (a) typical shape of a flared silicon tip and (b) oscillations of the tip and scanning on three axes.

**Figure 5.** Moving the industrial environment forward and in the right direction will require significant efforts with a view toward designing advanced probes in order to manage further extreme scaling of nanowire devices.

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**References**


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