

Paving the way for carbon nanotube integrated circuits

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Highly efficient carbon nanotube field-effect transistors employing scandium contacts could help usher in the next generation of nano-electronic devices.

Rapid increases in computer processing power over the past 40 years have been driven by the steadily decreasing size of metal oxide semiconductor field-effect transistors (MOSFETs). These comprise a n-type conductor, with negative electrons as the major charge carrier, joined to a p-type conductor, with positive 'holes' as the major charge carrier.

But the MOSFET will soon reach its technological and fundamental physical limits¹. This is leading researchers to look for alternative technologies, with semiconducting carbon nanotubes (CNTs) now considered to be one of the most promising building blocks for future nanoelectronic devices².

Since the first CNT field effect transistor (CNTFET) was designed in 1998³, device performance has continually improved. By using palladium (Pd) electrodes and high-k materials (which are less prone to current leakage) as gate dielectrics, p-type CNT-FETs have now surpassed the capabilities of state-of-the-art silicon p-MOSFETs⁴.

However, the development of n-type CNTFETs has lagged behind. This is mainly due to the difficulty of fabricating a type of junction known as an ohmic contact or Schottky barrier-free contact between metal electrodes and the conduction band of the CNT. The slow progress in producing n-CNTFETs has greatly hindered the development of CNT-based integrated circuits.

We recently discovered that scandium (Sc) can be used to generate an ohmic contact with the conduction band of a CNT⁵. This is because Sc has a very low work function (the energy required to remove an electron; $\sim 3.3\text{eV}$) and forms a good physical contact with the CNT (see Figure 1a). As a result, there is good alignment between Sc and the conduction band edge of the CNT, producing an ohmic contact (see Figure 1). So, both a high on-state current and a high on/off ratio can be obtained simultaneously. In addition, this approach has a better stability in air than those previously reported by other research groups.

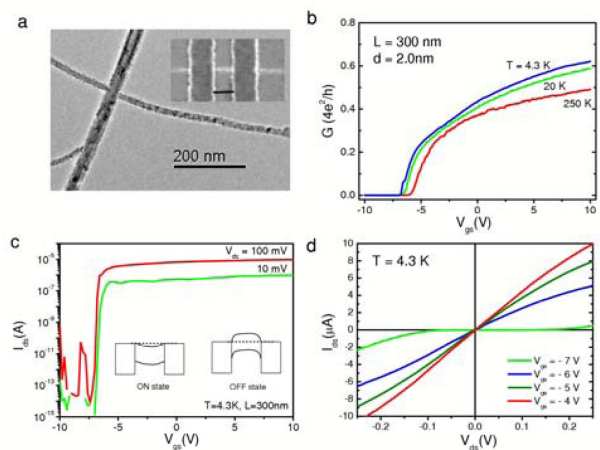


Figure 1. Back-gated single-walled carbon nanotube (SWCNT)-based n-type carbon nanotube (CNT) field effect transistor (FET) on a SiO₂ (100nm)/Si substrate. (a) Transmission electron microscope image showing scandium-coated CNTs of various diameters; (inset) scanning electron microscope image of the device (bar = 200 nm). (b) Low bias ($V_{ds} = 0.1\text{ V}$) conductance (G) vs gate voltage V_{gs} for a SWCNT with a diameter of 2.0nm and a length (L) of 300nm. (c) Transfer characteristics of the same device as in (b) for a different bias at 4.3K; (inset) schematic ON and OFF state band diagrams for a device with zero-Schottky barrier for electron injection into the conduction band of the CNT. (d) I_{ds} - V_{ds} curves for different V_{gs} and for the same device as in (b) at 4.3K; the linear behavior at ON state and the conductance increases with decreasing temperature indicate that the contact is ohmic. d : diameter.

By combining this new n-CNTFET, which can transport electrons very efficiently via a process known as ballistic transport, with a previously developed ballistic p-CNTFET, we have produced a doping-free CNT-based ballistic CMOS (complimentary metal-oxide-semiconductor) technology⁵. We have already demonstrated the feasibility of this technology by fabricating a simple complementary inverter. This involved forming a contact

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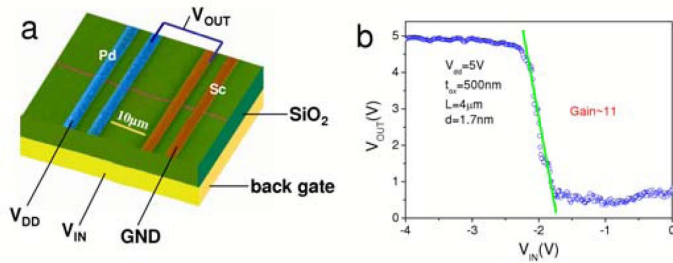


Figure 2. Back-gated SWCNT ($t_{ox} = 500\text{nm}$) complementary inverter. (a) Scanning electron microscope photo of a SWCNT-based complementary inverter with a p- and an n-type CNTFET fabricated on the same SWCNT. The polarity of the CNTFET is controlled by the injection of carriers to the valence band (hole carrier and p-type) and conduction band (electron carrier and n-type) using palladium (p-type) or scandium (n-type) electrodes. (b) Transfer characteristic for a complementary SWCNT-based inverter with a CNT diameter (d) of 1.7nm and a source-drain channel length (L) of 4 μm.

between an intrinsic CNT and two Pd and two Sc electrodes without any intentional doping (see Figure 2). In principle, much more complicated CMOS circuits could be integrated with CNTs placed on any suitable insulator substrate with top-gate geometry and high-k dielectrics.

An important feature of our CNT-based doping-free CMOS technology is that it simply requires patterned arrays of semi-conducting CNTs with moderately narrow diameter ranges, such as 1.6–2.4 nm, rather than CNTs with a defined chirality (alignment of the carbon bonds in the tube). These CNT arrays are within the reach of current nanotechnology techniques and could lead to the development of CNT-based CMOS devices with increasing complexity. To this end, we are now developing logic circuits based on this technology.

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