An ultrathin organic self-assembled monolayer gate dielectric enables low-leakage transistor fabrication on a wide range of substrates.

In recent years, single-walled carbon nanotubes (SWCNTs) have emerged as highly promising components for nanoscale devices. In particular, SWCNT-based field effect transistors (FETs), such as the one shown in Figure 1, have generated strong interest due to their excellent device characteristics.\(^1,\)\(^2\) These FETs are usually fabricated using a conventional three-electrode configuration consisting of source (S) and drain (D) electrodes in contact with a SWCNT semiconductor channel (white arrow in Figure 1), plus a gate (G) electrode, electrically insulated from source and drain by the gate dielectric. By applying a voltage to the gate electrode, the electrostatic potential—and hence the conductivity—can be tuned in the channel.\(^3\)

In maximizing the performance of SWCNT FETs, the contacts made to the SWCNT channel, the integrity of the SWCNT itself, as well as the gate dielectric are factors of the utmost importance. A high-performance gate dielectric has three major requirements. First, it has to have high capacitance to allow transistor operation at low gate voltages. Second, it must have good insulator properties to avoid undesirable gate leakage currents. And third, it must be compatible with a wide range of substrates. The most widely used configuration features a highly doped silicon substrate covered with a thermally grown SiO\(_2\) layer (thickness 100–200nm, growth temperature >700°C) that serves as a macroscopic back gate.\(^4\)

In our work, we seek to optimize the gate dielectric of SWCNT-FETs. To improve performance, we have explored devices that incorporate an organic gate dielectric. This gate consists of a 2nm-thick self-assembled monolayer (SAM) formed on a 4nm-thick SiO\(_2\) layer grown by plasma oxidation at room temperature, with the silicon substrate serving as back gate (see Figure 1).\(^5\) The SAM is formed at a temperature of 200°C and predominantly accounts for the excellent insulating properties of the dielectric stack. It reduces the leakage current by more than three orders of magnitude, namely, from 10\(^{-4}\)A/cm\(^2\) (in a SiO\(_2\) dielectric without SAM) to 10\(^{-7}\)A/cm\(^2\). For a thin (6nm), low-temperature processed, large-area dielectric, this value represents an exceptionally small current density. Owing to their low formation temperature, SAM gate dielectrics are compatible with unconventional substrates such as metallized plastic foils, thus enabling electronics on flexible substrates.\(^6\)

SWCNT-FETs with a channel length of 200nm and gold-palladium contacts were fabricated using e-beam lithography. The transistors exhibit an unprecedented combination of excellent performance parameters. The output characteristic resembles that of conventional p-type semiconductor FETs, including

Figure 1. Atomic force microscopy image of a single-walled carbon nanotube (SWCNT)–based field effect transistor. The SWCNT is colored red, and the white scale bar is 200nm. Inset: Chemical structure of the silane molecule constituting the self-assembled monolayer (SAM).
Figure 2. (a) Output and (b) transfer characteristics of a SWCNT transistor consisting of a SAM-based gate dielectric.

saturation of the drain current at higher \( V_{ds} \): see Figure 2(a). From the transfer characteristics of the devices, illustrated in Figure 2(b), a maximum transconductance \( g_m = \frac{dI_d}{dV_{gs}} \) of about 20\( \mu \)S is determined at \( V_{ds} = -1 \) V. This value is among the highest so far reported for SWCNT-FETs. In addition, the large ON/OFF drain current ratio of about \( 10^5 \) is remarkable in view of the small thickness of the gate dielectric and theoretical predictions on drain voltage scaling in SWCNT-FETs.\(^7\) Moreover, evaluation of the subthreshold swing \( S = \left[ \frac{dV_{gs}}{d\log I_{ds}} \right] \) yields a value of 60 mV/decade, which is very close to the theoretical limit at room temperature.\(^3\) Such a low value has not been previously reported for non-doped SWCNT-FETs with low operating voltages. Its realization with our devices is especially notable, considering that no attempts were made to reduce the contact resistance and that a global back gate was used.

The transfer characteristics of SWCNT-FETs commonly display an undesirable hysteresis in the drain current.\(^8\) This phenomenon has been ascribed to traps located within the bulk SiO\(_2\) gate insulator or near the nanotube/SiO\(_2\) interface, which can then fill with electrons from the nanotube channel.\(^1\) There have been a few reports where the hysteresis was reduced or eliminated by employing a liquid gate or by protecting the nanotube from air using inorganic dielectrics. In contrast, some of our SAM-based SWCNT-FETs exhibit essentially no hysteresis, despite the presence of a more convenient solid gate and the exposure of the CNT channel to air: see Figure 2(b). This lack of significant hysteresis can be attributed to the hydrophobic nature of the SAM-modified dielectric surface, which lowers the amount of adsorbed water, well documented as enhancing hysteretic behavior in nanotube FETs.\(^8\) The strong gate coupling achieved in our SWCNT-FETs by integrating an ultrathin organic SAM as a high-quality gate dielectric with low gate leakage current provides a highly versatile basis for further transistor development.