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The symposium, like our other conferences and activities, would not be possible without the dedicated contribution of our participants and members. This program is based on commitments received up to the time of publication and is subject to change without notice.

Conference 9985: Photomask Technology

Monday - Wednesday 12–14 September 2016

Part of Proceedings of SPIE Vol. 9985 Photomask Technology 2016

9985-1, Session 1

Make Lithography Great Again *(Keynote Presentation)*

Christopher J. Progler, Photronics, Inc. (United States)

No Abstract Available

9985-2, Session 1

Data analytics and machine learning for ID design-process-yield optimization in EDA, mask making, and semiconductor manufacturing *(Invited Paper)*

Luigi Capodieci, KnotPrime Inc. (United States)

Data Analytics and Machine Learning have been experiencing an accelerated (and greatly publicized) growth both in raw technical capabilities and in the number of application domains in virtually every industry. Nevertheless, adoption in the Semiconductor space throughout the Design-to-Manufacturing chain and across industry segments has been minimal. Starting from a synthetic survey of the state-of-the-art and ongoing developments in Data Analytics and Machine Learning, this presentation offers a perspective on the functional interactions and data information flows for IC Design-to-Manufacturing, and discusses risks and opportunities arising from the introduction of big-data (algorithmic) analytics and machine learning technologies, in response to the current challenges of advanced (end-of-Moore) IC nodes and semiconductor industry consolidation.

A quantitative definition of physical design space coverage is proposed in this work as the unifying abstraction available for all components of the Design-to-Manufacturing flow, allowing for the construction of a computational framework where (big) Data Analytics and Machine Learning methodologies and tools can be successfully applied.

The juxtaposition of Design-Technology-Co-Optimization (DTCO) with the novel paradigm of DFM-as-Search and their necessary integration in the DFM computational toolkit, clearly exemplify how the very advanced IC nodes (10, 7 and 5nm) can not only benefit from, but definitely require the adoption of a new class of correlation extraction algorithms for heterogeneous data sets.

9985-3, Session 1

Challenges of 10nm and 7nm CMOS for high-performance and low-power applications *(Invited Paper)*

Rama Divakaruni, IBM Thomas J. Watson Research Ctr. (United States)

No Abstract Available

9985-4, Session 2

World's 1st high-throughput multi-beam mask writer *(Invited Paper)*

Christof Klein, Elmar Platzgummer, IMS Nanofabrication AG (Austria)

The world's first high throughput multi-beam mask writer (MBMW) has been realized by upgrading the existing MBMW Alpha tool with a 10x faster data path. In this tool a multi-beam column provides 262k programmable beams of variable beam size. The current density is adjustable up to 1A/cm2, resulting in a total beam current of approximately 1 μA. With the upgraded 120 Gbps data path a full 7nm node mask can be written in less than 10 hours.

The performance of IMS' MBMW tool and its extendibility to future nodes will be discussed.

9985-5, Session 2

The technical consideration of multi-beam mask writer for production

Sanghee Lee, Byung-Sup Ahn, Jin Choi, In-Kyun Shin, Shuichi Tamamushi, Chan-uk Jeon, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

Multi-beam mask writer is under development to solve the throughput and patterning resolution problems in VSB mask writer. Theoretically, the writing time is appropriate for future design node and the resolution is improved with multi-beam mask writer. Many previous studies show the feasible results of resolution, CD control and registration. Although such technical results of development tool seem to be enough for mass production, there are still many unexpected problems for real mass production.

In this report, the technical challenges of multi-beam mask writer are discussed in terms of production and application. The problems and issues are defined based on the performance of current development tool compared with the requirements of mask quality. Using the simulation and experiment, we analyze the specific characteristics of electron beam in multi-beam mask writer scheme. Consequently, we suggest necessary specifications for mass production with multi-beam mask writer in the future.

9985-6, Session 2

Improvement of electron-beam lithography modeling for overdose exposures by using dill transformation

Mohamed Abaidi, LTM CNRS (France); Mohamed Saib, ASELTA Nanographics (France); Jean-Hervé Tortai, LTM CNRS (France); Patrick Schiavone, ASELTA Nanographics (France)

The Electron Beam Lithography (EBL) exhibits the best resolution over all lithography techniques [1]. Conversely this is the lithography technique dedicated for mask writing. It is mandatory to compensate for Proximity effects (PE) using compact models. Although current PE corrections are efficient for nominal process, it doesn't allow covering a broad process window, especially for overexposed patterns.

This paper shows how to improve the modeling accuracy of overexposed patterns by using a Dill transformation to the existing compact model. Current model uses a single level threshold that induces a lack of accuracy of simulation for overdosed patterns. These errors requires new models to enhance the reliability of the simulation of patterns that are overexposed. Advanced model package were developed and tested to reflect the chemistry mechanisms occurring in resist. The full modeling Inscale® software was used in this study. It offers a set of reliable modeling algorithms able to predict the electronic Aerial Image (E-AEI) and transform it to patterns contours using a standard resist model [2]. This paper shows that this resist model can be upgraded using a Dill transformation to

generate an Acid Aerial Image (A-AEI) that gives new pattern shape. This transformation needs only one input: the Dill parameter of the resist [3]. A strong impact is expected at high doses but no change occurs on patterns exposed close to nominal dose.

The experimental validation has been conducted on calibration design with patterns selected using sensitivity analysis [4]. Experimental measurements of these patterns were obtained when exposed at the nominal dose (1) and overdosed by 10% (1.1) and 20% (1.2). The process variability is evaluated to 1.2 nm. Calibration results of both standard and Dill models on these experimental data are compared. First, for both cases the calibration of the model using the Dill transform (E-AEI) gives the same parameters for the electron part of the model. Then, the estimated Dill parameter (0.05 μC/cm2) is consistent with values reported in the literature [5], pointing out the robustness of this new resist model. Root Mean Square errors (RMSE) of the simulation is 2, 1.6, 1.7 nm respectively with dose 1, 1.1 and 1.2 for standard model and 2, 1.3, 1.35 nm respectively for the advanced model. One can see that RMS values are slightly highest at nominal values due to outliers in measurements. The accuracy for nominal doses is kept at 2nm for both models. This is to be compared to the process intrinsic variability estimated at 1.2nm for the calibration set using repeated patterns.

To conclude, the new advanced model of Inscale® software from Aselta Nanographics allows increasing the overall accuracy by 62 % for a process window of dose with latitude extended up to 20%.

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9985-7, Session 2

Electron-beam mask writer EBM-9500 for logic 7nm node generation

Hideki Matsui, Takashi Kamikubo, Satoshi Nakahashi, Haruyuki Nomura, Noriaki Nakayamada, Mizuna Suganuma, Yasuo Kato, Jun Yashima, Kenichi Saito, Ryoei Kobayashi, Nobuo Miyamoto, Munehiro Ogasawara, NuFlare Technology, Inc. (Japan)

Semiconductor scaling is slowing down because of difficulties of device manufacturing below logic 7nm node generation. Various lithography candidates as ArF immersion with resolution enhancement technology like Inversed Lithography technology, Extreme Ultra Violet lithography and Nano Imprint lithography are being developed to break through the situation. In such advanced lithography, shot counts of mask patters will be estimated to be explosively increased in critical layers, and then it is hoped that multi beam mask writer (MBMW) is released to handle them within realistic write time. However, ArF immersion technology with multiple patterning with still continues to be a mainstream of the lithography for most of the layers. Then, the shot counts in less critical layers are estimated to be stable because of the limitation of resolution in ArF immersion technology. Therefore, single beam mask writer (SBMW) can play an important role for mask production still, relative to MBMW. Also the demand of SBMW seems actually strong for the logic 7nm node. To realize this, we have developed a new SBMW, EBM-9500 for mask fabrication in the generation. Newly introduced electron beam source enables higher current density of 1200A/cm2. Heating effect correction function can be also newly introduced to satisfy the requirements for both pattern accuracy and throughput. In this paper, we will report the configuration and performance of EBM-9500.

9985-8, Session 3

Material requirements for EUV mask substrates *(Invited Paper)*

Carlos A. Duran, Corning Incorporated (United States)

EUV Lithography has made significant progress towards production-scale adoption in recent years. As the long-awaited moment of widespread use approaches, it is meaningful to revisit the key requirements that must be fulfilled by all elements in the production chain. This talk focuses on the properties of mask substrate materials. The topic of mask material properties was a subject of discussion in the early stages, but moved out of focus as more pressing challenges required full attention. The requirement for low thermal expansion is the dominating feature in this context. After some consideration was given to glass-ceramics, the advantages of a single-phase glass became apparent, and the industry eventually settled on ultra-low expansion TiO_2-doped silica glass, known as ULE® Glass. We will discuss the different parameters that define the thermal behavior of ULE® Glass substrates, and how they can be tuned for optimal performance in view of the evolution of the operating conditions within the scanner. In particular, we discuss the choice of the material's “zero-crossing” temperature (i.e., the temperature at which the CTE(T) is exactly zero), and how this parameter should evolve as the light source output increases. We will also discuss material production readiness for large scale deployment of EUV lithography, and factors to be considered to enable timely availability of substrates with the correct parameters as material requirements evolve.

9985-9, Session 3

NXE pellicle development update

Derk Brouns, Daniel A. Smith, Andrea Mancuso, ASML Netherlands B.V. (Netherlands); Jim N. Wiley, ASML US, Inc. (United States); Paul Colsters, Par Broman, Eric Casimiri, Raymond Lafarre, David Ockwell, David van de Weg, Matthias Kruizinga, ASML Netherlands B.V. (Netherlands)

ASML introduced the NXE pellicle concept, a removable pellicle solution that is compatible with current and future patterned mask inspection methods. We will present results of how we have taken the idea from concept to a demonstrated solution enabling the use of EUV pellicle by the industry for high volume manufacturing. We will update on the development of the next generation of pellicle films with higher power capability. We will show imaging and overlay data acquired on 0.33 NA scanner exposures with use of the NXE pellicle along with a number of offline tests demonstrating the NXE Pellicle capabilities.

Further, we will provide an update on top level requirements for pellicles and external interface requirements needed to support NXE pellicle adoption at a mask shop; we will specifically revisit/revise the 2 μm maximum particle size on film and the nonuniformity specification of 0.2% as previously reported. We will explain the rationales behind the updated requirements.

Finally, we will present ASML's pellicle handling equipment to enable pellicle use at mask shops and our NXE pellicle roadmap outlining future improvements.

9985-10, Session 3

Development of a novel closed EUV pellicle for EUVL manufacturing

Yosuke Ono, Kazuo Kohmura, Atsushi Okubo, Daiki Taneichi, Hisako Ishikawa, Tsuneaki Biyajima, Mitsui Chemicals, Inc. (Japan)

Pellicle have been normally used as a dust cover film of the photomask for photolithography manufacturing from g-line lithography to ArF immersion lithography. Existing pellicle can in principle protect the pelliclized mask surface from particle pollution by completely covering the mask surface without any gaps, and then printing defects on wafers has been steadily reduced. As a result, it is a well-known fact that the design concept of this closed pellicle brings remarkable contribution for the improvement of productivity and yield in the manufacture of semiconductor chips. One of the most important features of pellicle is the closed structure to guarantee the clean-keeping performance of mask surface. As for the EUV pellicle, closed pellicle structure which has fundamentally no penetration path of particles is needed to guarantee the particle pollution free performance in EUVL manufacturing.

Pelliclized EUV mask experiences the significant pressure change from atmospheric pressure to high vacuum range in EUV inner-pod and then mask is led into the reticle stage in scanner. Pellicle membrane deflection due to the pressure difference between the inside and outside of pellicles must be below 0.5mm because the gap between membrane and base plate of inner pod is narrow. Expansion of the total filter area of pellicle will be generally effective for the suppression of membrane deflection. However, there is also an additional restriction that the stand-off of EUV pellicle must be 2.5mm. The height of the frames supporting the Si border becomes very low when we take into account the thickness of Si border which supporting a pellicle membrane. Therefore differential pressure cannot be suppressed by the method to put filters on the "side of the frame" like conventional ArF pellicle.

In the present study, we fabricated a novel closed EUV pellicle without any gaps by forming the vent holes in the Si border part and putting the sufficiently wide area filters on the top side of Si border. Sizes, areas and locations of filters were designed by taking into account the differential pressure during the pumping down and ventilation condition. Full-size closed EUV pellicle sample was installed in vacuum chamber and deflection of pellicle membrane was experimentally examined from the atmospheric pressure to vacuum pressure range during the pumping/ventilation condition. As the result, we found that the closed EUV pellicle can depress the membrane deflection below 0.5mm under the practical pumping down condition.

9985-11, Session 3

Introducing the EUV CNT pellicle

Jae Uk Lee, IMEC (Belgium) and KU Leuven (Belgium); Johannes Vanpaemel, Ivan Pollentier, Christoph Adelmann, Houman Zahedmanesh, Cedric Huyghebaert, IMEC (Belgium); Michael De Volder, Univ. of Cambridge (United Kingdom); Emily E. Gallagher, IMEC (Belgium)

EUV lithography insertion is anticipated at the 7 nm node and below; however, defects added to the mask during use is a lingering concern. Defectivity in the scanner is non-zero and an EUV pellicle membrane to protect the mask for high volume manufacturing power levels does not yet exist. The EUV photons are strongly absorbed by all materials. Si-based membranes leverage the low absorption coefficient k value (k = 0.0018 at 13.5nm) for reasonable transmission, but poly Si becomes fragile and wrinkles during the high temperatures associated with exposure. An alternate approach to high transmission is deploying very thin or porous layers so that there are fewer atoms to absorb light. For example, carbon nanomaterials have a reasonably low k value (k = 0.0069), but are strong enough to be fabricated in very thin layers. Graphene, graphite, carbon-nanosheets and carbon nanotubes are all candidate carbon nanomaterials for this application, but we focus here on carbon nanotubes (CNTs). Our first measurements on CNT films of ~60nm thick were found to have 95% transmission at 13.5nm. Adding CNT layers also enhanced the strength of a thin SiN membrane significantly. In this paper, critical pellicle metrics will be evaluated in more detail: EUV transmission, bulge test for mechanical strength, emissivity measurements for heat management, and exposure testing in a hydrogen environment.

9985-12, Session 3

Development of advanced multi-tone mask by using two different transmittance modulation materials

Sei-Min Kim, Min-Ki Choi, Seong-Min Seo, Jong Hwa Lee, Cheol Shin, Kee-Soo Nam, S&S TECH (Korea, Republic of)

High quality photomasks including phase-shift mask and half-tone-mask (HTM) have been investigated to achieve high-resolution and high-integration in recent years for flat-panel display process. Among of them, HTM has been widely used for thin-film transistor (TFT) fabrication process because of its high productivity. A major portion of manufacturing cost of the TFT depends on the number of the photomask.

However, the TFT industry is continuing to look for a cheaper option to fabricate TFT device, and the idea of multi-tone-mask (MTM) can be a good alternating candidate. MTM has a complex structure with multiple transmittance modulation layers which enables the control of light dose over the photoresist.

In this paper, the advanced MTM having two different materials which can act as an etch stop layer against to each other are investigated. A conventional MTM requires three mask writing processes to form three patterns whereas the proposed MTM design makes it possible to form three patterns by means of two mask writing processes.

The most significance of this design is very effective to decrease the mask manufacturing time as well as materials usage for extremely high productivity.

9985-13, Session 4

PMJ16 Best Paper: Multi-beam mask writer BMB-1000 and its application field

Hiroshi Matsumoto, Hideo Inoue, Hiroshi Yamashita, Hirofumi Morita, Satoru Hirose, Munehiro Ogasawara, Hirokazu Yamada, Kiyoshi Hattori, NuFlare Technology, Inc. (Japan)

No Abstract Available

9985-87, Session 4

PMJ 2016 Panel Overview: EUV, MPT, NIL: What challenges lie ahead for masks?

Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan)

No Abstract Available

9985-14, Session 5

Influence of non-uniform intensity distribution of locally deformed pellicle for N7 patterning

In-Seon Kim, Guk-Jin Kim, Hanyang Univ. (Korea, Republic of); Michael Yeung, Fastlitho Inc. (United States); Eytan Barouch, Boston Univ. (United States); Hye-Keun Oh, Hanyang Univ. (Korea, Republic of)

Extreme ultraviolet (EUV) lithography is one of the promising technology for fine and complex patterning, and it is initially targeted to sophisticated logic pattern because of high resolution capability and low optical proximity effects. In spite of high capability of patterning, some obstacles are still remained such as low source power, resist optimization, and defect control. In addition, EUV pellicle is essential for protecting mask from debris. The suggested EUV pellicle is made of inorganic material and it has extremely thin thickness for high transmission.

With these tight requirements, flawless fabrication of the pellicle is very difficult. Furthermore, high absorption of the EUV light leads not only deformation due to thermal expansion but also transmission drops due to oxidation. For these reasons, transmission of EUV pellicle can be varied during exposure process and the intensity distribution can also be changed.

Non-uniform intensity distribution caused by locally deformed pellicle leads critical dimension (CD) variation. We will report the influence of deformed pellicle in terms of transmission and CD non-uniformity with various patterns. With 0.4 % spatial non-uniformity (1 pass transmission), CD non-uniformity of 16 nm hp pattern is about 0.1 nm, but that of tip-to-line (22 nm) and tip-to-tip (31 nm) is about 0.15 nm. The influence of non-uniform intensity distribution of locally deformed pellicle could be serious for different pattern shapes and sizes. Local transmission non-uniformity spec of 0.4 % needs to be tightened to satisfy local CDU of 0.1 nm for N7 patterning.

9985-15, Session 5

Dependence of dissolution behavior of main-chain scission type resists on molecular weight

Akihiro Konda, Hiroki Yamamoto, Takahiro Kozawa, Osaka Univ. (Japan); Shusuke Yoshitake, NuFlare Technology, Inc. (Japan)

Ionizing radiations such as extreme ultraviolet (EUV) and electron beam (EB) are the most promising exposure source for next generation lithographic technology. For the realization of high resolution lithography, it is necessary to overcome the trade-off relationships among sensitivity, resolution, and line width roughness (LWR) of resist materials. In order to overcome them, it is important to understand the basic chemistry of resist matrices in resist processes. In particular, the dissolution process of resist materials is considered to be a key process. However, dissolution process has not been fully investigated especially for ultrathin films. In chemically amplified resists used for ionizing radiations, acid generators are decomposed through the dissociative electron attachment of thermalized electrons. This sensitization mechanism induces a resolution blur. On the other hands, main-chain scission type resists such as poly(methyl methacrylate) and ZEP520A are decomposed from their radical cations. From the viewpoint of sub-10 nm fabrication, the sensitization mechanism, with which the thermalized electrons are not associated, is attractive. Therefore, we investigated the dissolution behavior of main-chain scission type resists using EUV exposure tool and quartz crystal microbalance (QCM) method. Also, the change of main-chain scission type resists induced by EB radiation in molecular weight was analyzed by gel permeation chromatography (GPC).

Four kinds of PMMA with different molecular weight and ZEP520A were used as a main-chain scission type resists. PMMAs were dissolved into propylene glycol monomethyl ether acetate and ZEP520A is diluted with anisole. In the sample preparation for sensitivity and QCM experiments, resist solutions were filtered through a 0.20 ?m PTFE syringe filter prior to spin-coating onto silicon or QCM substrates in order to make clean films. Resist solutions are spin-coated onto silicon or QCM substrates to form thin films with c.a. 100 nm film thichness and exposed to EUV radiation (Energetic, EQ-10M). After EUV radiation, PMMAs were immersion-developed in o-xylene and methyl isobutyl ketone (MIBK)-isopropanol (IPA) mixture for 60 s and rinsed in IPA for 15 s. ZEP520A were developed in ZED-N50 (n-amyl acetate) and rinsed in ZMD-B (MIBK-IPA mixture). Dissolution behaviors of resists were investigated by the QCM-based development analyzer (RDA-Qz3). Resist film thickness was measured with a surface profiler (ET-200 (Kosaka Laboratory Ltd.)) and spectroscopic elipsometry (UVISEL (Horiba)). Also, the molecular weight of PMMA and ZEP520A degraded by EB radiation tool (EB-ENGINE) was analyzed using GPC system (Shodex GPC-104).

We measured sensitivity and dissolution behavior of PMMA with different molecular weight and ZEP520A. With increase of molecular weight, the sensitivity of PMMA decreased. It was observed that dissolution behavior of PMMA varies with molecular weight, exposure dose, and developer in the QCM measurement. It was indicated that the change of swelling behavior in PMMA with different molecular weight might lead to LWR formation. The comparison of dissolution behavior between PMMA and ZEP520A will be discussed in the conference.

9985-16, Session 5

Phase contrast pupil engineering for EUV actinic pattern inspection

Yow-Gwo Wang, Andy R. Neureuther, Univ. of California, Berkeley (United States) and Lawrence Berkeley National Lab. (United States); Patrick P. Naulleau, Lawrence Berkeley National Lab. (United States)

In this paper, we will discuss the possibility to utilize optimum phase shift in the pupil plan to enhance pattern defect sensitivity. Also, we will show the impact of the mask shadowing effect on defect behavior including: defect type, orientation, aspect ratio, and its interaction with the neighboring pattern when we apply optimum phase shift method. In the end we will compare our proposed method with the conventional bright field inspection method by a detail calculation of defect signal-to-noise ratio (SNR).

In our previous study on actinic blank inspection, we shows the possibility to utilize Zernike phase contrast method to enhance multilayer defect sensitivity, and optimum phase shift method to address the complex behavior of native defect on the EUV mask blank. In this study, we want to utilize the nature of the phase-shifted absorber material to enhance its defect sensitivity by optimum phase shift method. Also, we find that the defect behavior can be affected by defect type, orientation, aspect ratio, and its interaction with the neighboring pattern. This can result in a different strategy by optimum phase shift method for each defect. For example, the extrusion defect has a larger foot print than the intrusion defect under inspection even they have same physical size on the mask. Therefore, the defect behaviors are different and result in a different optimum phase shifts in order to maximize its defect sensitivity. The result also shows the possibility to improve defect signal strength by 40% using optimum phase shift in the pupil plane. Moreover, our simulation result finds that the interaction between defect location and shadowing effect can have huge impact on its behavior. For dense contact pattern, the defect at the left edge of the contact shows an absorption dominated behavior, while for the defect at the right edge of the contact; it shows a combination of phase and absorption. The coupling effect between pattern and defect can affect the defect behavior. The simulation result shows that for same type of defect, the signal enhancement by optimum phase shift method is 10% larger under the dense line pattern over the iso-line pattern situation.

Based on the detail study on various defects, we will discuss the possibility to improve pattern defect sensitivity by utilizing a general phase shifts in the pupil plane for a variety of critical defects. Preliminary result shows a 15% signal enhancement can be achieved by a general phase shift. Moreover,

we will compare our proposed method with the conventional bright field inspection technique by defect SNR which includes speckle noise from mask roughness, detector noise from typical EUV CCD camera, and photon shot noise as we did for actinic blank inspection study.

This research is sponsored by IMPACT+ (Integrated Modeling Process and Computation for Technology). Member companies – ARM, ASML, Global Foundries, IBM, Intel, KLA-Tencor, Marvell Technology, Mentor Graphics, Panoramic Tech, Photronics, Qualcomm, Samsung, SanDisk and Tokyo Electron. This work was performed in part at Berkeley Lab which is operated under the auspices of the Director, Office of Science, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231.

9985-17, Session 5

Feature size dependence of mask topography induced phase effects measured with an aerial imaging tool

Aamod Shanker, Univ. of California, Berkeley (United States); Martin Sczyrba, Falk Lange, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); Brid Connolly, Toppan Photomasks, Inc. (Germany); Andy R. Neureuther, Laura Waller, Univ. of California, Berkeley (United States)

Mask topography causes polarization dependent phase variations at the image plane of a lithography stepper, both at deep UV (193nm) and extreme UV (13.5nm) wavelengths. Since the perimeter to area ratio of mask features increases at smaller nodes, the phase contribution of thick mask edges/corners can be expected to grow in comparison to bulk effects. Using phase retrieval methods in a DUV Aerial Image Microscope, it is observed that while the imaging performance at the wafer is dominated by bulk phase at large feature sizes, mask edges/corners dominate for feature size near the diffraction limit, for both OMOG and ATT-PSM masks. Finally, a 2D thin mask model is used to extract mask parameters and quantify their individual impact on CD through-focus.

We have shown in earlier work that for well-resolved contact features, mask topography causes polarization-dependent phase at the wafer plane in an Aerial Imaging Measurement System (AIMS), not only for attenuating phase shift (ATT-PSM) but also for the thinner Opaque MoSi on Glass (OMOG) masks at 193nm [1]. Furthermore, thick mask edges cause additional spread in the wafer phase, similar to the affect of spherical aberration as described by other authors [2]. Since the wafer-phase impacts through-focus image intensity, thick-mask edges reduce the defocus process window by contributing an extra tilt to the critical dimension through-focus (Bossung plot) at the wafer, described analytically by the CD Transport of Intensity Equation (CD-TIE) [3]. As feature sizes reduce, the bulk phase contributed by the thick absorber area scales as the feature size squared, while the edge phase due to thick absorber edge scales with the feature size. Hence for features close to the diffraction limit, the phase contribution due to feature edges will dominate the bulk contribution. Using a Transport of Intensity Equation (TIE) [4] based phase retrieval method, through-focus intensity data on the AIMS tool is used to recover the phase of OMOG and ATT-PSM contacts for various target CDs and polarizations. It is observed that while the bulk contribution causes phase ripples across the contact for large sizes, for feature size close to the diffraction limit phase due to edges/corners dominates. Further, to quantify mask parameters from recovered field at the wafer, a sparse 2D thin mask model is fit to the field using a simplex optimization algorithm. Here edge effects are solved for computationally by representing them as additive boundary layers on the thin mask, which are tuned computationally to fit the measured wafer field, feasible since the field is sparse within the pupil NA (has only a few non-zero orders). This allows for an extension of the CD-TIE to higher orders, since various thin mask parameters affect not just the tilt, but also higher order derivatives of the Bossung plot at the wafer. These thin mask parameters under certain conditions correspond to physical mask parameters, thus enabling a quantification of process window dependence on mask topographical parameters as a function of feature size.

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J. Opt. Soc. Am., 73 (1983), pp. 1434–1441

9985-18, Session 5

PMJ16 Best Student Poster: Observation results of actual phase defects using micro-coherent EUV scatterometry microscope

Hiraku Hashimoto, Tetsuo Harada, Hiroo Kinoshita, Takeo Watanabe, Univ. of Hyogo (Japan)

No Abstract Available

9985-50, Session PS1

Bottom layered attenuated phase-shift mask (PSM) blanks for flat panel display

Kagehiro Kageyama, Satoru Mochizuki, Yasunori Noguchi, Daisuke Nakamura, Shigeru Uchida, ULVAC Coating Corp. (Japan)

The flat panel display which have fineness vision are developed recently and the fine pattern making process are strongly needed.

Ulcoat have developed CrOx based phase shift mask (PSM) blanks for PSM of flat panel display.Several exposure processes are required for several patterns of flat panel display and PSM with opaque area is needed.

Ulcoat developed new bottom layered PSM blanks which consist of CrOx based phase shifting layer, etching stop layer which stop etching of phase shifting layer at opaque layer etching, Cr based opaque layer.

We report the basic construction and optical, chemical characteristics and patterning process of Ulcoat's new bottom layered PSM blanks.

9985-51, Session PS1

Prototyping 9-inch size PSM mask blanks for 450mm wafer process (2016)

Noriyuki Harashima, ULVAC Coating Corp. (Japan)

6-inch size (known as 6025QZ) binary Cr mask is widely used in the semiconductor lithography for over 20years. Recently for the 450mm wafer process, high grade 9-inch size mask is expected. For this application, we have studied and developed prototyping 9-inch size PSM KrF and ArF mask blanks.

This time we will explain these PSM mask blanks status.

9985-52, Session PS1

Evaluation of the properties of the permeability film material using cellulose nanofibers

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Dilution solvents and cracked gasses generated from resist materials cause transcriptional defects on template materials in UV nanoimprint lithography. This study aimed to create the novel gas permeable nanoimprint template materials to prevent transcriptional defects by dilution solvents and cracked gasses from nanopatterning materials. Gas transmission coefficient, light transmission rate, and hardness in cellulose nanofibers were evaluated for transparent template materials with thermal cross-link urethane groups. The approach to use the cellulose nanofibers into transparent template materials was expected to be suitable as the next generation of clean separation technology in nanoimprint lithography.

9985-53, Session PS1

Characterization and reduction of pellicle degradation due to haze formation on leading edge technology photomasks

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Since the adoption of deep ultraviolet lithography, time-dependent haze defects have become an increasingly significant problem for the semiconductor industry as photomask lifetime continues to be shortened due to molecular contamination. With shorter wavelength lithography, the materials and space between the pellicle film and photomask surface can create a highly reactive environment resulting in the formation of haze defects on the photomask. One critical issue has been to understand the chemical mechanism of evolving defects on the photomask triggered by haze formation.

This fundamental study was completed in a manufacturing environment in response to a sudden increase of haze defect growth during the transition to new device nodes. Several analytical approaches were carried out to understand the source and composition of the increased number of defects. Time of Flight Secondary Ion Mass Spectrometry (TOF-SIMS) and Atomic Force Microscopy (AFM) analysis techniques were essential in characterizing pellicle degradation in parallel with increased haze defect growth on the photomask surface. TOF-SIMS surface spectra revealed elevated amounts of ammonium (NH4) and sulfates (SO4) on the pellicle membrane consistent with haze formation constituents. AFM topographical scans within the suspected haze region confirmed the presence of defects on the pellicle membrane; these defects were reported as ~10-20 nm in diameter and ~5-7 nm in height. Having found increased levels of ammonium and sulfates with characteristic haze defects on susceptible areas of the pellicle membrane, further analysis was carried out to characterize the pellicle frame as a possible source. The pellicle frame was of interest due to its discoloration correlating to the time when a rapid increase in defects was detected on the photomask. TOF-SIMS was used to characterize the inside of the pellicle where the inner wall adhesive should be present for gettering airborne particles. The surface spectra and images collected from the frame indicated the inner wall adhesive had been completely removed in the discolored region.

The extensive chemical and surface topography characterization of pellicle degradation provided fresh insight into potential scenarios causing an increase in time-dependent haze formation and led to a vitally important development and implementation of a design change in the pellicle frame for Flash Memory 3x nm and 2x nm node critical process layer photolithography. With an increased clearance between the pattern design and pellicle edge, the design modification ultimately brought an immense increase in photomask dose limitation between repell cleans and a reduction in haze growth; thus, reducing production costs and increasing wafer throughput.

9985-86, Session PS1

7nm e-beam resist sensitivity characterization

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Over time mask makers have been driven to low sensitivity e-beam resist materials to meet lithography patterning needs. For 7-nm logic node, resolution enhancement techniques continue to evolve bringing more complexity on mask and additional mask builds per layer. As demonstrated in literature, low sensitivity materials are needed for low line edge roughness but impact write tool through put. In characterizing resist sensitivity for 7-nm, we explore more broadly what advantages and disadvantages moving to lower sensitivity resist materials brings, where line edge roughness, dose latitude, critical dimension uniformity, pattern fidelity, image placement, and write time results and trends are presented. We also acknowledge that new evolving paradigms of e-beam exposure have potential to allow faster write times with low sensitivity resists, including in-line write tool cleaning and multi-beam exposures, meaning that the boundary conditions of sensitivity expand. In this paper, resist material performance will be reported for sensitivities ranging from 20 μC/cm2 to 150 μC/cm2 at 50% proximity effect correction, where the exposure will be using a single beam platform. Materials examined include positive and negative tone resist types with and without chemical amplification focusing on overall trends for 7-nm e-beam resist performance.

9985-55, Session PS2

Mechanical stress induced by external forces in the extreme-ultraviolet pellicle

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Defects on a mask will cause serious problems for high resolution patterning below 1x nm. Using the pellicle is a good way to protect the extreme ultraviolet (EUV) mask against defects generated during the lithography process for high volume manufacturing (HVM). The EUV pellicle should be very thin due to high absorption of the EUV light with 13.5 nm wavelength. The thickness is only about 50 nm and it is much smaller than ~100 mm of full-size EUV pellicle recently suggested by ASML. For this reason, the pellicle would be easily affected by external forces such as gravity and stage acceleration. The pellicle would be deflected or torn by the residual stress during manufacturing and thermal stress during exposure.

In addition, the chamber-pellicle pressure difference would cause the mechanical deformation. In load lock chamber, the pressure is varied from atmospheric pressure to high vacuum environment. A filter located on the pellicle frame generates significant flow resistance, and the pressure difference between the gap of the pellicle-mask and outside is getting bigger. We investigated the maximum stress that can be induced by the pressure difference for various materials and structures by using finite element method (FEM). We also used theoretical model and FEM for predicting the pellicle deformation. Our results show the mechanical

deformation and the stress of full size (152 x 120 mm2) pellicle with 50 nm thickness, and the pressure difference should be less than 2 Pa if the deflection should be less than ~1 mm.

The pellicle can be also affected by the acceleration force of the scanner with shear direction during exposure process. Especially, maximum deformation and stress are dramatically increased when the pulse width of the scanner movement is the same as the resonance frequency of the pellicle. We studied the maximum stress for different acceleration pulse widths. The full size pellicle is greatly influenced with the specific pulse width causing resonance. As one can see the mechanical stress with acceleration is very small compared with the thermal stress so that it can be ignored.

9985-56, Session PS2

Investigation of fabrication process for sub-20nm dense pattern of non-chemically amplified electron-beam resist based on acrylic polymers

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In the case of the multi-beam mask writer with an acceleration voltage of 50 kV, a line- and-space (L/S) pattern resolution of 20 nm is required for next generation photomask fabrication. It is also necessary to form a semi dense pattern below 20 nm. Non-chemically amplified resists have good resolution compared to the CA resists, though the sensitivity is lower. We have reported that the thickness loss in the unexposed portions of the resist in the 20 nm L/S pattern is suppressed by increasing the molecular weight of the non-CA resist consisting of methyl α-chloroacrylate and ?-methylstyrene upto 500 k. This chemical structure resist possesses higher sensitivity and higher dry-etching resistance compared to poly-(methyl methacrylate) (PMMA) due to the existence of halogen unit and benzene ring. In this study, in order to form sub-20 nm dense patterns of acrylic polymer type electron beam resist, we examine exposure characteristics by changing the development process conditions. The effect of post exposure baking (PEB) is also investigated.

The synthesized copolymers were dissolved in anisole. The copolymer having the molecular weight of 500 k was mainly used. The film thickness spin-coated on a Si substrate was approximately 50 nm. After pre-baking at 180 °C for 2 min on a hot plate, L/S patterns with 40 nm and 35 nm pitches were exposed by the electron beam writing system with an acceleration voltage of 50 kV and a beam current of 25 pA.

The exposed samples were developed by amyl acetate at 0 ºC for 120 s as well as room temperature of 22.5 ºC for 60 s. In the 40 nm pitch pattern, the sensitivity drastically decreased from 160 μC/cm2 for development at room temperature to 260 μC/cm2 for development at 0 ºC. For the 0 ºC development, the pattern quality such as the surface roughness was improved, but the pattern collapse easily occurred compared with the room temperature development. Next, the resist was developed by heptyl acetate at 22.5 ºC for 60 s. The sensitivity of 240 μC/cm2 in the 40 nm pitch pattern was slightly higher and pattern quality was also better than those for development at 0 ºC by amyl acetate. For heptyl acetate, the 40 nm pitch pattern was formed from 240 to 280 μC/cm2 while the pattern was only formed at 160 μC/cm2 for amyl acetate (room temperature development). Miyoshi and Taniguchi have demonstrated that the PEB process in the non-CA resist is effective as an advanced fabrication technique for high resolutions of the order of 20 nm. We carried out PEB at 120 °C for 2 min on the hot plate. Though the sensitivity became lower by PEB, pattern shape was improved. The L/S pattern with 35 nm pitch can be successfully obtained by combining PEB and heptyl acetate developer. The exposure dose range for pattern formation was from 360 to 400μC/cm2 for the design value of 20/15 nm and was from 340 to 360 μC/cm2 for the design value of 17.5/17.5 nm.

9985-36, Session PS3

The study of CD side to side error in line/space pattern caused by post-exposure bake effect

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In semiconductor manufacturing, as the design rule has decreased, the ITRS roadmap requires crucial tighter critical dimension (CD) control. CD uniformity is one of the necessary parameters to assure good performance and reliable functionality of any integrated circuit (IC), and towards the advanced technology nodes, it is a challenge to control CD uniformity well.

The study of corresponding CD Uniformity by tuning Post-Exposure bake (PEB) and develop process has some significant progress, but CD side to side error happening to some line/space pattern are still found in practical application, and the error has approached to over the uniformity tolerance. After details analysis, even though use several developer types, the CD side to side error has not been found significant relationship to the developing. In addition, it is impossible to correct the CD side to side error by electron beam correction as such error does not appear in all Line/Space pattern masks. In this paper the root cause of CD side to side error is analyzed, and the PEB module process are optimized as a main factor for improvement of CD side to side error.

9985-57, Session PS3

Reticle inspection equipment productivity increase using SEMI specification for reticle and pod management

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In a high volume manufacturing fab, utilizing reticle inspection tools with full automation capabilities (e.g. Automated Material Handling System (AMHS), Fab full remote control tool through an Equipment Interface (EI) automation) is expected and required. It is also expected that full automation will require no manual intervention and allows reticle inspection tools to load and unload reticles and jobs in parallel with mask inspection for more efficient operation.

On KLA-Tencor's (KT) reticle inspection tools, the internal library is used as an intermediate storage location increasing utilization and throughput of the tool by reducing processing cycles (time) for loading/unloading of reticles. Integrating the equipment's reticle library with full automation functionality has been challenging due to the design, integration complexity, and subsequent test verification of capabilities that have not been previously available through automation in a production environment.

In this work, SEMI E109 (Specification For Reticle and Pod Management) with internal reticle library support has been integrated for the first time on KT's TeronTM and TeraScanTM reticle inspection tools. Simultaneous Manufacturing Execution System (MES) scheduling reticle jobs and AMHS scheduling to transfer pods have also been integrated and tested. Globalfoundries collaboratively worked with KLA-Tencor to successfully implement these capabilities.

With full automation enabled, operational efficiency has been substantially improved. Before automation was implemented operators had to:

- Manually move the reticles to the tools
- Manually set up the jobs in the tool job queue.
- Check tool status periodically ensuring inspections were executing as expected.
- Tasked to support several different tool types, and at times, sparsely

located in the fab and couldn't handle tool interrupts in real time.

Because of manual processes, tool interruptions, operator availability, this caused extended periods of tool idle time while waiting for manual intervention reducing fab and equipment operational efficiency. After SEMI E109 implementation including automating the use of the internal reticle library locations, the system is sufficiently robust to continue inspection of other reticles in the queue even when a job failure occurs preventing the current job from running. The job failure is automatically reported to the fab equipment interfaces (EI) and operators are automatically notified allowing for determination of immediately addressing the failure or postponing until resources are free (personnel and or equipment). Due to a full fab automation integration, the manual decision making / time availability is virtually eliminated, thus improving overall operational efficiency. Moreover, the extensive alarm suite allows fast and efficient diagnosis of tool or inspection issues. In Globalfoundries manufacturing environment, a significant throughput gain for the inspection tools has been realized.

9985-58, Session PS3

Deposition of super-micron particles for creating photomask calibration standards

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Electrostatic deposition of dry particles on wafers and photomasks is a proven method for creating calibration standards for inspection and metrology tools used in semiconductor manufacturing. A number of deposit attributes can be controlled precisely including particle diameter, particle material, particle count, pattern width, and pattern location. Historically, particle size standards such as PSL spheres, primarily smaller than 2 µm in diameter, have been deposited on wafers and photomasks. As semiconductor device features have decreased in size, inspection sensitivities have improved, and the minimum particle size that can be deposited with good control using commercial particle deposition systems has kept pace. PSL and silica particle monomers as small as 10nm can be routinely deposited with confidence.

New inspection applications are emerging with a focus on detection and measurement of super-micron particles, up to 100 µm in diameter. In advanced semiconductor manufacturing, super-micron particles on the backside of a wafer or photomask can adversely affect lithography due to distortion of the substrate from high-force chucking. Super-micron particles are also problematic during the manufacture of glass displays used in mobile devices, monitors, and televisions.

In this work, we present early results of a new large-particle deposition tool being developed at MSP for placing particles larger than 2 µm in a controlled manner on a silicon or glass surface. The forces needed for manipulation of large particles are quite different than those of small particles, thereby requiring a different set of particle devices to be developed and integrated. This new tool relies on a recently commercialized flow-focusing monodisperse aerosol generator and on traditional methods of particle size measurement and detection. If large-particle standards are to ever rival small-particle standards in terms of quality, one of the biggest challenges will be development of a size-classification device for removal of unwanted particle sizes, which almost always exist as byproducts of the particle generation process.

9985-60, Session PS3

Scanning coherent scattering methods for actinic EUV mask inspection

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Actinic mask inspection for EUV lithography with targeted specifications of resolution, sensitivity, and throughput is a big challenge and effective solutions are needed. We present a method for actinic mask inspection based scanning coherent scattering microscopy. In this method the EUV mask is scanned with an EUV beam of relatively small spot size and the scattered light is recorded with a pixel detector. Customized algorithms reconstruct the aerial image by iteratively solving the phase-problem using over-determined diffraction data gathered by scanning across the specimen with a finite illumination. It provides the actinic phase and amplitude aerial images of EUV masks with high resolution without the need to use high NA (numerical aperture) lenses. Contrary to scanning microscopy and full-field microscopy, where the resolution is limited by the spot size or NA of the lens, the achievable resolution with our method depends on the detector noise and NA of the detector. We have recently presented a reflective mode EUV mask scanning lensless imaging tool (RESCAN), which is installed at the XIL-II beamline of the Swiss Light Source and showed reconstructed aerial images down to 10 nm (on-wafer) resolution. As a complementary method, the a-priori knowledge of the sample is employed to identify potential defect sites already in the diffraction patterns. In this method, the recorded diffraction patterns are compared with the database (i.e. expected scattering data of the sample calculated from the mask layout) and their difference is interpreted as the defect signal. Dynamic software filtering helps to suppress strong diffraction from defect free structures and allows registration of faint defects with high sensitivity. Alternatively die-to-die comparison also enables identification of defect sites with high throughput and sensitivity. Here we discuss the challenges and the basic principles of the method. We present proof-of-principle experiments and our progress with our RESCAN tool and describe the feasibility of a stand-alone tool. We believe that the realization of our prototype marks a significant step towards overcoming the limitations imposed by methods relying on imaging optics and has the potential of providing an effective solution for actinic mask metrology.

9985-61, Session PS3

To repair or not to repair: with FAVOR® there is no question

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In the mask shop the challenges associated with today's advanced technology nodes, both technical and economic, are becoming increasingly difficult. The constant drive to continue shrinking features means more masks per device, smaller manufacturing tolerances and more complexity along the manufacturing line with respect to the number of manufacturing steps required. Furthermore, the extremely competitive nature of the industry makes it critical for mask shops to optimize asset utilization and processes in order to maximize their competitive advantage and, in the end, profitability.

Full maximization of profitability in such a complex and technologically sophisticated environment simply cannot be achieved without the use of smart automation. Smart automation allows productivity to be maximized through better asset utilization and process optimization. Reliability is improved through the minimization of manual interactions leading to fewer human error contributions and a more efficient manufacturing line. In addition to these improvements in productivity and reliability, extra value can be added through the collection and cross-verification of data from multiple sources which provides more information about our products and processes.

When it comes to handling mask defects, for instance, the process consists largely of time consuming manual interactions that are error prone and often require quick decisions from operators and engineers who are under pressure. The handling of defects itself is a multiple step process consisting of several iterations of inspection, disposition, repair, review and cleaning steps. Smaller manufacturing tolerances and features with higher complexity contribute to a higher number of defects which must be handled as well as a higher level of complexity.

In this paper the recent efforts undertaken by ZEISS to provide solutions which address these challenges, particularly those associated with

defectivity, will be presented. From automation of aerial image analysis to the use of data driven decision making to predict and propose the optimized back end of line process flow, productivity and reliability improvements are targeted by smart automation. Additionally the generation of the ideal aerial image from the design and several repair enhancement features offer additional capabilities to improve the efficiency and yield associated with defect handling.

9985-62, Session PS3

Actinic review of EUV masks: status of the AIMSTM EUV system

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For the successful introduction of EUV lithography into volume production, the EUV mask infrastructure is of key importance. One essential element for the production of defect free masks is the actinic review of potential defect sites. Based on actinic review the printability on wafer of a defect or a repaired defect can be determined. This verification can be performed within a closed loop mask repair solution with the MeRiT® electron beam repair tool. For the realization of actinic mask review, ZEISS and the SUNY Poly SEMATECH EUVL Mask Infrastructure (EMI) consortium started a development program for an EUV aerial image metrology system, the AIMS™ EUV.

In this paper, we provide an update on the system performance status within this program. Achievements from more than one year EMI program participants measurement campaigns on the prototype system will be provided.

9985-63, Session PS3

Loading effect correction set up and verification using inspection based CD measurements

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With semiconductor technology approaching and exceeding 10 nm design rules the quality requirements for photomasks are continuously tightening. One of the crucial parameters is improved photomask critical dimension (CD) control across the mask. As long as linearity and through pitch effects are not involved, the quality measure is typically defined as CD uniformity. This parameter is normally measured on repeating structures of same size and shape, which are not necessarily placed in identical environment.

Density depended process effects, also called loading effects (LE), pose a challenge on the required CD control. There are several possible contributors to this kind of error during a mask manufacturing flow, such as etch driven loading effects, fogging effects during 50kV exposure and develop driven loading effects. All of them operate at different working ranges, such as millimetres down to only a few 100 µm scale.

While it is comparably easy to derive models for large scale phenomena like etch loading or fogging effects, it is not as straight forward to find suitable models for very short range effects, which typically arise in the resist process area. A large amount of CD measurements taken by CD SEM is needed to identify such signals of low magnitude and short scales, which make the setup pretty resource intensive. Furthermore, this methodology requires artificial designs and test structures that try to sample only the effect of interest.

However, when it comes to verification, CD collection becomes very complicated. The verification of a model quality is usually not only performed on the artificial pattern as used for calibration, but also on real circuit designs. Since OPC is applying aggressive edge segmentation, these designs become almost impossible to (automatically) measure from a CD SEM perspective.

Optical mask inspection can offer a solution to this problem. State of the art, high resolution inspection systems share the capability to generate CD information during die-to-database inspections at no additional cost. This CD signal is available for every region of a mask at high spatial sampling resolution as small as 100 µm and is almost independent from pattern complexity.

We report a methodology that uses inspection based CD information to set up and verify a loading effect correction for various processes of record. The set up process stretches from inspecting test masks using suitable calibration test structures over deriving suitable models at various scales to verification of the model and correction capability on multiple customer layouts of different content and complexity. The inspection based set up and verification is supported by complementary CD SEM data where needed. Improvements for typical mask quality measures like global CD-uniformity are also verified via CD SEM, as this is the agreed quality measure for CD control.

9985-64, Session PS3

Improvement of photomask CD uniformity using spatially resolvable optical emission spectrometry

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According to design rule shrink, more precise control of CD uniformity is required in photomask manufacturing. Dry etching is believed to be the most critical process to determine the CD quality of photomask and Optical Emission Spectroscopy (OES) has widely been used to monitor and control the dry etching process.

However it is impossible to measure the radical distribution of plasma with conventional OES tool. The OES acquire totally integrated light from the plasma in process chamber. To measure the distribution of radicals in plasma during dry etch process, we studied Spatially Resolved Optical Emission Spectroscopy (SR-OES).

SR-OES consist of a series of lenses, apertures, and pinhole as a spatial filter enabled to focus on certain area in a chamber to extract the emitted light from plasma and to perform the spectroscopic analysis. To correct the systematic error in the SROES due to the geometry of the plasma source, we use the normalized signal of the SROES.

The Argon based actinometry combined with SR-OES showed that several specific peaks related to the etch rate of Chromium on photomask are spatially distinguished. Furthermore, it was possible to detect delicate change in radical distribution with chamber aging after wet clean. In this paper, we present the experimental application results of SR-OES installed on a commercial photomask dry etcher to monitor the radical distribution and its change in plasma and the practical effectiveness of SR-OES by showing the correlation with CD uniformity.

9985-66, Session PS3

Development of actual EUV mask observation method for micro-coherent EUV scatterometry microscope

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An EUV mask has 3-dimensional (3D) structure for EUV wavelength, which is reflective type and consists of glass substrate, reflective Mo/Si multilayer, and absorber pattern. In addition, phase structure on the blank mask is also

printable as a defect, which is bump or pit structure on the substrate or a particle in the multilayer. Since the 3D structure affects the reflective phase, a phase-imaging microscope of the EUV mask is important for EUV mask development.

We have developed a lensless EUV microscope of micro coherent EUV scatterometry microscope (micro-CSM) to observe EUV defects with quantitative phase and amplitude contrast. Micro-CSM records diffraction from a defect directly that is exposed with focused coherent EUV of 140-nm in diameter. The focusing optics is Fresnel zoneplate of off-axis type. Acceptance angle of the CCD camera is approximately ±16° (NA 0.27). With a coherent illumination, phase information is embedded in the diffraction signal. Using the diffraction signal, phase images of the phase defect is reconstructed by the coherent-diffraction-imaging method.

The diffraction signal from the defect was depended on the focusing size. A best focus condition of the zoneplate was required to detect small defect. At programmed phase defect observation, we focused the zoneplate with an alignment mark around the defect. However, actual EUV mask does not have such alignment mark. It is required to focus the zoneplate without any alignment mark. In this study, we developed a focusing method with a mask speckle. The speckle structure size was depended on the illuminated size on the EUV mask.

We will introduce the observation result of actual EUV defect with this new focusing method.

9985-88, Session PS3

Upgrading the SHARP EUV mask microscope for flux, cleanliness, and positioning accuracy

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The SHARP High-NA Actinic Reticle review Project, is an actinic, synchrotron-based microscope dedicated to extreme ultraviolet (EUV) photomask research.1 We are carrying out a number of upgrades to improve the performance of the tool in several important areas, including photon flux, mask handling and cleanliness, and stage position accuracy.

We have improved the photon flux by a factor of nearly 60x by re-aligning the beamline and replacing a multilayer-coated MEMS-mirror with improved optical properties. The increased flux allows us to fill the dynamic range of the CCD sensor in less than three seconds, producing data with greatly improved signal-to noise ratio. Noise-sensitive measurements like isolated defect and line-width-roughness can now be carried out without compromising throughput.

To promote clean mask handling, a mask robot has been added to SHARP, allowing automated loading and unloading of photomasks using SMIF pods. Contamination is minimized by eliminating all manual handling of photomasks and operating in a controlled mini-environment around the load-lock.

In the past, SHARP has used magnetic encoders on the six axes of the mask and zoneplate stages. The encoders were selected to avoid light contamination in the experimental chamber, but they suffer from systematic errors on the level of ±10 μm that complicate navigation to arbitrary, unmarked positions. We are installing infrared laser-interferometric encoders on the mask and zoneplate stages to improve the position accuracy to less than 1 μm. The lasers' 1.4-μm wavelength is below the detection energy of the EUV CCD camera. In many experiments, including small defects, and near-perfect repairs, the region of interest cannot be distinguished from its surroundings visually. The upgrade allows us to confidently, and automatically center the point of interest within the field of view.

Upgrades in flux, position accuracy and cleanliness of SHARP complement the optical capabilities and versatility of the tool, increasing the throughput and quality of the image data and expanding the range of possible experiments. The paper summarizes the technical aspects of the upgrades and resulting performance improvements. Examples of user experiments illustrate the capabilities of SHARP.

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9985-68, Session PS4

Defect inspection and printability study for 10nm node and beyond photomask

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Mask patterns are becoming more complicated, as a result, the defect specifications will concurrently become more severe. It follows then, that mask defect inspection is rapidly becoming one of the key technology components toward high-quality HVM (High Volume Manufacturing) for 10 nm node and beyond. To satisfy the requirement of significantly smaller defect sensitivity, two different inspection approaches were optimized and compared. The first approach is typical High-resolution inspection during which the reticle is compared directly to the design database using high-NA optics. The second approach is a Litho-based inspection which is the ideal inspection concept. Litho-based inspection may be able to detect and identify only the defects that impact wafer CD, because the inspection uses the similar illumination settings for image capturing as the wafer scanner. Both high-resolution and Litho-based inspection settings are optimized individually, and then defect sensitivity and inspectability are compared using 14, 10 and 7nm node production and programmed defect masks.

This paper will also focus on the defect printability on wafer. Defect printability is calculated using Litho-based inspection and compared with AIMSTM (Aerial Image Measurement System).

Finally the best inspection approach will be discussed based on those results.

9985-69, Session PS4

Reticle decision center: a novel application platform for enhanced reticle yield and productivity for 10nm technology and beyond

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In the IC industry, challenges associated with photomask manufacturing have dramatically increased at the 1X nm technology nodes. Some of the top challenges include larger costs associated with increasing numbers of layers per device while at the same time most mask process related parameters show much lower signal-to-noise due with increased mask pattern complexity. With the cost and complexity to qualify defect-free masks higher than ever before, it is crucial to optimize productivity in every possible way.

The Reticle Decision Center (RDC) combines a highly reliable server architecture with novel software applications that operate in sync with

reticle inspection, repair, and metrology tools and effectively enhance their output by automating a lot of manually intensive operations. In addition to enhanced productivity, the RDC includes applications that improve signal-to-noise of mask defect inspection and metrology tools – examples include enabling higher-sensitivity inspections with Automated Defect Classification and wafer print impact estimation, and enabling more complex repairs by computing defect-free regions for mask repair and AIMS tools.

In this paper we summarize our findings on the benefits that RDC applications bring to mask defect yield, operator productivity, and cycle-time reduction.

9985-70, Session PS4

EBL2: high-power EUV exposure facility

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TNO is building EBL2: a laboratory EUV exposure system capable of operating at high broad band EUV powers and intensities, in which XPS analysis of exposed samples is possible without breaking vacuum. The system architecture is similar to the EUV Beam Line (EBL) which has been operated jointly by TNO and Carl Zeiss SMT since 2005 (see Proc. SPIE 9235, Photomask Technology 2014, 92351F (October 8, 2014); doi:10.1117/12.2083713). Its goal is to accelerate the development and testing of EUV optics, EUV photomasks, EUV pellicles, and general components for use in EUV systems by providing a publicly accessible exposure and analysis facility.

The EBL2 design contains a Beam Line, an XPS system and automatic sample handling. In the Beam line, samples can be exposed to EUV radiation in a controlled, representative environment for extended periods, to address lifetime questions. Compared to the existing EBL system, large improvements in EUV power, intensity, metrology, reliability, and flexibility are achieved. The system can accept a range of sample sizes, including standard EUV reticles with or without pellicles. This contribution will describe the design of the EUV beam line for mask exposures.

The Sn fueled Laser Discharge Plasma EUV source is provided by Ushio, Inc. It will provide high power EUV radiation to the Collector module, and low power EUV to a separate metrology port. The Collector module contains a two stage collector with an intermediate focus; the intermediate focus enables an effective vacuum separation between the EUV source and the Exposure chamber. The EUV spectrum emitted by the EUV source can optionally be filtered using membrane filters. The EUV spot on the sample can be tuned by a defocusing mechanism. Dedicated sensors monitor the EUV power output at source level continuously.

The Exposure chamber provides a clean background vacuum, to which several process gases can be added. Contaminants such as additional water, air, or hydrocarbons can be added in a controlled way. The Exposure chamber contains a thermally controlled sample stage with a wide range of possible temperature settings. Attached to the stage are EUV power and spot profile sensors measuring at sample location. The stage enables exposure of any spot on the sample or photomask. Photomasks or sample holders can be loaded onto the chuck from the sample handler using dedicated hardware. An in-situ ellipsometer enables real time monitoring of sample condition during EUV exposure. Additionally, it provides measurements to verify alignment of the sample and the EUV beam, and therefore also overlay between consecutive EUV exposures.

The automated sample handling infrastructure accepts SEMI standard dual pods, and maintains NXE compatibility for backside particle contamination. EBL2 also contains an XPS system capable of analyzing EUV masks, including pellicles (described in SPIE pmj100-13). The XPS is capable of handling reticles for analysis after irradiation without breaking vacuum to ensure optimal surface sensitivity.

9985-71, Session PS4

Comparing raw versus Manhattan ILT shape efficacy on EPE and process window

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Inverse Lithography Technology (ILT) is gaining acceptance as part of a comprehensive OPC solution especially as a repair technique to locally improve process window where conventional OPC does not have enough degrees of freedom to produce acceptable results. Since ILT is significantly more computationally intensive than conventional OPC, a localized application of ILT does not significantly increase OPC cycle time. As ILT methods mature and become more efficient, combined with the availability of huge compute clusters for post tape out data processing, the possibility of full-field ILT OPC could soon become reality. Full-field ILT OPC may provide improved process window and greater layout flexibility as long as multi-patterning methods with 193 nm exposure wavelength remain the primary lithography strategy for advanced technology nodes.

Due to limitations of photomask lithography tools that prevent efficient exposure of non-Manhattan shapes, ILT OPC output is typically post-processed to conform to mask MRC rules, rendering the raw all-angle features to a Manhattanized equivalent. Previous comparisons of raw vs Manhattan ILT OPC at earlier nodes have shown that a Manhattanized output can be made to print on wafer with equivalent process window while conforming to mask manufacturing rules.

In this paper we use wafer-level lithography simulation to compare raw vs Manhattanized ILT output based on current advanced nodes and MRC rules. We expand this study to include a mask model to ensure that mask corner rounding effects are considered.

9985-89, Session PS4

Wafer hot-spot identification through advanced photomask characterization techniques

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As device manufacturers progress through advanced technology nodes, limitations in standard 1-dimensional (1D) mask Critical Dimension (CD) metrics are becoming apparent. Historically, 1D metrics such as Mean to Target (MTT) and CD Uniformity (CDU) have been adequate for end users to evaluate and predict the mask impact on the wafer process. However, the wafer lithographer's process margin is shrinking at advanced nodes to a point that the classical mask CD metrics are no longer adequate to gauge the mask contribution to wafer process error. For example, wafer CDU error at advanced nodes is impacted by mask factors such as 3-dimensional (3D) effects and mask pattern fidelity on sub-resolution assist features (SRAFs) used in Optical Proximity Correction (OPC) models of ever-increasing complexity. These items are not quantifiable with the 1D metrology techniques of today. Likewise, the mask maker needs advanced characterization methods in order to optimize the mask process to meet the wafer lithographer's needs. These advanced characterization metrics are what is needed to harmonize mask and wafer processes for enhanced wafer hot spot. In this paper, we study advanced mask pattern characterization techniques and their correlation with modeled wafer performance.

9985-72, Session PS5

Defect management on photomasks with dry treatment assistance

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One of the key challenges of photomask manufacture is to achieve defect-free masks. Clean and repair has been applied to manage defects and particles on the mask imported during manufacturing processes. Since photomask patterns become smaller and more complicated as integrated circuit (IC) scaling to 28 nm node and below, the increasingly importance of mask quality compels us continuously research on more effective defect treatment solutions, to achieve mask yield enhancement and on-schedule delivery.

In this paper, we would like to introduce new approaches of defect management with dry treatment assistance, according to particular defect types. One is using plasma etching gases of Cl2/O2 to change the properties of glue compounds adhering to the mask surface, and make them removed by conventional cleaning. Another is the application of O2 plasma dry treatment for the benefit of alleviation on scan damage phenomenon, which comes from contamination on the scan area due to excessive repair cycles.

9985-73, Session PS5

Carbon dioxide gas purification and analytical measurement for leading-edge mask and wafer cleaning

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Supercritical carbon dioxide provides a very valid alternative for cleaning integrated circuits and masks having the physical characteristics of both a liquid and a gas: like a gas, it diffuses rapidly, has near zero surface tension, very low viscosity and thus penetrates easily into mask features or deep wafer trenches and vias. As a liquid it can be utilized to wash out particles and to solvate other chemicals such as alcohols and fluorinated hydrocarbons.

End users and tool manufacturers typically use very costly 6.0 N CO2 grade and compress the gas prior the cleaning tool. In addition to the high cost of the CO2 source there is an on-going issue with maintaining the ultra-high purity because there is no control of the hydrocarbon impurities. This hydrocarbon contamination is a result of the internal compressor components and is often invisible to the end user because of a lack of online gas analysis.

The most widely available and somewhat consistent (in terms of impurity level) type of carbon dioxide is 3.0 N beverage grade. Beverage grade CO2 is purified to a level as to not add any taste, odor, or carcinogens (such as benzene) to the consumer food products it is added too. Even with this level of regulation the level of condensable hydrocarbons and refractory compounds can vary significantly. The variation in impurity levels is a direct result of the wide variety of carbon dioxide sources utilized in beverage grade production (such as ethylene oxide production, coal gasification, combustion processes, and many others) along with impurities added in the compression/storage process. Table 1 shows the analysis of several different beverage grade samples. SAES Pure Gas has developed specific purification and compression technologies for CO2 cleaning starting from readily available and cost effective 3.0 N Beverage Grade CO2.

This paper covers the analytical tests and characterizations carried out to compress and assess impurity removal from 3.0 N Beverage Grade CO2 for its final utilization in mask and wafer cleaning applications. Full characterization of the purifier and the compressor was carried out monitoring the impurity concentrations at the inlet and outlet of the device and, as an example, Table 2 shows the results obtained while supplying it with beverage 3N grade CO2.

9985-74, Session PS5

Acoustic characterization of two megasonic devices for photomask cleaning

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Wet photomask cleaning relies on megasonic agitation to enhance the process, but there are many challenges to reliably control performance in terms of particle removal efficiency (PRE) and damage. With the shift to pellicle-free EUV masks, photomask processes are more vulnerable to contamination. This gap exists largely because of the unavailability of appropriate measurement of the acoustic field. Typically all that is specified about the acoustic output is the driving frequency and the electric power delivered to a transducer. However, the efficiency of the transducer and the distribution of acoustic waves remain unknown and therefore uncontrolled. Understanding how the acoustic waves interact with the substrate is essential to optimize cleaning, and this knowledge is becoming accessible with new measurement methods like the ones presented here.

Two different megasonic devices were considered. One is a novel design consisting of a transducer coupled to a tilted, truncated quartz cone with a flat surface that hovers over the substrate, leaving an elliptical footprint of about 4 x 6 cm. It is coupled with the substrate by cleaning fluid infused through the cone. The second device is a more traditional spot shower that couples a transducer nozzle above the substrate by a smooth jet of cleaning fluid, 4 mm in diameter.

Both transducer configurations were characterized by various methods. A hydrophone was used to directly measure the acoustic field and the two forms of cavitation, stable and transient, which have been shown to closely relate to cleaning efficiency and damage. Hydrophone scanning allowed mapping the pressure distribution and determining the transducer electro-acoustic efficiency. In addition, a sensor embedded in a photomask was used to characterize the acoustic field in the presence of a quartz plate. Finally, schlieren imaging was used to capture the wave propagation behavior between the transducer and the photomask.

The conical device presents a diffuse and irregular field with slight stable cavitation and no observable transient cavitation, as could be expected from a spread source. However, when analyzed in a Schlieren system, a sweeping effect due to the interference of the reflected waves is evident, as can be seen in the slow-motion video recording to be presented. This brush-like sweeping effect is likely a major contributing factor in cleaning.

On the other hand, the spot shower device presents a concentrated field of several atmospheres of pressure in a confined area, more than sufficient to cause cavitation, yet it shows a moderate amount of stable cavitation and a negligible amount of transient cavitation.

The performance of each device is analyzed vis-a-vis its potential to clean and/or cause damage, and a call is made to start correlating PRE and damage to these measurable parameters. This work demonstrates a better understanding of the important acoustic factors in a cleaning system, with great application potential in optimizing megasonic cleaning systems.

9985-76, Session PS6

Auto-score system to optimize OPC recipe parameters using genetic algorithm

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The ever increasing pattern densities and design complexities make the tuning of optical proximity correction (OPC) recipes more challenging. There are various recipe tuning methods to meet the challenge, such as genetic algorithm (GA), simulated annealing, and vendor provided recipe optimizers. However, these methodologies usually only consider edge placement errors (EPEs). Therefore, these techniques may not provide adequate freedom to solve the unique problems at special geometries, for example bridge, pinch, and process variation band related violations at complex 2D geometries.

This paper introduces a general methodology to fix specific problems identified at the OPC verification stage and demonstrates its successful application to three test-cases. The algorithm and method of the automatic scoring system is introduced in order to identify and prioritize the problems that need to be fixed based on severity, with the POR recipe score used as the baseline reference. A GA optimizer, whose object function is based on the scoring system, is applied to tune the OPC recipe parameters to optimum condition after generations of selections. The GA optimized recipe would be compared to existing recipe to quantify the amount of improvement.

This technique was subsequently applied to eliminate certain chronic OPC verification problems which were encountered in the past. Though the benefits have been demonstrated for limited test cases, employing this technique more universally will enable users to efficiently reduce the number of OPC verification violations and provide robust OPC.

9985-77, Session PS6

Calibrating accurate MPC models on a reduced set of mask measurements

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Accurate mask modeling is the corner stone of any mask proximity effect correction (MPC) method and any correction method can only be as good as the underlying model.

The need for accurate mask models under a wide range of conditions including line and space CDs, pattern densities, VSB shot dose levels, and complex pattern shapes down to the resolution limit easily drives the number of mask measurements required to calibrate such a comprehensive model into a range of several thousand. Such a high number of metrology points constitutes considerable cost and adds significantly to model development time.

In this paper we demonstrate accurate mask model calibration on a reduced number of metrology points. By selecting a sparse matrix from the entire pattern variation space, we are able to reduce the number of metrology points below 150. Sparse sampling of the pattern space is possible due to the characteristics of mask errors which are mostly of Gaussian form. Unlike wafer models for OPC which have to deal with interference and therefore fast changing signals at small pattern variations, mask models have to describe relatively smooth and slowly changing signals.

When reducing the number of measurements those measurements have to capture as much information about the mask model as possible. We achieve this by including two important aspects of a mask model, namely its through-dose behavior and 2D corner rounding. Several features are measured at various dose levels so that the delta CD through-dose behavior is captured. In addition, we include a significant number of 2D measurements which are all taken by averaging the CD inside a measurement box. This method is more sensitive to mask corner rounding than just measuring the center CD of a 2D shape and therefore provides additional information about corner rounding.

The method described above is demonstrated for various models for DUV and EUV masks.

9985-78, Session PS6

OPC model sampling evaluation and weak point in-situ improvement

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One of the major challenges of optical proximity correction (OPC) models is to maximize the coverage of real design features using sampling pattern. Normally, OPC model building is based on 1-D and 2-D test patterns with systematically changing pitches alignment with design rules. However, those features with different optical and geometric properties will generate weak-points where OPC simulation cannot precisely predict resist contours on wafer due to the nature of infinite IC designs and limited number of model test patterns. In this paper, optical property data of real design features were collected from full chips and classified to compare with the same kind of data from OPC test patterns. Therefore sample coverage could be visually mapped according to different optical properties. Design features, which are out of OPC capability, were distinguished by their optical properties and marked as weak-points. New patterns with similar optical properties would be added into model build site-list. Further, an alternative and more efficient method was created in this paper to improve the treatment of issue features and remove weak-points without rebuilding models. Since certain classification of optical properties will generate weak-points, an OPC-integrated repair algorithm was developed and implemented to scan full chip for optical properties, locate those features and then optimize OPC treatment or apply precise sizing on site. This is a named "in-situ" weak-point improvement flow which includes issue feature definition, allocation in full chip and real-time improvement.

9985-79, Session PS6

Suppressing rippling with minimized corner rounding for an asymmetric pixelated source through OPC fragmentation optimization

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As technology shrinks, the requirements placed on the post-OPC solution become so exacting that even small residual optical effects are significant. Simultaneously minimizing rippling and corner rounding cannot be realized in parallel in wafer patterning especially when using complex asymmetric pixelated sources. While either effect can be moderated by accurate application of optical proximity correction (OPC), they are both characteristic of unfiltered diffraction due to asymmetric illumination or design geometry and will remain inherent. Corrections that over emphasize reduced corner-rounding necessarily sacrifice edge convergence, resulting in a standing wave or unacceptable rippling along an entire edge. OPC can be used to reduce the magnitude of rippling, but fragment placing is extremely critical. In this paper, we discuss optimized OPC fragmentation that offers balanced consideration to suppressing rippling and minimizing corner rounding. Specifically, we correlate design shape with simulated post-OPC contour to account for design geometry-dependent rippling signature given existing illumination conditions. In contrast to adaptive fragmentation that relies on multiple iterations of simulation of intensity extrema redistribution, our method predicts the optimum contour as allowed by process and fragments accordingly. The maximum imaging curvature resolvable by process coupled with the rippling signature, gives rise to the exact locations of the inflection points of the wafer contour. From there we achieve the best correction results by segmenting edges at the inflection points.

9985-80, Session PS6

Verification flow of model-based fracture output

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The demands of 20nm and smaller technology nodes are making it difficult for the mask manufacturing process to keep up. On the one hand, shrinking features and the increasing complexity of OPC make controlling mask errors much more difficult even as the Mask Error Enhancement Factor (MEEF) amplifies their impact on the wafer. On the other hand, these smaller and more numerous features drive a large increase in the exposures needed per mask, thus increasing mask write times. This increasing complexity is especially acute for Inverse Lithography Technology (ILT) masks, as the pattern will either contain curvilinear features that are very costly to expose with the VSB mask writers, or if "manhattan-ized", will still contain a large number of small jogs reducing process window and increasing the write times to some extent.

One solution to these issues is to abandon strict geometric correctness when fracturing, and instead use a model of the electron beam manufacturing process to generate shots of various sizes and control the placement of these shots to achieve the desired contour on the mask. Such an intentional discrepancy between post-OPC layout and the layout actually written by the electron beam exposure tool means that a simple XOR verification based on strict geometric correctness of the MDP output is no longer possible. This paper describes a model-based verification flow instead of the traditional XOR verification.

9985-81, Session PS6

Combining mask and OPC process verification for improved wafer patterning and yield

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As technology advances into deep submicron nodes, the mask manufacturing process accuracy and reliability become more important. Mask process correction has been transitioning from rules-based process correction into Model-Based Mask Process Correction (MPC). MPC is a subsequent step to OPC, where additional perturbation is applied to the mask shapes to correct for the mask manufacturing process. Shifting towards full model-based MPC is driven mainly by the accuracy requirements in advanced technology nodes, both for DUV and EUV processes.

In the current state-of-the-art MPC process, MPC is completely decoupled from OPC, where each of them assumes that the other is executing perfectly (within a range of acceptable variations. However, this decoupling is not suitable anymore due to the limited tolerance in the mask CDU budget and the increased wafer CDU requirements required from OPC. It is becoming more important to reduce any systematic mask errors, especially where they matter the most.

In this work, we present a new combined-verification methodology that allows testing the combined effect of mask process and lithography process together and judging the final wafer patterning quality. This has the potential to intercept risks due to OPC and MPC correction residues superposition, and capturing such a previously hidden source of patterning degradation.

9985-82, Session PS7

Fundamental study of green EUV lithography using natural polysaccharide for the use of pure water in developable process

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An approach of natural polysaccharide to green resist polymers in extreme-ultraviolet (EUV) and electron beam (EB) lithography has successfully achieved for the use of pure water in the developable process of mask application, instead of conventionally used tetramethylammonium hydroxide and organic solvents. The green resist material with adjusted weight-average molecular weight and hydroxyl groups as a water-developable property was found to have the acceptable properties such as spin-coating properties on 200 mm wafer, prediction sensitivities of EUV at the wavelength of 6.7 and 13.5 nm, a high contrast of water dissolution rate before and after EB irradiation, and line patterns with sub-100 nm in high EB sensitivity of 15 microC/cm2.

9985-83, Session PS7

Approach of UV nanoimprint lithography using template with gas-permeable and gaseous adsorption for reduction of air-trapping issue

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The key issue of fabricating the next generation devices using the UV nanoimprint lithography with continuous multiple shots is the template material of minimizing air-trapping. New approach of UV nanoimprint lithography using a porous template with gas-permeable or gaseous adsorption is needed for reduction of air-trapping issue before introduction into a manufactability of the various applications required for high-accuracy printing and well-defined nanoscale patterning. The porous template shows excellent properties of resolution and UV nanoimprint lithography cycles compared with PMDS template.The chemical design of UV cross-linked materials and the processes required multiple functions and cost reduction are beneficial for various device applications using UV nanoimprint lithography.

9985-84, Session PS7

Production and evaluation of measuring equipment for share viscosity of polymer melts included nanofiller with injection molding machine

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A template material for nano-imprint substrate using the natural fiber mainly composed of nanofibers composed primarily of glucose was manufactured. As for the template material, it is wished it is low viscosity coefficient at geometry incorporation for transferal of the minute geometry. However, as for the template, it is needed tensile strength with the solid state. The properties of matter observation is important, but, in such a new material, the measuring apparatus is not set up very much. The quality in the liquid of provided nano-imprint substrate material did not follow the Cox-Merz law. The device which measured the rheology properties of matter as material property of the templates was produced. Therefore the plasticization device

of the injection molding machine was utilized and produced capillary type shear viscosity measuring apparatus. Rheological property of the nanobacking to imprint and geometry formativeness are reported.

9985-85, Session PS7

High-performance fabrication process for 2xnm hole-NIL template production

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UV nano imprint lithography (UV-NIL) has high-throughput and cost-effective for complex nano-scale patterns and is considered as a candidate for next generation lithography tool. In addition, NIL is the unmagnified lithography and contact transfer technique using template. Therefore, the lithography performance depends greatly on the quality of the template pattern.

According to ITRS 2013, the minimum half pitch size of Line and Space (LS) pattern will reach 1x nm level within next five years. On the other hand, in hole pattern, half pith of 2x nm level will be required in five years. Pattern shrink rate of hole pattern size is slower than LS pattern, but shot counts increase explosively compared to LS pattern due to its data volume. Therefore, high throughput process is especially needed as well as high resolution. Some results of this development have been reported recently.

After making trial test pattern, technically critical point moves to its quality control from the view point of commercial products. Then we focused on three important quality factors as it is called low defect density, CD uniformity(CDU), and Image placement(IP). We evaluated those three factors by using complicated layout patterns which include various surrounding density. VSB type EB writer EBM9000 was used to form 2xnm level hole. Because it can allocate appropriate EB dose for local region even if there is less contrast due to wide gap of coverage. That contributes to low defect density as reported previously. Besides that we control CDU and IP in this time. Regarding CD measurement, we have to take care not only for 2-dimentional value but also 3D's such as side wall profile or depth. Because of contact process, success of NIL printing strongly depends on it. Then we employed newly developed GI-SAXS method for measuring 3D shape of hole pattern. It was found to be so useful for guarantee 3D shape. Consequently we can show the readiness for manufacturing master template in mass production period.

9985-19, Session 6

The CD control improvement by using CDSEM 2D measurement of complex OPC patterns

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As the process node becomes more advanced, the accuracy and precision in OPC pattern CD are required in mask manufacturing. CD SEM is an essential tool to confirm the mask quality such as CD control, CD uniformity and CD mean to target (MTT).

Unfortunately, in some cases of arbitrary enclosed patterns or aggressive OPC patterns, for instance, line with tiny jogs and curvilinear SRAF, CD variation depending on region of interest (ROI) is a very serious problem in mask CD control, even it decreases the wafer yield. For overcoming this situation, the 2-dimensonal (2D) method by Holon is adopted. In this paper, we summarize the comparisons of error budget between conventional (1D) and 2D data using CD SEM and the CD performance between mask and wafer by complex OPC patterns including ILT features.

9985-20, Session 6

YieldStar based reticle 3D metrology and applications

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YieldStar (YS) is well established in its capability to measure wafer Critical Dimension (CD), Overlay and Focus. In a recent work, the application range of YS was extended to measure 3D CD patterns on reticles (absorber CD, height, Side Wall Angle). The primary motivation for this study came from imaging studies that indicated a need for measuring and controlling mask 3D topography1.

CD scanning electron microscope (CD-SEM), Atomic force microscope (AFM), 3D multiple detector SEM (3D-SEM) are the preferred tools for reticle metrology. While these tools serve the industry well, the current research to the impact of mask 3D involves extensive costs, logistic challenges and increased reticle lead time.

YS provides an attractive alternative as it can measure absorber CD, SWA and height in a single measurement and at high throughput. Multiple EUV imaging reticles were measured. YS performance is well within specifications set for tools to measure reticles for imaging related studies at ASML (Table 1). This performance places YS as a means to investigate reticle induced effects for applications that require high precision data.

While the measured CD and absorber height across multiple pitches confirmed the designed CD variation and a tight absorber height control, SWA change of 4-5 through pitch was observed (Figure 3). These measurements give a good insight into the topography variations across multiple features and can be used as input for a range of simulations and applications.

Latest results on smaller LS features and outlook on the impact of YS mask 3D metrology on wafer level CDU performance and other applications will be given in this presentation.

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9985-21, Session 6

Total effective EUV reticle distortion budget analysis and assessment of gains through industry adoption of write compensation for reticle flatness

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As the semiconductor industry continues to strive towards high volume manufacturing for EUV, flatness specifications for photomasks have decreased to below 10nm for 2018 production, however the current champion masks being produced report P-V flatness values of roughly ~50nm. Write compensation presents the promising opportunity to mitigate errors through the use of geometrically adjusted target patterns which counteract the reticle's flatness induced distortions and address the differences in chucking mechanisms between write and scan. Topographic features which lack compensation capability must then be held to stringent specifications in order to limit their contributions to the final image placement error (IPE) at wafer. By understanding the capabilities and limitations of write compensation, it is then possible to shift flatness requirements towards the "non-correctable" portion of the reticle's profile, potentially relieving polishers from having to adhere to the current single

digit flatness specifications. Compensation relies on high accuracy flatness data which provides the critical topographical components of the reticle to the write tool. Any errors included in the flatness data file are translated to the pattern during the write process, which has now driven flatness measurement tools to target a 6? reproducibility <1nm.

This study investigates the repeatability of flatness measurements of substrates and blanks provided by multiple manufacturers. We perform an evaluation of additional known process error contributors such as exposure tool, reticle fabrication, and e-beam write, and provide a total reticle distortion budget analysis. From this distortion budget, we demonstrate the current state of the industry with respect to the 2018 overlay targets both with and without write compensation. The conclusions drawn from this investigation seek to highlight areas which require further exploration and new empirical data.

9985-22, Session 6

Take a bite out of MEEF: VAMPIRE (vehicle for advanced mask pattern inspection readiness evaluations)

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MEEF is simply defined as the ratio of the change in printed wafer feature width to the change in mask feature width. It is an important component of chip manufacturing that often leads to the amplification of mask errors as it impacts the printed wafer image. As MEEF becomes more challenging, the need for increased mask defect sensitivity in high-MEEF areas becomes more and more critical.

There are multiple approaches to mask inspection that may…or may not provide enough sensitivity to detect all wafer-printable defects, while simultaneously maintaining an acceptable level of mask inspectability. The higher the MEEF…the harder the challenge will be to achieve that level of sensitivity…and to do so on the geometries that matter.

The predominant inspection systems in use today compare the reticle directly with the design database using high-NA optics. This approach has the ability to detect small defects, however, when inspecting aggressive OPC, it can lead to the over-detection of inconsequential nuisance defects. Global desense can improve the inspectability of a mask inspected in high-NA mode, however, it leads to the inability to detect subtle, yet wafer-printable defects in High-MEEF geometry. There are also 'lithographic' approaches to inspection that use various means to provide high defect sensitivity and the ability to tolerate inconsequential, non-printing defects by using scanner-like conditions to determine which defects are wafer printable.

Regardless of how the defects are detected, the real question is when should they be detected? For larger technology nodes, defects are considered 'statistical risks'…i.e., first they have to occur, and then they have to fall in high-MEEF areas in order to be of concern. In short, the 'perfect storm' had to happen in order to miss printable defects using well-optimized traditional inspection approaches. The introduction of lithographic inspection techniques has revealed the statistics game is a much higher risk than originally estimated, in that very subtle wafer-printable CD errors typically fall into the desense band for traditional reticle plane inspection. Because printability is largely influenced by MEEF, designs with high-MEEF values are at greater risk of traditional inspection missing printable CD errors. The question is… how high is high… and at what MEEF is optical inspection at the reticle plane sufficient? This paper will provide evaluation results for both reticle-plane and litho-plane inspections as they pertain to varying degrees of MEEF. A newly designed high-MEEF programmed defect test mask, named VAMPIRE, will be introduced. This test mask is based on 7 nm node technology and contains varying degrees of MEEF as well as a variety of programmed defects in high-MEEF environments…all of which have been verified for defect lithographic significance on a Zeiss AIMSTM system.

9985-23, Session 6

Die to database reticle inspection: a new approach to data-prep optimization

Patrick LoPresti, KLA-Tencor Corp. (United States)

Mask inspection has been using legacy formats derived from the MEBES files format for the past couple of generations. With increasing complexity and higher density of OPC correction features driving up the number of polygon figures in mask designs, files sizes are becoming very large especially after fracture. Post fracture database sizes of > 1TB are becoming common place. This creates challenges for file transfer rates, Masks data preparation times for mask inspection which can have an impact overall cycle times for mask manufacture and also IT infrastructure due to the required bandwidths to transfer files.

This paper explores the development of new pre inspection data processing techniques and hardware, central to this is using modern native formats such as industry standard OASIS which is very efficient and compact format, further to this, OASIS enables multilayer and multi data types which can enable new applications in mask inspection. Using such data rich formats also enables new inspection technologies and techniques, such as Dual imaging and advanced high resolution RPI inspection modes. This technology can also pave the way for database driven sensitivity control applications for mask inspection In this paper we demonstrate that we can significantly reduce the files sizes to be consumed and optimize the pre inspection data-prep times.

9985-24, Session 7

Recent efforts in EUV mask fabrication toward high-volume manufacturing

Guojing Zhang, Ted Liang, Srinath Satyanarayana, Sambit Misra, Kishore K. Chakravorty, Su Xu, Seh-Jin Park, John F. Magana, Yongbae Kim, Intel Corp. (United States)

Establishment of the EUV mask infrastructure and steady progress of the EUV mask fabrication have been made and recognized in the recent years. The EUV mask process is now in a transition from its pilot-line to high volume manufacturing. In a preparation for EUV insertion into advanced technology nodes, requirements of EUV mask yield improvement, productivity and cost control become a center focus in addition to the integrated mask performance.

In this paper, we will start with understanding of requirements of the EUV mask fabrication with a desire of many-to-1 replacement of 198i masks and complementary EUV/193i patterning, following a discussion of strategies and solutions of critical process modules in the EUV mask fabrication. Efforts to ensure mask quality and results of defect-free masks for wafer fab will be showed. Lastly we will address remaining challenges especially in pellicle implementation and reticle protection from particles.

9985-25, Session 7

Mask manufacturing of advanced technology designs using multi-beam lithography, part II

Michael Green, Photronics, Inc. (United States); Daniel Chalom, IMS Nanofabrication AG (Austria)

As optical lithography is extended into 10nm and below nodes, advanced designs are becoming a key challenge for mask manufacturers. Techniques including advanced optical proximity correction (OPC) and Inverse Lithography Technology (ILT) result in structures that pose a range of issues across the mask manufacturing process. Among the new challenges are continued shrinking sub-resolution assist features (SRAFs), curvilinear SRAFs, and other complex mask geometries that are counter-intuitive

relative to the desired wafer pattern. Considerable capability improvements over current mask making methods are necessary to meet the new requirements particularly regarding minimum feature resolution and pattern fidelity. Advanced processes using the IMS Multi-beam Mask Writer (MBMW) are feasible solutions to these coming challenges. In this paper, Part 2 of our study, we further characterize an MBMW process for 10nm and below logic node mask manufacturing including advanced pattern analysis and write time demonstration.

9985-26, Session 7

Enabling defect-free masks for EUV high-volume manufacturing by e-beam repair

Thorsten Hofmann, Hendrick Steigerwald, Tristan Bret, Klaus Edinger, Carl Zeiss SMT GmbH (Germany)

It may be extremely difficult to manufacture EUV blanks entirely free of multilayer defects when EUV ramps-up to HVM. Whereas absorber pattern complexity and defect density on the EUV mask limit the application of pattern shift, Compensational Repair offers a reliable method to make multilayer defects of typical size “non-printing”. Inspection data of an EUV mask with 27-nm-half-pitch vertical lines and spaces and in-situ AFM technology of the MeRiT mask repair tool are used to locate and characterize the multilayer defects. After e-beam modification of the absorber the significant reduction of the CD variation is verified by through-focal actinic imaging emulating state-of-the-art EUV scanner technology and by AFM-imaging. To improve the results a second approach of absorber reshaping is done based on the more AFM data containing more defect information. This yields even more reduction of the CD variation and demonstrating “rework capability” to iteratively and reliably compensate multilayer defects.

9985-27, Session 7

The costs of masks: hiding or revealing the real solution

Michael J. Lercel, ASML Fishkill (United States); Bryan S. Kasprowicz, Photronics, Inc. (United States)

No Abstract Available.

9985-28, Session 8

Patterning in the era of sub-5nm technology node *(Invited Paper)*

Nihar Mohanty, Jeffrey T. Smith, Anton de Villiers, David R. Hetzer, Richard A. Farrell, Lior Huli, Hoyoung Kang, Subhadeep Kal, Akiteru Ko, Peter Biolsi, TEL Technology Ctr., America, LLC (United States)

Ever since Moore’s law was first published in 1965, the semiconductor industry has come a long way following the path where making devices smaller resulted in lower price per transistor, higher performance gain and more profits. While in the beginning lithographic advances played a major role in enabling the regular cadence of areal shrinkage, in the recent past, etch and atomic layer deposition (ALD) processes have been instrumental in assisting lithography for continued scaling. As the industry marches on onto the 5nm node and beyond, scaling has slowed down, with all major IDMs & foundries predicting a 3-4 year cadence for scaling. The reason for this slowdown is not the technical challenge of making features smaller, but effective control of the variation that creeps in to the fabrication process. That variability manifests itself as edge placement error (EPE) (including overlay), which has a direct impact on wafer yield. Resolving EPE and overlay concerns necessitates an integrated approach between unit process, materials development, process integration and design. In this paper we will provide a brief overview of the current and upcoming EPE and overlay improvement techniques with special emphasis on self-alignment based approaches. We will present some of the key challenges including the design element of self-alignment based integration and discuss mitigation strategies. We will conclude the talk with our view on the future direction for industry on patterning in the era of the sub-5nm technology node.

9985-29, Session 8

Correction of deflection under mask’s own weight by bending mask

Takashi Kambayashi, Minako Azumi, Naoyasu Uehara, Nikon Corp. (Japan)

The technology for liquid crystal displays’ is progressing every year with larger sizes and higher definition. Along with larger size, higher accuracy is also required for color filters. Mainstream production methods are lithography for color filters as well as the proximity method. In the proximity method, although the substrate is exposed in close proximity with a gap of several tens to several hundreds of microns from the mask, it is necessary to reduce this gap for higher accuracy. However, as the size of the mask increases, the deflection value by its own weight becomes greater, and the problem of contact damage between the substrate and the mask occurs.

To solve this problem, we have developed a technology for producing a “bending mask” having a shape that corrects deflection by its own weight. First, assuming the mounting method of the mask, the amount of deflection is calculated. Then using our precision polishing technology, the mask is processed to cancel the deflection induced under its own weight. By using this technique, it is possible to produce a mask shape suitable for a mounting with an error of 10 um.

With this process, it is possible to produce a mask shape capable of correcting deflection under its own weight, as a result, it becomes possible to obtain a uniform focus property in the exposure surface.

9985-30, Session 8

Contrast enhancement and its interplay with mask 3D effects in EUVL

Thorsten Last, Jo Finders, Laurens C. de Winter, Friso Wittebrood, Kateryna Lyakhova, Eleni Psara, Jan Lubkoll, ASML Netherlands B.V. (Netherlands)

Continuous scaling allows EUVL to be introduced as the next-generation lithography technique for high volume manufacturing of integrated circuits. The two main ingredients in the optical column to ensure high pattern fidelity and low line width roughness (LWR) are (i) mask absorber material and thickness and (ii) the angular spread and angles of incidence at mask level. A reduction of Ta-based absorber thickness below 70 nm would lead to favorable lithographic metrics such as decreasing dose-to-size (leading to increased throughput), and reduction of aberration-sensitive n-bar CD asymmetries. On the other hand an absorber thickness reduction leads to contrast loss, a situation increasingly critical for features with half pitches below 16 nm. We will present an experimental contrast enhancement study of combined Ta-based absorber thickness and illumination optimization for features with half pitches down to 14 nm. We will show that the reduction of line width roughness, and hence, local variability, is closely related to contrast enhancement. We reduce the absorber thickness from 70 nm through 40 nm and the pupil fill ratio of leaf shape dipole illumination conditions from 40% through 18%. Across this parameter space of absorber thickness and pupil fill ratio we can show that the normalized image log slope as measure of contrast is inversely proportional to the LWR of our dense horizontal 1D line/space features. Furthermore, we will show that for those half pitches of 14 nm which are slightly larger than the resolution limit it is preferable to concentrate the light closer to the center of the pupil. There a contrast maximum exists which is originating from the

interplay between a reduction of mask 3D induced phase aberrations and the capturing of diffracted light. Out of the results of this study in combination with a 2% upper bound of Ta absorber reflectivity a lower limit of 54 nm can be set for a typical Ta absorber thickness ensuring a resist limited LWR below 4.5 nm. An option recently put forward for further absorber thickness reduction could be the utilization of a high K alternative absorber material. This indeed would allow additional benefits for contrast-aware mask 3D mitigations without throughput penalty. Currently the balancing between contrast and mask 3D effects is being extended to two trench features (common in logic designs). Under conditions of maximum contrast the Bossungs of the top and bottom trenches of such a feature are severely tilted, leading to a reduced overlapping process window. We will explain how pattern fidelity can be restored by applying aerial image decomposition. We will show that balancing intensity and phase across the diffracted orders will drive optimal conditions of illumination and sub-resolution assist feature placement such that the CD difference between top and bottom trench is minimum and figures of merit such as overlapping process window and edge-placement will be optimized.

9985-31, Session 8

Quantifying imaging performance bounds of extreme dipole illumination in high-NA optical lithography

Myungjun Lee, Mark D. Smith, John Biafore, Trey Graves, Ady Levy, KLA-Tencor Corp. (United States)

In order to precisely monitor process variations and overlay errors between layers, computational target design is now necessary. Optimal target design will be achieved by understanding the fundamental aspects of the patterning process as well as the interaction among the features in the reticle, projection optics, and illumination optics. Researchers have made significant progress in understanding the limits and capabilities of projecting the image of the reticle onto a resist-coated wafer. Several notable analyses of lithography imaging based on key performance metrics such as the normalized image log-slope (NILS), the mask error enhancement factor (MEEF), and the depth of focus (DOF) throughout various different reticle dimensions and different reticle types have been previously undertaken. However, those important findings and contributions were all performed more than a decade ago on previous generations of DUV tools with a relatively low numerical aperture (NA) ≤ 0.65 and long wavelength ? ≥ 248nm. Therefore, the impressive recent improvement of a state of the art immersion lithography tool, providing an optimized FlexRay illumination with a higher NA and lower wavelength, has motivated a renewed interest in investigating the fundamental limits and capabilities of imaging performance throughout various pitches and line-to-space (LS) duty cycles.

We will present a framework to analyze the performance of optical imaging in a hyper NA immersion lithography scanner. We investigate the method to quantify imaging performance by computing upper- and lower-bounds on the threshold NILS and the DOF in conjunction with the traditional image quality metrics such as MEEF and linearity for various pitches and LS duty cycles. The effects of the interaction between the light illumination and the feature size are extensively characterized based on the aerial image (AI) behavior, in particular for the extreme dipole illumination. This type of illumination is one of the commonly used off-axis illuminations for sub-100nm logic and memory devices, providing resolution near the physical limit of an optical single patterning. The calculated AI-based DOF bounds are compared to the results obtained from an experimentally calibrated resist model, and we observed good agreement. In general, the extreme dipole illumination is only optimum for a single pitch, therefore understanding the through-pitch imaging performance bound, which depends on the illumination shape, the pattern size, and process conditions, is critically important. Overall imaging performance varies depending upon the number of the diffracted beams passing through the scanner optics. Significant non-linear behavior occurs in the 3-beam interference imaging region, where imaging performance and pattern printability become extremely sensitive to the LS duty cycle. In addition, the notable tradeoff between the DOF and the NILS (which define the achievable process window) is observed in such a problematic region. Under the given practical real world constraints such as the design rules and target design restrictions, computing upper- and lower-bounds of the through-pitch DOF and NILS will be especially useful for both lithographers and metrology target designers to understand complex behaviors, as well as the design of optimal targets used for applications including alignment, overlay control, and process control in high volume semiconductor manufacturing.

9985-32, Session 8

UDOF enhancement and photoresist profile tuning by modulating mask absorber thickness

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As the process generation migrate to advanced and smaller dimension or pitch, the mask and resist 3D effects will impact the lithography focus common window severely because of both individual depth-of-focus (iDOF) range decrease and center mismatch. Furthermore, some chemical or thermal factors, such as PEB (Post Exposure Bake) also worsen the usable depth-of-focus (uDOF) performance. So the mismatch of thru-pitch iDOF center should be considered as a lithography process integration issue, and more complicated to partition the 3D effects induced by optical or chemical factors.

In order to reduce the impact of 3D effects induced by both optical and chemical issues, and improve iDOF center mismatch, we would like to propose a mask absorber thickness offset approach, which is directly to compensate the iDOF center bias by adjusting mask absorber thickness, for iso, semi-iso or dense characteristics in line, space or via patterns to enlarge common process window, i.e uDOF, which intends to provide similar application as Flexwave[1] (ASML trademark).

By the way, since mask absorber thickness offset approach is similar to focus tuning or change on wafer lithography process, it could be acted as the process tuning method of photoresist (PR) profile optimization locally, PR scum improvement in specific patterns or to modulate etching bias to meet process integration request.

For mass production consideration, and available material, current att-PSM blank, quartz, MoSi with chrome layer as hard-mask in reticle process, will be implemented in this experiment, i.e. chrome will be kept remaining above partial thru-pitch patterns, and act as the absorber thickness bias in different patterns. And then, from the best focus offset of thru-pitch patterns, the iDOF center shifts could be directly corrected and to enlarge uDOF by increasing the overlap of iDOF. Finally, some negative tone development (NTD) result in line patterns will be demonstrated as well.

9985-90, Session 9

Translation of lithography variability into after-etch performance: monitoring of “golden hotspot”

Jo Finders, Ton Kiers, ASML Netherlands B.V. (Netherlands); Bertrand Le-Gratiet, Amine Lakcher, STMicroelectronics (France)

No Abstract Available

9985-33, Session 10

Effects of hard mask etch on final topography of advanced phase-shift masks

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Continuous shrinking of the semiconductor device dimensions demands steady improvements of the lithographic resolution on wafer level. These requirements challenge the photomask industry to further improve the mask quality in all relevant printing characteristics. Phase Shift Masks (PSM) are state-of-the-art and commonly use interference effects for contrast enhancement on wafer level. Printing behavior of these masks is not only affected by the critical dimensions (CD) but also by mask topography [1]. Insufficient quality of absorber profile can cause disturbing 3D effects on wafer and narrow the common process window. The etch processes (hard mask etch and absorber etch) jointly define the absorber profile. The final absorber etch is known to have the largest impact and has been extensively investigated already and optimized in the past [2]. Nevertheless, etch conditions of the hard mask layer (Cr) can also impact final absorber profile apart from defining the CD footprint.

In this paper we investigate the influence of the hard mask etch on phase shift uniformity and mask absorber profile. Design of experiments method (DoE) was used for the process optimization, whereas gas composition, bias power and overetch time were varied. We analyzed sidewall angle (SWA), reactive ion etch lag (RIE lag), uniformity and through pitch dependence of absorber depth range. Measurements were performed by means of Atomic-force microscopy (AFM) using CD mode with Boot Shape tip. Scanning electron microscope (SEM) cross-section images were prepared to verify the profile quality. Finally CD analyses was performed to identify the best etch conditions.

Significant dependence of the absorber SWA on hard mask etch conditions was observed revealing improvement potential for mask absorber profile. It was found that hard mask etch can leave a depth footprint in the absorber layer. Thus, etch depth uniformity of hard mask etch is crucial for achieving a uniform phase shift over the active mask area. The optimized hard mask etch process results in significantly improved mask topography without deterioration of tight CD specifications.

9985-35, Session 10

Improvement of CD error in local pattern area by optimizing develop loading condition

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The constant progress of chip's minimization and pattern shrinkage decreases dramatically the process margin of any step in the semiconductor manufacturing process. Diminished acceptable tolerance level in wafer process generally increases the MEEF (mask error enhancement factor) so require tighter critical dimension (CD) control in the Mask. Especially, it became very important to control the CD variation in the chip boundary and the CD variation between central mat and mat in one chip. Changing the resist or e-beam writing conditions have been tried to solve the CD error. But this approach not only can cause the CD error in unexpected region but also requires various experiments to verify the stability of process. Some papers have named develop loading effect as main reason of the CD error. It makes CD variation of a few nm in a distance of several tens of micrometers according to the pattern density. We studied how develop loading effect can be diminished by optimize factors in the develop process such as total develop time, puddle time, dispense time, scan speed and chuck height, etc. And we analyzed factors to make the CD error in the chip boundary.

9985-54, Session 10

Optical properties comparison of Cr and MoSi based PSM for flat panel display

Jin Woong Jeong, Jin Han Song, Ho Jin Lee, Kyu Sik Kim, Woo-Gun Jeong, Sang Pil Yun, Young Jin Yoon, Samuel S. Jung, PKL Co., Ltd. (Korea, Republic of)

The requirements for Flat Panel Display (FPD) photomasks become tighter as the resolution increases. Mask pitch of sub-pixel goes decreased continuously in Liquid Crystal Display (LCD) and pixel density of Active Matrix Organic Light Emitting Diode (AMOLED) requires more than 700ppi in Ultra Define (UD) for higher resolution. Lens Numerical Aperture (NA) and broadband wavelengths such as I-line, H-line and G-line of existing scanners have been limited factors for obtaining high resolution in FPD. It is well known that half-tone phase shift masks (HT-PSMs) improve the resolution in the semiconductor industry. MoSi has been widely used as material with the phase shifter for i-line, KrF and ArF lithography in Integrated Circuit (IC) photomasks. Also Cr based PSM was also researched and developed for both IC and FPD. Even if Cr and MoSi based PSM is already developed, application of these PSMs in FPD has to consider all feasibility of production. At the same time we do not know exactly which PSM material is better for application of FPD with respect to mask quality including optical properties.

So we have evaluated 5% Cr and MoSi based i-line PSMs by analyzing optical properties such as reflectance, phase and transmittance of the phase shifter, because the optical properties of the PSM are important factors which determine product qualities by affecting Critical Dimension (CD) on the panel. Both Cr and MoSi based PSMs are compared when it comes to optical properties of them.

Finally, a guideline on selection of half-tone shifter material is discussed for FPD mask. Also we can suggest some directions for using each type of PSM.

9985-67, Session 10

Registration performance on EUV masks using high-resolution registration metrology

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The extension of optical lithography operating at 193nm illumination wavelength down to the 10 nm node and below have increased the complexity and production costs significantly. Although still facing multiple challenges such as source power and blank defectivity, EUV is nevertheless widely accepted as future technology to meet the semiconductor industry's need beyond the 10 nm node. The introduction of EUV technology into production is currently targeted for the 7 nm node and an initial hybrid approach is expected. Thus, the most critical layers are printed by EUV technology while other less critical layers are continued with 193nm technology. Assuming an EUV introduction in 2018, the ITRS roadmap specifies tight mask registration and overlay specs of 1.8 nm and 3 nm, respectively. This requires precise and high-resolution metrology not only on DUV masks, but also on patterned high-end EUV reticles.

The scope of this work is an image placement investigation of high end EUV masks together with a registration and resolution performance qualification of a new generation registration metrology system embedded in a production environment for full spec EUV masks.

Past generations of mask registration tools were not necessarily limited in their tool stability but in their resolution capabilities. The primary focus is therefore set on a detailed evaluation of resolution capability vs. measurement precision for standard metrology targets as well as production features.

9985-37, Session 11

Quantitative simulation of MoSi migration in OMOG by ArF exposure and the effect of mask cleaning

Taeki An, Jong Min Kim, Hyo-Jin Ahn, Ik-Boum Hur, Sang-

Soo Choi, PKL Co., Ltd. (Korea, Republic of)

OMOG(Opaque MoSi-On-Glass) reticles have been widely used for lithography at high-end wafer production. Therefore, CD(Critical Dimension) variation at OMOG reticle should be managed much tighter than PSM. It is reported that MoSi on OMOG can migrate into the clear region after cumulative radiation as chrome on COG showed similar phenomenon. It results degradation of pattern edge. In addition, it is observed that the degradation of MoSi is affected by the cleaning process before exposure.

We conducted several experiments focusing cleaning effect on MoSi migration. A cross-section of affected MoSi was observed. MoSi CD increase by light exposure was measured. We used a HATB(Haze Acceleration Test Bench) equipped with 193nm laser as an exposure tool instead of an ArF scanner.

Furthermore, we also evaluated the influence of cleaning process on the MoSi migration. Several different chemicals were applied for the cleaning process. Influence by each chemical was measured quantitatively. The MoSi migration mechanism itself and the effect of chemicals were discussed.

9985-38, Session 11

Megasonic cleaning strategy for sub-10nm photomasks

Jyhwei Hsu, SUSS MicroTec (Taiwan) Co., Ltd. (Taiwan); Martin Samayoa, Uwe Dietze, SUSS MicroTec Inc. (United States); Peter Dress, SUSS MicroTec Photomask Equipment GmbH & Co. KG (Germany); Ai-Jay Ma, Chia-Shih Lin, Rick Lai, Jong-Yuh Chang, Laurent C. Tuo, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

Advanced lithographic processes require complex resolution enhancement technologies. These resolution enhancement technologies include building sub-resolution assist-features (SRAF) on photomask. With each advancement in device nodes, the size of SRAF is further reduced. At the same time, smaller particles must be removed from the mask surface, especially out of trenches, which requires increasing physical forces, i.e. higher megasonic power, to be applied during cleaning. However, due to their high aspect ratio, SRAF are prone to damage at high megasonic power, and therefore it has become increasingly difficult to achieve high Particle Removal Efficiency (PRE) and at the same time preserve the integrity of SRAF. To mitigate pattern damage, higher frequency megasonic cleaning strategy is adopted.

In megasonic cleaning, the formation of micro-bubbles is important for obtaining reasonable high PRE. In addition, compression of the hydrodynamic boundary layer is playing a role. In order to maximize cleaning efficiency and, at the same time minimize the pattern damage, it is important to control the bubble size as well as bubble dynamics, compress the hydrodynamic boundary layer and maintain high enough physical force momentum. Uniform bubble size is a key to have controllable cavitation. However, bubble heterogeneous nucleation on the substrate surface can cause unexpected size and cavitation behavior. Moreover, gas pockets trapped in trenches between SRAF and main features are also a cause for uncontrolled bubble formation. In order to avoid such unexpected cavitation behavior, proper conditioning of the substrate surface is also very important prior to applying megasonic energy.

In our studies we found that, higher megasonic frequency, combined with proper surface preparation provides high PRE without pattern damage, hence is extending Megasonic cleaning technology into 10nm device node and potentially beyond. In this paper we are discussing PRE and SRAF preservation, comparing 3 MHz, 4MHz and 5 MHz Megasonic technology. In addition, we are showing the impact of various surface treatment methods on Megasonic cleaning results.

9985-39, Session 11

Identification of a new source or reticle contamination

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No Abstract Available

9985-40, Session 11

Impact of EUV photomask multilayer defect repair on resolution enhancement techniques

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As extreme ultraviolet lithography (EUVL) is being pursued for high volume manufacturing, the necessity of optical proximity correction (OPC) and source mask optimization (SMO) must be considered. Furthermore, the absense of readily available defect-free blanks mandates a robust mask defect repair strategy. Commercialized mask repair techniques focus on absorber biasing to compensate for imaging contrast loss originiating from multilayer phase defects, while preliminary studies have looked into multilayer nanomachining for compensating the through-focus Bossung asymmetry. The work here explores the limitations of these techniques and expands upon them through finite-difference time-domain (FDTD) simulations, focusing on the interactions between various repair strategies and the resolution enhancement techniqes necessary for EUV HVM enablement. Particular attention is placed on bi-direcitonal and 2D designs, optimized using aggressive OPC and custom SMO sources, and the viability of native phase defect repair via both absorber and multilayer modification. The results here reveals the subtle dependencies of mask repair strategies on resolution enhancement techniques, and the need for a robust phase repair solution to ensure EUV HVM readiness.

9985-41, Session 12

Computational Imaging: The Path Forward *(Invited Paper)*

Vivek K. Singh, Intel Corp. (United States)

Moore's Law is an observation that a transistor – the fundamental building block of the digital age – will decrease in cost at a steady, exponential rate. This decrease in cost as well as transistor size over the past 50 years has also led to dramatic increases in compute power and energy efficiency and transformed our world with ever-more powerful smart phones, tablets, personal computers and data centers. These imperatives are the reason Moore's Law will continue, and motivated teams will continue to find innovative solutions to the engineering challenges of the day. Many of these challenges lie in the realm of imaging and mask making. This talk will describe some of those challenges, and associated opportunities, with a particular focus on EUV.

9985-42, Session 12

Software-based data path for raster-scanned multi-beam mask lithography

Archana Rajagopalan, Ankita Agarwal, Mentor Graphics (India) Pvt. Ltd. (India); Peter D. Buck, Mentor Graphics Corp. (United States); Paul Geller, H. Christopher Hamaker, Applied Materials, Inc. (United States); Nagswara Rao, Mentor Graphics (India) Pvt. Ltd. (India)

According to the 2013 SEMATECH Mask Industry Survey, roughly half of all photomasks are produced using Laser Pattern Generator (“LPG”) lithography. LPG lithography can be used for all layers at mature technology nodes, and for many non-critical and semi-critical masks at advanced nodes. The extensive use of multi-patterning at the 14-nm node significantly increases the number of critical mask layers, and the transition in wafer lithography from positive tone resist to negative tone resist at 14-nm enables the switch from advanced binary masks back to attenuated phase shifting masks that require second level writes to remove unwanted chrome. LPG lithography is typically used for second level writes due to its high productivity, absence of charging effects and versatile non-actinic alignment capability. As multi-patterning use expands from double to triple patterning and beyond, the number of LPG second level writes increases correspondingly. The desire to reserve the limited capacity of advanced electron beam writers for use when essential is another factor driving the demand for LPG capacity.

The increasing demand for cost-effective productivity has kept most of the laser mask writers ever manufactured running in production, sometimes long past their projected lifespan, and new writers continue to be built based on hardware developed some years ago.The data path is a case in point. While state-of-the-art when first introduced, hardware-based data path systems are difficult to modify or add new features to meet the changing requirements of the market. As data volumes increase, design styles change, and new uses are found for laser writers, it is useful to consider a replacement for this critical subsystem.

The availability of low-cost, high-performance distributed compute systems combined with highly scalable EDA software lends itself well to the creation of an advanced data path system. EDA software, in routine production today, scales well to hundreds or even thousands of CPU-cores, offering the potential for virtually unlimited capacity. Features available in EDA software such as sizing, scaling, tone reversal, OPC, MPC, rasterization and others are easily adapted to the requirements of a data path system.

In this paper we will present the motivation, specification, design, and performance of an advanced, scalable software data path system suitable to support multi-beam laser mask lithography.

9985-43, Session 12

OPC care-area feedforwarding to MPC

Masakazu Hamaji, Tomoyuki Muramatsu, Nippon Control System Corp. (Japan); Shuichiro Ohara, Nippon Control System Corp. (United States); Yi-Hsing Peng, Xiaolong Zhang, Stanislas Baron, Yi Zou, ASML US, Inc. (United States)

Demand for mask process correction (MPC) is growing for leading-edge process nodes. MPC was originally intended to correct CD linearity for narrow assist features difficult to resolve on a photomask without any correction, but it has been extended to main features as process nodes have been shrinking.

As past papers have observed, MPC shows improvements in photomask fidelity. Using advanced shape and dose corrections could give more improvements, especially at line-ends and corners. However, there is a dilemma on using such advanced corrections on full mask level because it increases data volume and run time. In addition, write time on variable shaped beam (VSB) writers also increases as the number of shots increases.

OPC care-area defines circuit design that requires high mask fidelity under mask writing process variations such as energy fluctuation. It is useful for MPC to switch its correction strategy and permit the use of advanced mask correction techniques in those local care-areas where they provide maximum wafer benefits. The use of mask correction techniques tailored to localized post-OPC design can result in similar desired level of data volume, run time, and write time. ASML-Brion and NCS have jointly developed a method to feedforward the care-area information from Tachyon OPC to NDE-MPC to provide real benefit for improving both mask writing and wafer printing quality.

This paper explains the detail of OPC care-area feedforwarding to MPC between ASML-Brion and NCS, and shows the results. In addition, improvements on mask and wafer simulations are also shown. The current results indicate that the worst PV Bands are reduced up to 23% and 32% for metal and contact cases respectively.

9985-44, Session 12

Improving corner acuity on photomasks using dose-based MPC

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Photo masks for leading edge semiconductor process nodes are mostly written using 50keV VSB (Variable Shaped Beam) e-beam writers and chemically amplified resists. Due to the various effects, such as beam blur, electron scattering and diffusion, rectangular shapes do not print with sharp corners but exhibit significant corner rounding.

For small feature sizes such as contact holes and SRAFs (Sub-Resolution Assist Features), corner rounding itself impacts the wafer printing results only slightly as long as the area of the feature is kept constant [1]. When keeping the area constant, rounder contacts are even slightly brighter than more square contacts. However, it is not always possible to compensate the area loss caused by corner rounding and in such cases, the smaller area of the mask feature causes a smaller CD on wafer [2]. Improving corner acuity of Manhattan type features on photo masks is therefore desirable and will be discussed in this article.

While optical lithography generally uses serifs on corners to improve the wafer image, e-beam lithography provides another degree of freedom through shot dose assignment of individual VSB shots. We have shown before how this technique can be used in an integrated MPC solution to extend the mask process resolution limit towards smaller features, improve mask CD linearity, and mitigate the impact of mask hotspots [3], [4].

In this article we show how dose-based MPC can be used to improve corner rounding of Manhattan features on photo masks. The effectiveness of various solutions will be evaluated in a simulation study and some of those solutions will be verified on EUV masks. Simulations show that size and dose of corner or line-end shots need to be well optimized in order to achieve the best results. For EUV masks those shots are well below 50nm in size and therefore pose a significant challenge for e-beam mask writers.

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9985-45, Session 12

The performance improvement of SRAF placement rules using GA optimization

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Sub-resolution assist features (SRAF) are widely used in Optical Proximity Correction (OPC) to enhance the main feature printing ability. Since off-axis illumination allows for larger focal range, but increases bias, SRAF

could extend its application with additional diffraction orders provided by additional edges. Larger SRAF's typically provide more benefit to the main feature, but increase the risk of SRAF printing. Thus, placement rules determine how well SRAF's could assist the main pattern. The primary parameters to define SRAF insertion are:

1) Shape of the main pattern.

2) Offset of the assist feature from the main pattern.

3) Width and length of the assist feature.

4) Distance between two assist features.

To optimize these parameters, tools and methods such as pixelated OPC simulation, Inverse Lithography Technology and other optimization algorithms are available. In this paper, we demonstrate via intense simulation and wafer verification that a GLOBALFOUNDRIES developed SRAF optimization tool with genetic algorithm (GA) method, successfully predicted the RBSRAF placement rules. This tool can optimize the multiple SRAF parameters mentioned above and construct an intelligent cost function capturing matrices which are directly related to wafer imaging and SRAF printing performance. In detail, a specific pattern, which could be a hotspot or anchor structure, is generated as the input to this tool. The output will give us a set of optimized SRAF rules, which are subsequently applied to a large test macro to refine the rules and validate the results via OPC simulations. Typically several iterations of this procedure are required to finalize SRAF placement rules. The optimized SRAF rules are further incorporated into the OPC recipe with SRAF Printing Avoidance (SPA) to insure the elimination of the SRAF printing risk. Full chip simulation and physical wafer verification are utilized to confirm results.

Additional steps were taken to compare this method with MBSRAF and RBSRAF with pixelated OPC simulation. MBSRAF is unable to provide the optimal solution for SRAF placement and has to rely on the SPA to avoid SRAF printing issues. RBSRAF with pixelated OPC simulation was not able to find the optimal rules either. RBSRAF with GA method, on the other hand, produced the better SRAF placement rules requiring little to no modification during the SPA operation. SRAF printing avoidance was verified on wafer.

9985-46, Session 13

Writing next-generation display photomasks *(Invited Paper)*

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In recent years there has been a fast technological development within the display industry. The displays get higher and higher resolution, which means pixels get smaller and smaller. At the same time there is a trend towards more complex displays such as AMOLED, which require more complicated pixel designs and more patterns inside the pixel. AMOLED is generally more sensitive and demanding, since the transistors are used in the active domain to control the light, instead of being used as switches for the LCD case.

These trends have rapidly tightened the lithography requirements with implications for the photomasks quality. The top critical display photomasks requirements become similar to the low end semiconductor nodes. For this reason many of lithography technologies used for semiconductors is transferring to display industry such as RET (Resolution Enhancement Technology) which requires smaller feature size with finer CD control. Hence, the demand increase for higher resolution lithography equipment not only for panel manufacturing, but also in photomask manufacturing. Fig. 1 is the resolution trends for lithography system used in display manufacturing and for mask writers. It shows that higher resolution mask writing is needed to support the next generation display. Display photomasks typically are 30-80 times larger than an ordinary 6 inch mask used in semiconductor manufacturing. This creates an extraordinary challenge to meet the future requirements over the full area and to have the stability needed for writing times which can be 24-48 hours.

In this paper Mycronic shares what is needed to meet current and future requirements in terms of next generation mask writer performance and platform stability. It is demonstrated how to achieves high resolution with better than 40nm CD uniformity and keep global registration better than 100nm without jeopardizing productivity.

9985-47, Session 13

Advanced NIL mask technologies which hold the key to achieving the semiconductor production *(Invited Paper)*

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The cost reduction and high performance of memory device will be required by customer continuously. However, investment costs in pattern shrinking technologies, such as multi-patterning and EUVL become enormous. The framework in these pattern shrinking technologies has not been able to provide lower-cost semiconductor devices. Therefore, in order to significantly reduce investment cost in lithography, nanoimprint lithography technology has been developing1). One of the most significant challenges in nanoimprint technology is nano-defect management (NDM) technology in which defect inspection of templates and imprinted wafer, the resist material innovation and the defect mitigation is implemented. Nano-imprint specific problem has been predicted and corrected with computational lithography technology development. Moreover, resist defects on the template are generated after etching and resist pattern etching resistance under sub 20 nm hp is a critical issue for NIL. Resist material innovation and process integration are required for all upcoming lithography technologies.

We tried NIL technology to advanced device and succeeded to obtain the yield evidence with CANON NIL2). We are verifying the fundamental technologies and the compatibility of NIL to Si-fab. We are now preparing the NIL technologies for the production line. We must solve the unique challenges of NIL in defectivity, overlay accuracy, and productivity. The key to future success in semiconductor business will continue to be developing high performance and low cost patterning technology such like NIL. The success in NIL depends on the advances template technologies.

In this paper, status of the nanoimprint lithography applications to the semiconductor device, progress of nanoimprint related technology by improvement of template technologies will be shown.

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9985-48, Session 13

Performance of nanoimprint templates for the next-generation lithography

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Nanoimprint lithography (NIL) is one of the most potential candidates for the next generation lithography for semiconductor and is gathering more attentions. This technology needs almost no additional mask data preparation from design, simpler exposure system, and just single patterning process without any coat/develop truck, and has potential of cost effective patterning rather than very complex optical lithography and/or EUV lithography.

Replica templates are made by replicating the EB written high quality master templates. Maintaining the quality of the master templates in replication process is very important. NIL technique is used for the template replication, and optimization of the nanoimprint process is the key as well as pattern transfer etching process after imprint.

Defect quality is one of the most concerns for NIL templates. The master templates were defect free owing to the advanced repair technology. In replication, nanoimprint specific defects will appear on the replicated templates. By classifying these defects and analyzing the mechanism of the defect generation, we have succeeded to reduce the defect density drastically.

Image placement is another focus of nanoimprint templates, especially for the next generation lithography. Template image placement degrades at replication because nanoimprint process produces physical stress on both substrates. Stress reduction is necessary for image placement improvement.

In this presentation, our development results on NIL template replication will be presented.

9985-49, Session 13

Nanoimprint wafer and mask tool status for high-volume semiconductor manufacturing

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Imprint lithography is an effective technique for replication of nano-scale features. Jet and Flash Imprint Lithography* (J-FIL*) involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, the mask is removed, and leaves a patterned resist on the substrate.

Previous studies have demonstrated resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero resist waste leads to a cost model that is very compelling for semiconductor memory applications.

There are many other criteria that determine whether a particular technology is ready for manufacturing. With respect to the imprint stepper, both critical dimension uniformity (CDU) and line edge roughness meet the criteria of 2nm. Overlay of 5nm, 3? has been demonstrated, and defect levels ~ 5/cm2 has been achieved. Other criteria specific to any lithographic process include throughput, and for a four station cluster tool, a throughput of 40 wafers per hour has been reported.

On the mask side, there are stringent criteria for CDU, image placement accuracy and imprint defectivity. Semiconductor requirements dictate the need for a well-defined form factor for both master and replica masks which is also compatible with the existing mask infrastructure established for the 6025 semi standard, 6" x 6" x 0.25" photomasks.

In this paper, we review the advancements in both wafer imprint and mask replication systems. To address high volume manufacturing concerns, a cluster approach will be used in order to meet throughput and cost of ownership requirements (CoO). The FPA-1200 NZ2C is a four station cluster tool, and the status of overlay, throughput and defectivity will be discussed. Mask replication is required for nanoimprint lithography, and criteria that are crucial to the success of a replication platform include both particle control and image placement accuracy. These topics, as well as others will be presented.

*Jet and Flash Imprint Lithography and J-FIL are trademarks of Molecular Imprints Inc.

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