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8166-200, Session JPM1

Mask blank material optimization impact on leading-edge ArF lithography

K. Mesuda, Dai Nippon Printing Co., Ltd. (Japan)

No abstract available

8166-201, Session JPM1

Study on the correlation between mask preparation techniques and its lifetime in the wafer fab

E. Foca, Advanced Mask Technology Ctr. GmbH Co. KG (Germany)

No abstract available

8166-202, Session JPM1

The effect of resist removal methods on mask CD variation by cleaning process

J. Ryu, Hynix Semiconductor Inc. (Korea, Republic of)

No abstract available

8166-203, Session JPM1

Binary 193-nm photomasks aging phenomenon study

F. Dufaye, STMicroelectronics (France)

Binary 193nm photomasks are still used in the semiconductor industry for the lithography of some critical layers for the nodes 90nm and 65nm, with high volumes and long usage time. These binary 193nm masks seem to be well-known but recent studies have shown surprising degrading effects, like Electric Field induced Migration of chromium (EFM) [1] or chromium migration [2] [3]. Phase shift Masks (PSM) or Opaque MoSi On Glass (OMOG) might not be concerned by these effects [4] [6] under certain conditions.

In this paper, we will focus our study on two examples of layers gate and metal lines. We will detail the effects of mask aging, with SEM top view pictures revealing a degraded chromium edge profile and TEM chemical analyses demonstrating the growth of a chromium oxide on the sidewall. SEMCD measurements after volume production indicated a modified CD with respect to initial CD data. A regression analysis of these CD measurements shows a radial effect, a die effect and an isolated-dense effect. Mask cleaning effectiveness has been also investigated, with sulphate or ozone cleans, to recover the mask quality in terms of CD.

In complement, wafer intrafield CD measurements have been performed on the most sensitive structure to monitor the evolution of the aging effect on mask CD uniformity. Mask CD drift have been correlated with exposure dose drift and isolated-dense bias CD drift on wafers.

In the end, we will try to propose a physical explanation of this aging phenomenon and a solution to prevent from its occurrence.

8166-204, Session JPM1

193-nm radiation durability study of MoSi binary mask and resulting lithographic performance

I. Servin, Commissariat à l'Énergie Atomique (France)

Dimensions on mask continue to shrink to keep up with the ITRS roadmap. This has implications on the material of choice for the blanks. For example, the new binary OMOG stack (Opaque MOSi on Glass) was successfully introduced to meet the mask specifications at the 32nm technology node. Obviously 193-nm optical lithography will be further used in production at even higher NA and lower k1 emphasizing, for example, the impact on wafer of any electromagnetic field migration effects. Indeed, long term radiation damage inducing CD growth and consequently, device yield loss, has already been reported [1, 2]. This mechanism, known as Electric Field induced Migration of chrome (EMF) often shortens masks lifetime.

Here, a study was conducted to investigate the impact of intensive ArF scanner exposure both on final wafer and mask performances. The Si printed wafers measured with top-down CD-SEM were characterized with respect to CD uniformity, linearity, Sub Resolution Assist Feature (SRAF) printability through process window, MEEF, DOF, and OPC accuracy. The data was also correlated to advanced mask inspection results (e.g. AIMSTM) taken at the same location. More precisely, this work follows a preliminary study [1] which pointed out that OMOG is less sensitive to radiation than standard COG (Chrome On Glass). And, in this paper, we report on results obtained at higher energy to determine the ultimate lifetime of OMOG masks.

8166-205, Session JPM1

RegC : a new registration control process for photomasks after pattern generation

E. Graitzer, A. Cohen, V. Dmitriev, G. Ben Zvi, D. Avizemer, Carl Zeiss SMS Ltd. (Israel)

As the lithography roadmap unfolds on its path towards ever smaller geometries, the pattern placement (Registration) requirements are increasing dramatically. This trend is further enhanced by anticipating the impact of innovative process solutions as double patterning where mask to mask overlay on the wafer is heavily influenced by mask registration error.

In previous work a laser based registration control (RegC) process in the mask periphery (outside the exposure field) was presented. While providing a fast and effective improvement of registration, the limitation of writing with the laser outside of the active area limits the registration improvement to ~20%. This process can be applied after the pattern generation process and tune the mask registration.

In this work we will show registration correction results where the whole mask area is being processed. While processing inside the exposure field it is required to maintain the CD Uniformity (CDU) neutral .In order to maintain the CDU neutral several different laser writing modes are utilized. A special algorithm and software were developed in order to compute the process steps required for maintaining the CDU neutral from one side while correcting for mask placement errors on the other side. By applying the correction process inside the active area much better improvements regarding mask registration and overlay can be achieved

8166-206, Session JPM1

Benefits of overlapping shots for ArF and EUV mask process correction

A. Fujimura, D2S, Inc. (United States)

No abstract available

8166-207, Session JPM1

Evaluation of process variations on OPC model predictions

S. Barai, IBM Semiconductor Research and Development Ctr. (India)

Process models have been in use for performing proximity corrections to designs for placement on lithography masks for a number of years. In order for these models to be used they must provide an adequate representation of the process while also allowing the corrections themselves to be performed in a reasonable computational time. As the semiconductor industry continues to march toward smaller and smaller dimensions - with smaller tolerance to error- we must consider the importance of those process variations. In the present work we describe the results of experiments performed in simulations to examine the importance of many of those process variables which are often regarded as fixed. We show examples of the relative importance of the different variables.

8166-208, Session JPM1

Defect printability of advanced binary film photomask

M. Naka, Toshiba Corp. (Japan)

No abstract available

8166-209, Session JPM1

Role of ellipsometry in DPT process characterization and impact of performance for contact holes

I. Kamohara, Nihon Synopsys G.K. (Japan)

No abstract available

8166-01, Session 1

Keynote Presentation

No abstract available

8166-02, Session 2

Mask Industry Assessment: 2011

G. P. Hughes, D. Y. Chan, SEMATECH North (United States)

A survey created and supported by SEMATECH and administered by David Powell Consulting was sent to microelectronics industry leaders to gather information about the mask industry as an objective assessment of its overall condition. The survey was designed with the input of semiconductor company mask technologists and merchant mask suppliers. This year's assessment is the tenth in the current series of annual reports. With ongoing industry support, the report can be used as a baseline to gain perspective on the technical and business status of the mask and microelectronics industries. It will continue to serve as a valuable reference to identify the strengths and opportunities of the mask industry. The results will be used to guide future investments pertaining to critical path issues. This year's survey was basically the same as the 2005 through 2010 surveys. Questions are grouped into categories: General Business Profile Information, Data Processing, Yields and Yield Loss Mechanisms, Delivery Times, Returns, and Services. Within each category are multiple questions that result in a detailed profile of both the business and technical status of the critical mask industry. This profile combined with the responses to past surveys represents a comprehensive view of changes in the industry.

8166-03, Session 2

EMLC 2011 Best Paper: Evidence of printing blank-related defects on EUV masks missed by blank inspection

R. M. Jonckheere, D. Van den Heuvel, IMEC (Belgium); T. Bret, T. Hofmann, Carl Zeiss SMS GmbH (Germany); J. F. Magana, Intel Corp. (United States); I. Aharonson, D. Meshulach, Applied Materials (Israel); E. Hendrickx, K. G. Ronse, IMEC (Belgium)

No abstract available

8166-04, Session 3

Accelerating EUV learning with synchrotron light

P. P. Naulleau, Lawrence Berkeley National Lab. (United States)

No abstract available

8166-05, Session 3

Phase defect analysis with actinic full-field EUVL mask blank inspection

T. Yamane, T. Tanaka, T. Terasawa, O. Suga, Semiconductor Leading Edge Technologies, Inc. (Japan)

Extreme Ultraviolet lithography (EUVL) is a promising technology for ULSI devices with a half pitch of 32 nm and beyond. However, the fabrication of defect-free mask blanks and their inspection continues to be a matter of concern. To address this issue, an actinic (at wavelength) full-field EUVL mask blank inspection system with a dark field imaging technique had been developed in Selete.

Due to advanced optics, and improvement in detector and detection algorithm, defect sensitivity had been enhanced to prevent false defect detection resulting in improved throughput. Then, programmed defects of 1 nm-high 40 nm-wide were detected at a probability of 90% with no false detection at full-field of a mask and the inspection time for full-filed of a mask was attained to be 4 hours 45 minutes. Therefore, the inspection system is found to be available for 22 nm HP and beyond. Regarding native defects, a 1.1 nm-high 20 nm-wide defect was detected successfully. Our simulation shows that a large strain in multilayer might be residing in such small native defects. To confirm this estimation, internal structure in multilayer of native defects detected with the inspection system were observed with TEM. The TEM result shows that the defect heights become lower from middle of the multilayer to the surface and the defect widths become wider from bottom of the multilayer to the surface. This means that the inspection system detect a small defect on the surface which contains a large

strain in the multilayer.

In this presentation, improvement of inspection capability during Selete project will be reported. Inspection result for several mask blanks will be shown, and the analysis result of the detected phase defects with AFM and TEM will be presented.

This work was supported by New Energy and Industrial Technology Development Organization (NEDO).

8166-06, Session 3

Defect printability of native blank defects, program defects, and their stack structures

H. J. Kwon, J. Harris-Jones, T. Ranganath, V. Jindal, A. M. Cordes, D. Y. Chan, F. Goodwin, G. P. Hughes, SEMATECH North (United States); T. Nakajima, AGC Electronics America, Inc. (United States); I. Mochi, K. A. Goldberg, Lawrence Berkeley National Lab. (United States); Y. Yamaguchi, H. Kinoshita, Univ. of Hyogo (Japan)

Defect control in both mask making and wafer processing becomes increasingly critical when using extreme ultraviolet (EUV) pre-production tools. Much effort has been devoted to studying the printability of blank defects on wafers. Printability and inspectability are reviewed at the current design nodes using various metrology tools. Blank and patterned mask defects are usually correlated with the defects printed on wafers. Although the defect dimensions can be characterized using atomic force microscopy (AFM), realistic characterization of native phase defects cannot be done without knowledge of the defect-induced changes in the structure of the deposited multilayer (ML).

In this paper, we describe characterizations of native phase defects in the manufacturing of EUV mask blanks using the state-of-the-art mask metrology equipment in SEMATECH's Mask Blank Development Center. We use commercially available masks, which have different ML deposition conditions, to characterize and compare effects on phase defects. We also have prepared programmed bump and pit defects of various dimensions using e-beam patterning technology and investigate ML decoration on them. Printability studies include a review and compare both native and programmed defects. Transmission electron microscopy (TEM) is used to study ML profile change, while SEMATECH's actinic inspection tool (AIT) is used to image defects and predict their printability. Defect images at different focal depths of the AIT will be correlated to TEM cross sections and AFM dimensions.

8166-07, Session 3

Advancing EUV mask microscopy with ultra-high resolution and the capacity for shorter EUV wavelengths

K. A. Goldberg, I. Mochi, E. M. Gullikson, E. H. Anderson, P. P. Naulleau, Lawrence Berkeley National Lab. (United States); H. J. Kwon, D. Y. Chan, SEMATECH North (United States)

We are developing a next-generation EUV mask-imaging microscope based on the proven optical principle of the SEMATECH Berkeley Actinic Inspection Tool (AIT), but surpassing it in every performance metric. The new tool design will enable research on multiple generations of EUV lithography technology, down to 8 nm and beyond.

Owing to the wavelength-specific reflective properties of EUV reticles, imaging with EUV light is the only faithful way to understand the physical response of defects, repairs, and pattern optical proximity corrections. The wavelength-specific properties limit the effectiveness of all non-EUV inspection technologies, and the differences between EUV and non-EUV measurements are likely to increase in future nodes.

As a high-magnification, all-EUV Fresnel zoneplate microscope, the AIT has been in the vanguard of high-resolution EUV mask imaging for several years. The AIT's measurement of mask architectures, blank and pattern defect imaging, defect smoothing and printability, and recently, direct, quantitative aerial image phase measurement, has expanded our collective understanding of EUV masks and shaped the course of current mask development. The new tool will greatly surpass the capabilities of the AIT by overcoming many of its current limitations.

A Fourier-synthesis illuminator will provide the new, synchrotron-based microscope with lossless, programmable coherence control with arbitrary pupil fills and partial-coherence σ values as low as 0.2. The illuminator will also deliver a range of azimuthal angles of incidence, which can be paired with rotated zoneplate lenses to emulate arbitrary current and future steppers across the arc-shaped field of view.

The original design concept for the new microscope enables variable-NA imaging with 4xNA values between 0.25 and 0.625 with angles of incidence between 6° and 10° using an array of user-selectable zoneplate lenses. However, we recognize that it will be possible to include additional zoneplate lenses for special, high-resolution imaging modes with non-circular pupils that greatly increase the collection solid angle and resolution. We will describe the usable range of zoneplate lens resolutions given current nano-fabrication patterning limits and predicted EUV efficiencies.

Many in the EUV community are now looking forward to opportunities at shorter EUV wavelengths, near 6.5 nm. If necessary, the new microscope could be upgraded for operation at a new wavelength merely by replacing three multilayer-coated mirrors-two flat and one ellipsoid. We will explore the relative efficiency of short-wavelength configurations under current assumptions of multilayer coating reflectivity and zoneplate efficiency.

We are now working to bring this capability online in late 2012, well in advance of commercial tool availability, to have it ready for advanced research into future EUV lithography generations.

This work was performed under the auspices of the U.S. Department of Energy by University of California Lawrence Berkeley National Laboratory. This work was funded by SEMATECH through the U.S. Department of Energy under Contract No. DE-AC02-05CH11231.

8166-08, Session 3

EUV mask absorber and multi-layer defect disposition techniques using computational lithography

M. Satake, V. L. Tolani, P. Hu, D. Peng, Y. Li, L. Pang, Luminescent Technologies, Inc. (United States); B. Cha, G. Yoon, W. Cho, J. Na, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

Many efforts in EUV are currently focussed on detecting and reducing defects on blanks and patterned masks. Bumps and pits found on blank substrates are particularly of concern since these effectively cause phase change and often print severly under EUV conditions. With the current inspection of EUV blanks and patterned masks being primarily high-resolution DUV or e-beam based, it becomes very challenging to assess the impact of the detected defects. Even with the realization of EUV AIMS, expected in 2014, the nature of the buried multi-layer defect in terms of its location, size, shape, and profile will always be uncetain.

In this paper, we have demonstrated several techniques that can be used for EUV defect disposition both short- and long-term. These techniques include use of SEM and DUV inspection images for absorber-defect disposition, and a combination of SEM, AFM, and DUV inspection images for determining the printability of buried defects.

In the case of absorber defects, the SEM image of the defect is processed through a novel contour-extraction algorithm which accurately extracts the contours of the defective and reference regions. The mask contours are then simulated in Luminescent's EUV Defect Printability Simulator (DPS), a fast and accurate EUV simulator, and the EUV aerial images subsequently analyzed in the Aerial Image Analyzer (AIA). Good matching of simulations with actual print of absorber-level

defects have been achieved in this flow.

For buried defects, several models describing the evolution of the multi-layer defect from substrate and multi-layer to the surface have been developed and calibrated based on cross-sectional TEM data. Using these models then, and the surface profile of the buried defect as indicated in the SEM and AFM images, the exact nature of the buried defect is “recovered”. Knowing the height, shape, and location of the bump or pit defect then allows estimation of its printability impact in DPS. Furthermore, this also enables computing changes that could be then made to the absorber pattern in order to compensate for the buried defect printability, i.e., in Luminescent’s Multi-layer Defect Compensation (MDC). This technique of inverting to the shape and height of the buried defect, can also be refined later once EUV aerial images, i.e., AIMS, are also available.

While defectivity on EUV masks is currently the #1 concern in its high-volume adoption, disposition of the detected defects to EUV conditions is also very crucial. The proposed disposition techniques using Computation Lithography can be used in combination with print-tests to make the overall EUV mask defect handling flow manufacturable.

8166-09, Session 4

Mask cycle-time reduction for foundry projects

A. P. Balasinski, Cypress Semiconductor Corp. (United States)

Key deliverable for foundry projects is low cycletime. Building new and maintaining existing products by mask changes involves logistical effort which could be reduced by standardizing communication procedures and tools. As an example, a typical process of taping out can take up to two weeks, to align among the database handling (2 days), mask form completion (2 days), management approval (2 days), PO signoff (2 days), JDV signoff (2 days), alignment with silicon online (up to several weeks). In order to reduce the impact of these delays, we are proposing a unified online system which should perform the following functions: enable database edits, automatically run final verifications, providing links to management and PO approvals, standardize mask grade information, capture all the required mask information, and enable automated JDV review with engineering signoff if required. This type of automation is necessary to deal with the growing number of semiconductor products manufactured at a limited number of advanced fabs. In this paper, we will prove that the cycletime may get reduced by at least 50% for the example 2 week schedule.

8166-11, Session 4

The novel CD MTT prediction system in photomask fabrication

J. Chun, E. Park, S. Kim, C. Kim, O. Han, Hynix Semiconductor Inc. (Korea, Republic of)

It is very difficult to mass-produce photomask unlike semiconductor fabrication. Basic system for photomask is small quantity batch production, so it is an important work to correct CD mean to target (MTT) accurately. The factors (like Blank, e-beam writing, develop and dry-etch etc) that have a decisive effect on CD performance are various and constantly changing. On this account, before photomask fabrication, it is necessary to predict expected CD values and to control the condition of e-beam writing to reflect the calculated figures. In the case of photomask, however, the ratio of photomasks that have similar CD trend is very low (under 5%, AVE) and reference samples for analysis of CD MTT are few. For this reason, it becomes difficult to analyze expected CD MTT and finally this problem causes decreasing yield.

In this paper, we introduce the novel CD MTT prediction system to increase yield in photomask.

Each photomask has different correction values (e-beam dose or data bias) and measured CD includes both correction value and real CD value. So, though CD MTT of all samples is basically targeted at “0”, measured original CD data is hardly available to analyze total CD trend of the photomasks. To solve this problem, we had studied how to change original data for making effective samples from CD data of all photomask and how to analyze modified data accurately for predicting expected CD value. Finally, the system that is able to predict expected CD data was completed. Through this system, it is available to control correction values of each layer exactly for meeting specification of CD MTT and process yield improved by approximately 10% in comparison with manual analysis of expert engineers.

8166-12, Session 5

More than monitoring: advanced lithographic process tuning

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Critical dimensions (CD) measured in resist are key to understanding the CD distribution on photomasks. Vital to this understanding is the separation of spatially random and systematic contributions to the CD distribution. Random contributions will not appear in post etch CD measurements (FICD) whereas systematic contributions will strongly impact FICD. Resist CD signatures and their variations drive FICD distributions, thus an understanding of the mechanisms influencing the resist CD signature and its variation plays a pivotal role in CD distribution improvements.

Current technological demands require strict control of reticle CD uniformity (CDU) and the Advanced Mask Technology Center (AMTC) has found significant reductions in reticle CDU are enabled through the statistical analysis of large data sets. To this end, we employ Principle Component Analysis (PCA) - a methodology well established at the AMTC - to show how two different portions of the lithographic process contribute to resist CD variations. One portion centers on photomask blank preparation prior to lithography, while the other represents a difference between two very similar 50kV direct write pattern generators (PG). Resist CD variations were markedly changed by modulating the photomask blank preparation and/or the selection of a dedicated PG. Both lithographic process modulations led to improved resist CDU on test reticles in two different chemically amplified resist (CAR) processes.

8166-13, Session 5

Mask topography effect modeling in the context of source and mask optimization

C. Pierrat, IC Images Technologies, Inc. (United States)

Extension of optical lithography can be achieved by more and more precise optimization of the overall lithography system used to create wafer images. Improvements can be achieved by individual optimization of each fabrication steps such as for example the resist processing but further gains are made by a more global approach along the lines of source-mask optimization. The resulting mask images created by source-mask optimization software tools are creating a new challenge for the lithography simulation community regarding the accurate modeling of mask topography effect.

Recently, we have implemented a fast and accurate mask topography model and verified it with simple 1D and 2D test structures [1,2].

In this paper we will investigate the accuracy of this new mask topography model for a broad variety of patterns such as the one created by inverse lithography and source mask optimization tools. One particular aspect of this study is to evaluate the impact of mask corner rounding on the model accuracy.

[1] Pierrat, C., Proceedings of SPIE Vol. 7823, 782330 (2010).

[2] Pierrat, C., Proceedings of SPIE Vol. 7973, 797342 (2011).

8166-87, Session 5

Mask CD-SEM image contour extraction for production wafer simulation

T. Dam, D. Chen, H. Chang, N. Corcoran, P. Yu, L. Pang, Luminescent Technologies, Inc. (United States); C. Chen, R. Lai, L. Tuo, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

A wafer's printed CD error can be impacted by unaccounted mask making process variation. Unaccounted mask CD and/or corner rounding could alter the intended drawn mask pattern contributing to a wafer's printed CD error. During OPC wafer calibration, average mask bias and corner rounding can be accounted for in the OPC model, but random local mask making process variations or mask-to-mask variations can be difficult to account in such model calibration. Thus when a wafer's CD has error, it can be difficult to determine if the general root cause was due to mask making, OPC inaccuracy, wafer processing or all combinations. To isolate the mask making error component, an in-line monitoring application was developed to extract accurate mask CD and rendered mask polygon contours from collected mask CD-SEM images. Technical information will be presented on the challenges of accurately extracting information from SEM images. In particular, discussions will include SEM image calibration, contour extraction, and general image processing to account for mask SEM aberrations (translation, rotation, & dilation), tool-to-tool variation, vendor-to-vendor variation, run-to-run variation, and pattern-to-pattern variation. After accurate mask SEM contours are obtained, lithographic simulations were then performed on extracted polygon contours to determine the impact of mask variation on wafer CD. This paper will present detail information about this Wafer CD (WCD) application and its results, which was proven to achieved 0.5 nm accuracy across multiple critical layers from 28 nm to 40 nm nodes on multiple CD-SEM tools over multiple mask shop locations.

8166-88, Session 5

PPF-Explorer: pointwise proximity function calibration using a new radial symmetric calibration structure

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E-beam patterning encounters growing challenges to meet the requirements of current and future semiconductor technology nodes of 32nm half pitch or below. The reason for this issue is the physical characteristic of the whole transfer process including the e-beam blur, electron scattering and resist effects. These effects cause an unavoidable blurring of the intended shapes. Common proximity effect correction algorithms can correct the CD deviations caused by this blurring but are not capable of preventing the significant reduction in pattern contrast and process window when switching to smaller technology nodes. There are promising approaches for contrast enhancing proximity effect correction concepts, which to a certain extend can compensate this decrease of pattern contrast and process window. To nevertheless enable a stable patterning great efforts are put into decreasing the errors of all involved technologies.

The described transfer process blurring is usually described by a so called process proximity function (PPF) and mostly approximated by a superposition of two or more Gaussian functions. All proximity effect correction algorithms use that PPF to perform their correction. Thus, an accurate determination of that PPF contributes to reducing the error budget of the proximity effect correction scheme. Several methods for PPF calibration have been introduced in the past. Some are based on modelling the transfer process and performing Monte Carlo simulations. Another common approach is to design and expose calibration patterns, measure the results and obtain the process proximity function as the result of a simulation based fitting with respect to an assumed function model such as for instance a sum of Gaussian terms.

This paper describes the newly developed PPF-explorer method for pointwise proximity function calibration which is based on the exposure and evaluation of new calibration layouts. Following the common assumption that a process proximity function is radial symmetric, we use radial symmetric calibration layouts.

This calibration structure allows determining the amount of energy deposition in a circle of a given radius, being the radial integral of the process proximity function. Here, no fitting is necessary. The pointwise PPF can then be extracted from the determined radial integral values. Using this method the PPF can be characterized down to a radius of about 150nm or below. The inner PPF area is modelled by Gaussian terms which are calibrated by means of an additional calibration structure.

Further, first very promising calibration results obtained by test exposures are presented. They show some accordance with the process proximity function calibrated using an available PPF-calibration tool but also some systematic differences indicating potential PPF-calibration improvements due to the new method.

8166-14, Session 6

OPC modeling and correction solutions for EUV lithography

J. C. Word, M. Lam, C. Zuniga, Mentor Graphics Corp. (United States); M. Habib, Mentor Graphics Egypt (Egypt)

The introduction of EUV lithography into the semiconductor fabrication process will enable a continuation of Moore's law below the 22nm technology node. EUV lithography will, however, introduce new and unwanted sources of patterning distortions which must be accurately modeled and corrected on the reticle. Flare caused by scattered light in the projection optics result in pattern density-dependent imaging errors. The combination of non-telecentric reflective optics with reflective reticles results in mask shadowing effects and a so-called rotated illuminator effects. Reticle absorber materials are likely to have non-zero reflectivity due to a need to balance absorber stack height with minimization of mask shadowing effects. Depending upon placement of adjacent fields on the wafer, reflectivity along their border can result in inter-field imaging effects near the edge of neighboring exposure fields. Finally, there exists the ever-present optical proximity effects caused by diffraction-limited imaging and resist and etch process effects. To enable EUV lithography in production, it is expected that OPC will be called-upon to compensate for most of these effects. With the anticipated small imaging error budgets at sub-22nm nodes it is highly likely that only full model-based OPC solutions will have the required accuracy. The authors will explore the current capabilities of model-based OPC software to model and correct for each of the EUV imaging effects. Modeling, simulation, and correction methodologies will be defined, and experimental results of a full model-based OPC flow for EUV lithography will be presented.

8166-15, Session 6

High-speed mask inspection data prep flow based on pipelining

S. H. Kim, D. Hung, Synopsys, Inc. (United States); P. Liu, J. E. Sier, KLA-Tencor Corp. (United States)

Mask manufacturers are continuously challenged as a result of the explosive growth in mask pattern data volume. The IO bandwidth in commercial computers has not kept pace with the processing power or growth in the mask data volume. If IO bottlenecks are not anticipated and removed in a streamlined manner, manipulation and transfer of such large data sets can significantly limit scalability and increase the time spent performing mask data preparation for inspection.

In this paper, we present a new pipelined approach to mask data

prep for inspection which significantly reduces the data prep times compared to the conventional flows used today. The focus of this approach minimizes IO bottlenecks which enables higher throughput on computer clusters. This solution is optimized for the industry standard OASIS.MASK format to take advantage of its localized data organization and efficient data representation.

These enhancements in the data processing flow, along with optimizations in the data preparation system architecture, offer a more efficient and highly scalable solution for mask inspection data preparation.

8166-16, Session 6

QoR analysis of fractured data solutions using distributed processing

D. S. S. Bhardwaj, N. R. Guntupalli, R. R. Pai, N. P. Bhat, SoftJin Technologies Pvt. Ltd. (India)

Mask shops perform the QoR analysis of the fractured data by measuring the quality of the various basic metrics like the shot count, sliver count, smashed figure count, file size, shot perimeter, sliver perimeter, number of thin slivers etc. Mask shops also need to compare different fracture solutions to arrive at the better solution for their manufacturing standards. The different fracture solutions may be needed to be compared against each other either while evaluating different MDP tools or while tuning the various control parameters of a given MDP tool.

Other than the basic metrics mentioned above, the QoR of fractured data is also judged upon more advanced quality metrics like the number of CD splits, number of embedded and shoreline slivers as well as the lengths of embedded and shoreline slivers. Computation of these advanced metrics involves complex and compute-intensive algorithms, especially because the fractured mask data sizes have already reached hundreds of GBs. Hence, an efficient distributed processing solution with fast turn-around-time is required to measure the overall QoR metrics of fractured data solutions. This paper clearly describes the definitions of various QoR metrics and then describes parallelizable schemes to measure these QoR metrics.

Another important QoR metric of the fractured data is the orientation-independent fracturing uniformity. Fracturing uniformity plays a significant role in ensuring CD uniformity. However, at present, there are no clear criteria to measure the metric of fracturing uniformity. Hence, this quality metric is often ignored while evaluating the fractured data generated by any MDP software. This paper suggests a criterion to define the fracturing uniformity and then proposes a method to find out the amount of fracturing uniformity in a fracture solution.

Apart from being independent of data format of the fractured data, the approaches proposed in this paper could be used to find the QoR of fractured data irrespective of the MDP tool which generated it. The paper describes the implementation of such a software tool, viz. NxStats (A format-independent mask data QoR analysis software developed by SoftJin Technologies) and lists out the run-time details and samples of comprehensive comparison reports generated. NxStats supports almost all popular mask data formats (viz. OASIS.MASK, MEBES©, JEOL©, VSB-11©, VSB-12©, MIC©). The objective of this software is to enable mask shops to unambiguously evaluate the QoR of fractured data generated by different MDP software tools across a set of sample real-life designs and to ascertain that the comparison is done in an objective, unbiased and quantifiable manner.

8166-17, Session 6

Reducing shot count through optimization-based fracture

T. Lin, Mentor Graphics Corp. (United States)

The increasing complexity of RET solutions with each new process node has increased the shot count of advanced photomasks. In particular, the introduction of inverse lithography masks represents a significant increase in mask complexity. Although shot count reduction can be achieved through careful management of the upstream OPC strategy and improvement of fracture algorithms, it is also important to consider more dramatic departures from traditional fracture techniques. Optimization based fracture allows for overlapping shots to be placed in a manner that allows the mask intent to be realized while achieving significant savings in shot count relative to traditional fracture based methods. We investigate the application of optimization based fracture to reduce the shot count of inverse lithography masks, provide an assessment of the potential shot count savings, and assess its impact on lithography process window performance.

8166-18, Session 6

Application of signal reconstruction techniques to shot count reduction in simulation driven fracturing

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Resolution enhancement techniques such as Optical Proximity Correction (OPC) have enabled the semiconductor manufacturing industry to continuously shrink the critical dimension of integrated circuits. This is at the cost of increasingly complex masks and processing techniques in addition to excessively long write times. Pixel based OPC results in masks with complex curvilinear shapes rather than rectangles. Current approach to manufacture such masks with traditional Variable Shape Electron Beam (VSEB) mask writing tools consists of (a) approximating the curvilinear shapes with a rectilinear polygon, and (b) partitioning the rectilinear polygon into rectangular or trapezoidal shots. This process results in an explosion of shot count and loss of optimality of the OPC solution.

In this work, we propose an alternative fracturing approach to minimize mask write time, whereby the shot location, size, and dose are directly determined from the curvilinear OPC output. In doing so, we model the resist with a fixed threshold step function, and the proximity effect by convolution with the scattering filter, namely, a sum of Gaussians, and allow for overlap between the shots. Our approach is to use results from reconstruction of bandlimited signals from level crossings to recover the resist energy from the mask contour. Next, we solve for the dosage profile by deconvolving the resist energy with the scattering filter. This results in a dosage profile which is then approximated with a series of shots using a greedy matching algorithm. This greedy algorithm is inspired by the matching pursuit algorithm in image and video compression whereby a dictionary of basis functions is searched to find the position and amplitude of atoms in order to approximate an image.

Next, we refine the shot dosage and location by sampling the mask contour and computing the influence of each shot on the sampled points of the contours. By solving the resulting least squares problem, we can determine the best dose for a given shot location. Finally, we heuristically update the location of the edges for each shot by computing the edge placement error between the simulated and desired contours. The algorithm may be repeated to generate more accurate shot placement and shot description.

A salient feature of our approach is the capability to produce desired resist contours with arbitrary degrees of approximation. In particular, the approximation error of the resist contour is an input parameter to our proposed method that directly controls the shot count. Thus, it is possible to tradeoff between the two in a systematic way. This sets apart our approach from existing approaches such as [1].

We provide simulation results comparing the shot count and approximation error between our proposed approach and that of commercially available fracturing packages for a number of layouts.

[1] Harold R. Zable, Aki Fujimura, Tadashi Komagata, Yasutoshi Nakagawa, John S. Petersen, “ Writing “wavy” metal 1 shapes on 22 nm Logic Wafers with Less Shot Count” SPIE Microlithogrpahy 2010.

8166-19, Session 7

SMO applied to contact layers at the 32-nm node and below with consideration of MEEF and MRC

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Experimental results presented here demonstrate that masks optimized to maximize contrast or depth of focus may be far from optimum when we also consider MEEF. The reason for this is easily understood in the case of contact layers. Common process windows for contacts are usually not limited by dense arrays or isolated contacts for which there is sufficient space to insert well-designed SRAFs. More commonly, the limits come from semi-dense patterns, particularly when the space between contacts is about three times the minimum allowed space. This is approximately the space for which it may be beneficial to insert an SRAF between the contacts. If an SRAF is inserted, it will increase the high spatial frequency content of the image, improving contrast and depth of focus. Because the SRAF is the smallest feature, however; the percentage change in its size for a constant mask CD error is greatest, causing MEEF to increase. To control the compromise between MEEF and other important performance factors, the cost function minimized during optimization includes them explicitly with appropriate weights. This work quantifies the compromises for contact patterns, and shows how to control them, using a combination of experiments and computational lithography.

The solution must comprehend two other factors: MRC and side-lobe suppression. MRC introduces a discontinuity by imposing a minimum width on SRAFs. As the space between a pair of contacts increases, we cannot go smoothly from no SRAF to SRAFs of increasing width, but must switch abruptly from no SRAF to one large enough to pass MRC. Just as MRC sets the minimum size for SRAFs, side-lobe suppression sets the maximum. Together, these two considerations establish the allowable range of sizes for each SRAF. Here we show how much these constraints affect performance of optimized masks.

Because mask optimization alone has inherent compromises and is subject to constraints, we naturally look for other degrees of freedom to improve lithography process windows. Two considered here are illuminator optimization and mask bias, which effectively reduces to freedom to adjust exposure time. Adding the illuminator to the optimization (SMO) improves performance for very dense features, for which available space limits what is possible if only the mask is optimized. By solving for the optimized masks for different exposure times we change the sizes of the mask patterns relative to their corresponding targets. This affects all of the characteristics that we are optimizing, but especially MEEF, as it permits us to enlarge the small mask apertures that are proportionally affected most by mask CD errors. In some cases, the larger apertures may also suffer from fewer MRC constraints. Combining SMO with freedom to adjust effective mask bias in this fashion offers the best results.

8166-20, Session 7

Evaluation of the accuracy of complex illuminator designs

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Off-axis illumination is a commonly used resolution enhancement method in optical lithography. The design of illuminators has become increasingly complex, progressing from simple circular illumination to annular, multipole, and finally computer-optimized pixellated illumination sources. These complex illuminator designs are physically generated using a variety of different devices, such as simple stencil apertures, diffractive optical elements, programmable micro-mirror arrays, or patterned filters fabricated from partially transparent light absorbers. Differences between the physically realized illumination and the original illuminator design might be expected to affect the accuracy of the aerial image projected by the optical system using the illuminator. In this presentation we report on a series of measurements to quantify the accuracy of illuminators used in an Aerial Image Measurement System (AIMS).

A series of progressively less accurate approximations to the design illumination was used to evaluate the changes in the aerial image, induced by the illumination errors. Photomasks with programmed defects over a range of sizes were used to evaluate the various illuminators. It was found that different levels of illumination error could produce changes in the AIMS sensitivity to the programmed defects.

The AIMS response to programmed defects under different illumination conditions was compared to the results of lithographic simulation software. Several effects contributing to the aerial image measurements were modeled, including mask fabrication errors (corner rounding), high numerical aperture vector effects, three-dimensional electromagnetic field effects, and lens aberrations.

The relative importance of each of these effects was evaluated, and compared to the contribution from illumination errors.

8166-21, Session 7

Double patterning from design enablement to verification

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[Design enablement]

A significant obstacle in alt-PSM days is the lack of an effective feedback mechanism for design errors that stem from alt-PSM considerations. For LELE DP to be successfully accepted by the design community, an effective DP conflict feedback mechanism is needed. We will present the various DP conflict feedback mechanisms we have in place, and how they can help designers pin-point conflicts, guarantee conflict resolution if a highlighted few number of places are corrected.

[P&R]

In placement -- Even if the IP (library cells) are designed to be DP clean, placement of these IP can cause coloring problems on M1. DP friendly libraries can only guarantee that there is no DP conflict between different rows. However, for the same row placement, legalization problems could occur between adjacent cells. The placement engine needs to be aware of the assumptions made during IP cell design and must be smart about using the various placement directives provided by the library designer. For example, the directives could be constraints to the placer for adjacent cell orientations, colors on cell boundaries, etc. The placer must understand such constraints and either flip violating cells or move them away from each other.

In routing -- The router aspect of DP is much more complicated. There are several choices of LELE and the cut allowances leading to different approaches. In addition to repair capabilities in the presence of conflicts, detail router need to have prevention rules to avoid typical DP violations. It requires an built-in coloring mechanism to address context dependent situations in an fast & efficient manner. DP also introduces new effects in detail routing world - for example, window based search & repair cannot be verified locally due global nature of DP conflicts. Finally, because of the close interaction with the manufacturing world, the P&R engines must be capable of natively invoking signoff DP verification engines for a more convergent design and manufacturing closure.

[OPC]

In LELE DP, due to the inevitable line end shortening and the fact that two etch steps are used to achieve the single original input layer, concerns of where an input geometry can be cut, how to ensure

sufficient overlap at position cut, and the consistency between them are critical. With model difficulty around line ends, a hybrid mechanism of rule and model based overlap generation, indeed provides the best of both worlds and at the same time without little compromise to speed.

[Verification]

Due to the two litho-etch steps, mask misalignment has become a genuine concern and needs to be considered during verification. Further complicating the situation is that as high frequency information is lost during each imaging step, the image after litho-etch is rounded. Such rounding exacerbates the pinching risk, and can introduce sharp angles which are susceptible to electro-migration. We will present how the OPCVerify engine has been enhanced to check for pinching and bridging in presence of DP overlay errors and acute angles.

8166-22, Session 7

Study on the design rule verification procedure of semiconductor memory devices by using design-based metrology

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Design rules are communication systems between process engineers and design engineers. So the main purpose of design rule is to provide process characteristics such as lithography limitations to the design engineers. Lithography limitations usually evaluated in minimum pitch, so design rules are often expressed in terms of minimum size of simple patterns. Generally, minimum size design rules have been well used for designing a chip. However as the chip size shrinks, smaller design rules are required and complex lithography illumination systems are used. In this case, minimum size rules become no longer suitable for optimum design, because the chip has various shapes of design patterns. And the shapes differences often show different lithography properties. Therefore verifying many types of different patterns are required for setting up design rules. But it is not easy to verify a large number of different patterns. For that reason, sometimes only a worst-case pattern was evaluated and the “safe design rule” was defined to guarantee the most of pattern feasibility. The safe design rule is literally safe for lithography but it is not good for chip size reductions, because it is a waste of lithography performance in other design patterns. For a chip size reduction, design rules considering various patterns were needed and it was usually introduced by model-based design rule. But the model-based design rules are often risky to use for a mass production design without ensuring model accuracy through the detailed verification procedures.

In order to guarantee design rules, real wafer pattern inspection must be carried out for verifying the pattern feasibility and process margin. But normal CDSEM measurements are not preferable for that purposes because of its time-consuming pattern-by-pattern inspection method.

In order to overcome the difficulties of inspecting many types of patterns for design rule verification procedures, we introduce Design Based Metrology (DBM) of Nano Geometry Research, Inc. It is a die to database (DB) inspection system which can compare the pattern on wafer to the design layout. This metrology system provides a large inspection field size which makes it possible to measure the CD of all the features in a test chip at a fast speed.

In our work, we tried to figure out as many types of design patterns of devices as possible and investigated lithography characteristics of each design patterns. In the beginning, we carried out DRC (Design Rule Check) for a gate poly layer of 30nm-node DRAM layout in order to sort out various types of design layouts which may be a potential design rule fail point. And then we applied pattern analysis tool to pick out distinctive types of design patterns from the DRC results. By doing this, we could possibly select several types of design layout from the classified patterns. And we have drawn test patterns which reflect the lithographic and design characteristics of real chip design. The test patterns were consist of simple line and space patterns with different duties and different overlap length, line-end to edge patterns, line-end to line-end patterns, and line-end to edge with L-shaped and U-shaped edge. We evaluate the test pattern with real wafer process. All the test patterns could be inspected within a few hours by using design based metrology. From the measurement CD data and the inspected image, we could decide a specific criterion which defines safe or dangerous design size and analyze key layout parameters which made those differences such as neighboring line-width and assist features. In lithographic point of view, the wide resist pattern without assist features make the space pattern prone to bridge. And undoubtedly that phenomenon can be seen in our experiments. And we also figured out the lithographic behavior of line-end patterns by line-end width change. From all these measurement results, optimized design rules could be introduced and verified successfully by suggested procedure using design based metrology system.

8166-23, Session 8

Holistic lithography for EUV: NXE:3100 characterization of first printed wafers using an advanced scanner model and scatterometry

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We report holistic lithography results of NXE:3100 scanners with impact for EUV mask-making. The work consists of 1) detailed modeling of the scanner and mask, 2) NXE wafer exposures to detect EUV imaging effects, and 3) high-resolution CDU characterization by YieldStar angular-resolved scatterometry.

The imaging behavior of ASML’s first prototype manufacturing platform NXE:3100 has been modeled in detail for computational lithography purposes. The model includes the optical system (pupil, slit, reflective projection lens), EUV-specific flare effects (long-range), the EUV mask properties, and other NXE:3100 hardware components. Accurate predictive modeling is of high importance for ASML’s customers to generate reliably (OPC) corrected and full-chip litho verified masks for a successful introduction of EUV to their fabs.

We present printed wafer results using a special mask that was designed by ASML and manufactured by Samsung’s captive mask shop. The mask measurements show excellent uniformity and quality. The mask was designed to be able to characterize the specific flare details of EUV lithography such that parameters in the model can be extracted. Furthermore, the measurements yield information on the quality of the projection optics in the NXE:3100.

The wafers were measured for CD uniformity by an ASML YieldStar S-100 scatterometry tool and by a Hitachi CD-SEM. After careful analysis of the large set of YieldStar data, the results reveal the predicted imaging effects of lithography such as flare details and residual black-border reflections from the mask absorber stack. Furthermore, the results allow a calibration of system parameters such as a precise determination of the very small fraction of out-of-band DUV light that reaches the wafer on the demonstrator NXE:3100 scanner. We will show OPC results that apply the corrections for all these effects on the mask, as well as the impact on process-window across the field.

We will conclude with 1) an explanation on the differences in EUV-OPC compared with iArF-OPC, 2) the computational litho roadmap to support the higher-NA NXE:3300 platform for high-volume

manufacturing, and 3) recommendations for EUV mask blank properties.

8166-24, Session 8

Development status and infrastructure progress update of aerial imaging measurements on EUV masks

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The high volume device manufacturing infrastructure from the 22nm node and below based on EUVL technology requires defect-free EUV mask manufacturing as one of its foundations. The EUV Mask Infrastructure program (EMI) initiated by SEMATECH has identified an actinic measurement system for the printability analysis of EUV mask defects to ensure defect free mask manufacturing and cost-effective high-volume EUV production as an infrastructural prerequisite for the EUVL roadmap.

Based on the results at the end of 2010 of a concept and feasibility study performed by Carl Zeiss under funding of the SEMATECH and the Research Foundation of the State University of New York (USA), providing a feasible concept for the AIMS. EUV satisfying the application requirements for 16nm defect printability review; a development program for the AIMS. EUV has been initiated between Carl Zeiss and the SEMATECH together with the EMI program with the target of a commercialized tool available in 2014.

In this paper we will present the status of the progress of the design phase of this development and an infrastructure progress update of the EUV Mask defect printability review.

8166-25, Session 8

EUV mask preparation considering blank defects mitigation

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For the successful implementation of extreme ultraviolet lithography (EUVL) technology for the future semiconductor fabrication process, EUV mask technology is considered to be one of the most critical issues. The high reflection of ultraviolet requires the blank to be a multilayer (ML) structure, usually a stack of 40 to 50 Mo-Si alternating layers. Each of the layers is a discrete processing step with a cumulative opportunity for adding defects. And it is quite possible that EUV blanks will not achieve zero defectivity by the time they are needed for production[1]. According to blank-defect inspection technology, the number of defects increases with the decrease of the sizes. Those large defects bigger than feature size should be avoided by rotating and shifting layout in the blank[1], but the smaller ones can be accommodated under the absorbers which are used to make features on the blank[2]. If some blank defects cannot be avoided or accommodated, they might cause failure in the final mask, such as bridge or broken problems. For any design, there is an optimal orientation and position to place it onto a given blank whose defect distribution is already inspected, such that the total area of problematic defects is minimized.

From the perspective of EUV mask manufacturer, all the blanks are fabricated and inspected before circuit designs from customers are provided. And depending on the production volume, some designs might require more than one mask because the lifetime of EUV masks is much shorter than that of traditional masks used in Deep UV. Before the EUV mask fabrication, blanks and designs should be matched to each other while minimizing the possible failures caused by blank defects at the same time.

In this paper, we present a cost-effective optimal methodology to find the optimal matching between a set of blanks and a set of design layouts. Each pair of layout and blank reports a total problematic defect area. For a certain pair, by properly rotating and shifting one layout on the blank, we can minimize this problematic area with our fast defect mitigation algorithm and report the minimum total problematic area as the cost of this pair. Then we adopt an optimal min-cost max-flow algorithm to find the optimal match between those blanks and layouts.

Reference

[1] John Burns, Mansoor Abbas. “EUV mask defect mitigation through pattern placement.” Proc. SPIE, Vol. 7823, pp. 782340-782340-5 (2010).

[2] Chris H. Cli_ord, Tina T. Chan, Andrew R. Neureuther, Ying Li, Danping Peng, Linyong Pang. “Compen-sation methods using a new model for buried defects in extreme ultraviolet lithography masks.” Proc. SPIE, Vol. 7823 78230V-1 (2010).

8166-26, Session 8

EUV mask inspection field applications: status update

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The EUV mask poses a significant inspection challenge to a DUV based inspection tool as it constitutes significant changes compared to ArF masks. In particular, it has a multilayer reflective (ML) stack, covered by patterned absorber materials at sub wavelength thickness, carrying sub-wavelength size features. In this paper, we report on recent advancements that extend the capability of a 193 nm mask inspection tool to meet pre-production requirements for the 28nm HP or 15nm Logic node. EUV mask pattern design is unique since they incorporate flare correction and H/V bias. Meeting the reticle qualification requirements requires development of a number of novel capabilities for mask inspection, including the use of multiple off-axis Illumination conditions, advanced proprietary algorithms and use of an advanced focus control.

8166-27, Session 10

A study on irregular growing defect mechanism and removal process

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Main Topics of a photomask have been CD(Critical Dimension), Overlay and Defects. In side of defects, technique suppressing growing defects which are occurring on a mask surface becomes as important as defect control method during mask manufacturing process. Conventional growing defects arise out of combination of sulfuric ion on a mask surface and environmental facts such as pellicle ingredient, humidity and etc. So Mask cleaning process was driven to reduce sulfuric acid on a mask surface which source of growing defects. And actually various cleaning process has been developed through the elimination of sulfuric acid such as DI, O3 cleaning. Normally Conventional growing defects are removed using DI, SC1 or SPM cleaning according to incidence. But recently irregular growing defects are occurred which are completely distinct from conventional growing defects. Interestingly, irregular growing defects are distributed differently from conventional on a mask. They spread in isolated space patterns and reduce the transmittance so that space pattern size continuously decreased. It causes Wafer Yield loss. Furthermore, irregular growing defects are not fully removed by cleaning which is traditional removal process. In this study, we provide difference between conventional and irregular growing defects based on its characteristic and distributed formation.

In addition, we present and discuss removal and control technique about irregular growing defects. For elemental analysis and study,

diverse analysis tool was applied such as TEM for checking Cross-Section, AFM for checking the roughness of surface, EDAX, AES, IC for analyzing remained ions and particles on the mask and AIMS.

8166-28, Session 10

In situ UV process optimization for resist removal and final cleaning of EUV masks

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EUV mask structures are optimized for extreme ultraviolet (EUV) light, which is reflected from the mask surface to make patterns on the wafer. To enhance EUV lithography performance, EUV mask structures are made up of various layers of materials, and each layer has a certain role in EUV patterning. It has been considered an important subject to understand how the original properties and surface morphologies of each layer change during mask fabrication and EUV exposure processes.

EUV masks will likely undergo more cleaning cycles than optical masks during their lifetime, since in EUV lithography a pellicle cannot be used to protect the mask surface. This requires that EUV masks utilize cleaning processes that can minimize degradation of their layers during cleaning and thus help to extend their lifetime. The conventional SPM cleaning process is known to cause negligible damage on EUV mask films down to the 22 nm node, but it has limited ability to remove thick carbon contamination from ruthenium surfaces. It is believed that UV-radiated cleaning media (i.e., in situ UV cleaning processes) recently developed to replace conventional SPM are capable of improving organic removal and mask film loss during EUV mask cleaning, although they have not yet been fully optimized.

In this paper, we will present the process windows of various cleaning media activated by in situ UV for removing post-etch resist, carbon contamination, and particles while minimizing loss of the ruthenium capping, tantalum-based absorbers, and anti-reflective coating (ARC) layers. Also, changes in the chemical composition and surface adhesion properties of each layer during new acid-free cleaning processes will be examined. Based on this information, EUV mask lifetime for post-etch or final cleaning using an in situ UV POR will be determined.

8166-29, Session 10

MegaSonic cleaning: possible solutions for 22-nm node and beyond

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Photomask design and fabrication is becoming more complex with each new technology node. Additional imaging improvement strategies (SRAFs, HT etc.) must be adopted to extend the technology but, at the same time these enhancement techniques further increase the complexity and fragility of the photomask. According to the latest ITRS roadmap, SRAFs will shrink to a size comparable to the defect allowed for that technology node. High aspect ratio features with sensitive interface are prone to physical force damage and the need to control the energy in photomask cleaning has never been deemed as urgent as today. The lifting force needed to remove soft particles (typically adhered to the surface by van der Waals forces) is less than the interface strength and therefore theoretically, a process window for damage-free cleaning exists. Current state-of-the-art physical force technologies seem to lack the level of precision and control to match the available process window. However, with a better understanding of the MegaSonic acoustic phenomenon and its interaction with contaminant particles and photomask features, the process window for damage-free physical force cleaning can be achieved. MegaSonic energy transfer to the photomask surface is indirectly controlled by process parameters that provide an effective handle to physical force distribution. In this paper we will specifically present the effect of higher frequencies (3 & 4 MHz) and media gasification on pattern damage and cleaning efficiency. An innovative concept of resonance cavitation in MegaSonic cleaning will be discussed and relevant data will be presented. All damage and cleaning results will be correlated to energy and cavitation measurements for tested conditions.

8166-30, Session 10

Extending CO_2 cryogenic aerosol cleaning for advanced photomask cleaning

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Cryogenic CO2 aerosol cleaning being a dry, chemically-inert and residue-free process is a very attractive cleaning option for the mask industry to achieve the requirement for removal of all printable soft defects on lithography masks. A CO2 cluster is formed by sudden expansion of liquid from high to almost atmospheric pressure through an optimally designed nozzle orifice. Then it is directed on the contaminants for momentum transfer and subsequent removal from the mask substrate without damaging the fragile features present. Unlike wet cleaning, there is no degradation of the mask after processing with CO2, i.e., no CD change, no transmission/phase losses, or haze formation for optical masks. This implies the advantage of no restriction on number of cleaning cycles with CO2, compared to conventional wet cleaning. CO2 aerosol cleaning has already been extended to do full mask Final Clean in production environments. Phase Doppler Anemometry (PDA) is being utilized to design and qualify nozzles with the optimum snow properties (size, velocity and flux) required for specific applications.

Previously, for optical masks, removal of all soft defects without damage to the fragile features, while ensuring zero adders (from the cleaning and handling mechanisms) down to a 50nm printability specification have been successfully demonstrated by our group using CO2 aerosol on advanced node patterned masks. In addition, CO2 aerosol cleaning technique is being utilized to remove debris from Post-RAVE (AFM) repair of hard defects on lithography masks, in order to achieve the goal of no printable defects on these masks. It is expected that CO2 aerosol cleaning can be extended to EUV masks. Recently, our group has experimentally demonstrated that a 50× cleaning on the fragile Ru film on the EUV Front-side, resulted in no appreciable reflectivity change, implying that no oxidation of the Ru film occurs.

Pellicle glue residue removal using CO2 aerosol cleaning was also investigated. Usually, the residue left over after the pellicle has been removed from returned masks (after long term usage/exposure in the wafer fab), requires a very aggressive wet clean, that drastically reduces the available budget for mask properties (CD, phase/transmission). CO2 aerosol cleaning can be utilized to remove the bulk of the glue residue very effectively, while preserving the mask properties. Preliminary results showed that the optimized nozzle for Optical Front-side was not at all effective. This application required a differently designed nozzle to impart the required removal force for removing the sticky glue residue. A nozzle was qualified that resulted in PRE in the range of 92-98%. Results also include data on a patterned mask that was exposed.

In this paper, the two new areas of focus for CO2 aerosol cleaning are: a) Ru film on EUV Mask, and b) pellicle glue residue removal on optical masks.

8166-89, Poster Session

Reticle process monitoring and qualification based on reticle CDU and wafer CDU correlation

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Reticle process of record (POR) sometimes need fine tuning for some reasons such as multiple layer process, better critical dimension uniformity (CDU) or new etch chamber. The side edge and corner rounding will be varied due to the reticle processing tuned compared with previous POR. However, because the reticle critical dimension (CD) measurement is based on middle side lobe measurement or other algorithm, the reticle CD can not reflect the change of of reticle side lobe and corner rounding variation which is critical for 65nm and below technology node. Because the intra-field wafer CD is equal to both the contribution of scanner, process, reticle and metrology tool. Normally, the reticle contribution to the wafer CDU should be as small as possible, that is less than 0.33. By averaging all the wafer CD of individual features to obtain a wafer CD reference independent of feature location and wafer die, the correlation of wafer MTT and reticle MTT can be found. The correlation can accurately qualify and monitoring the tuning processing of reticle.

We have manufactured two masks of 65nm active layer using different reticle process, one using the original active layer POR process and another using a different multi-layer-reticle (MLR) process. The wafer CDU and reticle CDU correlation of two reticles are demonstrated for both isolated and dense features in vertical and horizontal direction, respectively. The same effect is demonstrated for a fine tuning POR process of 40nm metal layer showing its own wafer CDU and reticle CDU correlation for both dense and isolated structures individually. By the wafer and reticle MTT correlation, the POR reticle processing also can be evaluated. The wafer and retice CDU correlation POR process for 45nm poly and contact layers are also demonstrated in this manuscript.

8166-90, Poster Session

Contamination control of reticle SMIF pods through intelligent material selection and purification

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The semiconductor industry continues reducing the incident rate of progressive defect growth on reticles used at 193nm. Possible multiple sources indicates that reduction in haze risk includes controlling the reticle in storage and exposure environment. However, reticle users, equipment and material providers should be prepared to ensure better storage and reduce the risk of haze growth. This study continued the works previously reported by Gudeng Precision Industry, on an advanced testing apparatus recently designed and completed. We optimized the purging flow rate to reduce the running cost, also to maintain performance. Our approach was to design RSPs affected by the number and location of the ports, and material selection.

8166-91, Poster Session

Effects of cleaning on NIL templates: surface roughness, CD, and pattern integrity

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Nano-Imprint Lithography (NIL) is considered a promising alternative to optical lithography for technology nodes at 22nm hp and beyond. Compared to other advanced and complex lithography methods, NIL processing is simple and inexpensive making it a widely accepted technology for pattern media and a potential cost effective alternative for CMOS applications. During the NIL process, the template comes into direct contact with the resist on the substrate and consequently template cleanliness plays a decisive role in imprinted substrate quality. Furthermore, if the template has any form of a defect such as resist residue, stains, particles, surface scratches, chipping and bumping etc. it can lead to poor quality imprints, low yield and a decrease in throughput.

The latest ITRS roadmap has provided stringent CD, CD uniformity, surface roughness and defect control requirements for NIL templates. Any template cleaning process that is adopted must be able to remove defects while maintaining the critical parameters outlined by the ITRS. Aggressive chemistries (such as NH4OH) and strong physical force treatments (such as Megasonic) may cause damage to the template if not optimized. This paper will present the effects of cleaning treatments on template surface roughness and CD. Different chemical concentrations will be compared and an optimized process will be proposed. The effect of megasonic treatment on fragile and sensitive pattern features will be presented. Based on the results, the number of wet cleans that a template can sustain in its lifetime while maintaining surface integrity could be estimated.

8166-93, Poster Session

Study on EUV photomask resist striping and cleaning

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An advanced mask cleaning method, which has the capability of not only preserving optical properties but also high particle removal efficiency, has been developed using the combination of advantages at chemical and physical cleanings based on fully understanding the characteristics of their process.

It is known that the resist removal techniques in the ArF photomasks have SPM, Ozonized Water (O3W), Asher and so on. However, the problem that cannot correspond in the current process processed so far occurs from the material change in the substrate in the EUV photomasks. Because the problem of damaging the optical characteristic from the influence on the material of Ru occurs when these means are applied with EUV photomasks. So it is difficult to remove the resist and clean the surface on EUV photomasks.

In this report, the influence of Ru in a chemical and physical processing is evaluated, and it reports whether become a processing method for which what treatment technology is the best from the correlation with the optical characteristic.

We evaluated the surface composition change of Ru by XPS after O3W. The increase of surface oxygen atom has occurred by supplying O3W.In addition, it has been understood that the Ru film thickness has changed by the rate of about 0.1nm/min depending on the O3W process by ellipsometry. These results are corresponding to the changing trend of the optical characteristic. Therefore, we think that the processes which don't influence on the surface of Ru will not change optical characteristic of Ru mask substrate.

8166-94, Poster Session

Removing carbon from EUV photomask blanks using downstream plasma cleaning

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The fabrication of photomasks for extreme ultraviolet (EUV) lithography requires that pristine blanks and substrates are used in the process. One type of contamination found on mask blanks and substrates is carbon particles. These particles can be around 10 nm in diameter, and they will cause surface defects which will then propagate through the multilayer coating. This propagation will cause a phase defect in the reflected EUV light, which could then be printed on the wafer. Therefore, elimination of these carbon particles is critical in the fabrication of EUV photomasks.

Commercially available technology which removes carbon contamination from electron microscope chambers may also be used to remove carbon particles from mask blanks and substrates. This technology, called downstream plasma cleaning, uses low power radio frequency plasma to generate neutral radicals in a vacuum chamber. These radicals travel by convection to the area of contamination. They chemically etch the contamination, the etching reactions produce volatile species which can be pumped out of the vacuum chamber. The advantage of this technology is the gentleness of the cleaning. There is no sputter etching or heating of the surface to be cleaned; both these processes would alter detrimentally the surface of the mask blank or substrate.

A preliminary set of experiments have been performed at SEMATECH to determine the effectiveness of downstream plasma cleaning in removing carbon particles. These experiments were performed using both cleanroom air and oxygen. The results have shown that there is a reduction in particle size due to the cleaning, and they have encouraged further investigations into using this technology to remove carbon particles.

This paper will report on further experiments using downstream plasma cleaning. A new prototype of the downstream plasma cleaner will be fabricated for SEMATECH; this prototype is designed to maximize the cleaning rate while minimizing the possibility that particles from the cleaner will be added to the mask substrates and blanks. A new test bench will be made at SEMATECH for the purpose of testing the effectiveness of downstream plasma cleaning. Tests at SEMATECH will be performed with the new prototype to measure cleaning rates, see if carbon particles are eliminated in a timely manner, and check that particles are not added to the substrates by the cleaning process.

8166-95, Poster Session

Investigating the intrinsic cleanliness of automated handling designed for EUV mask pod-in-pod systems

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Extreme Ultraviolet Lithography (EUVL) is the most promising solution for technology nodes 16nm (hp) and below. However, several unique EUV mask challenges must be resolved for a successful launch of the technology into the market. Uncontrolled introduction of particles and/or contamination into the EUV scanner significantly increases the risk for device yield loss and potentially scanner down-time. With the absence of a pellicle to protect the surface of the EUV mask, a zero particle adder regime between final clean and the point-of-exposure is critical for the active areas of the mask. In addition, contamination of the scanner chuck from particles found on the backside of the mask is leading risk for scanner downtime. Consequently, control of particles and/or contamination during storage and transport must be eliminated to ensure scanner compatibility with the EUV mask. A pod-in-pod concept for handling EUV masks between various tools and storage is proposed as a means to minimize the risk of mask contamination as described above. Intrinsic cleanliness in handling the pod-in-pod system brings new challenges for the industry.

The HamaTech MaskTrackPro InSync, introduces a fully automated solution for the handling of EUV masks in and out of a pod-in-pod storage box. The InSync module is comprised of a SMIF loader, inner pod opener, handling systems for the inner pod and the EUV mask and an inner pod storage unit.

In collaboration with TNO, HamaTech investigated the intrinsic cleanliness of each individual handling and storage step of the inner pods and the EUV masks. The particle detection for the qualification procedure was executed with the Rapid Nano TNO Particle Scanner, qualified for particle sizes down to 70nm (PSL equivalent). Monitor masks were utilized for all testing.

8166-96, Poster Session

Optimized qualification protocol on particle cleanliness for EUV mask infrastructure

J. van der Donck, J. Stortelder, G. Derksen, TNO (Netherlands)

With the market introduction of the NXE:3100, Extreme Ultra Violet Lithography (EUVL) enters a new stage. Now infrastructure in the wafer fabs must be prepared for new processes and new materials. Especially the infrastructure for masks poses a challenge. Because of the absence of a pellicle reticle front sides are exceptionally vulnerable to particles. It was also shown that particles on the backside of a reticle may cause tool down time. These effects set extreme requirements to the cleanliness level of the fab infrastructure for EUV masks. The cost of EUV masks necessitates the use of equipment that is qualified on particle cleanliness.

Until now equipment qualification on particle cleanliness have not been carried out with statistically based qualification procedures. Since we are dealing with extreme clean equipment the number of observed particles is expected to be very low. These particle levels can only be measured by repetitively cycling a mask substrate in the equipment. Recent work in the EUV AD-tool presents data on added particles during load/unload cycles, reported as number of Particles per Reticle Pass (PRP). In the interpretation of the data, variation by deposition statistics is not taken into account. In measurements with low numbers of added particles the standard deviation in PRP number can be large.

An additional issue is that particles which are added in the routing outside the equipment may have a large impact on the testing result. The number mismatch between a single handling step outside the tool and the multiple cycling in the equipment makes accuracy of measurements rather complex.

The low number of expected particles, the large variation in results and the combined effect of added particles inside and outside the equipment requires a statistically well-founded test plan. Without a proper statistical background, tests may not be suitable for proving that equipment qualifies for the limiting cleanliness levels. Other risks are that a test may require an unrealistic high testing effort or that equipment can only pass for a test when it meets unrealistic high cleanliness levels.

TNO developed a model which enables setting up a qualification test on particle cleanliness for EUV mask infrastructure. It is based on particle deposition models with a Poisson statistics and an acceptance sampling test method. The test model combines the single contribution of the routing outside the equipment and contribution of multiple cycling in the equipment. This model enables designing a test which proves that equipment meets a required cleanliness level. The model predicts the testing effort. Furthermore, it gives insight in other equipment requirements on reliability. By using the test model the requried effort for particle cleanliness qualification can be minimized.

8166-97, Poster Session

EQ-10 electrodeless Z-pinch EUV source for metrology applications

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With EUV Lithography systems shipping the requirements for highly reliable EUV sources for mask inspection and resist outgassing are increasing. The sources needed for metrology applications are very different than that needed for lithography, brightness is the key. Suppliers for HVM EUV sources have all resources working on high power and will not focus on the smaller market for metrology.

Energetiq Technology has been shipping the EQ-10 Electrodeless Z-pinchTM light source since 1995[1]. The source is currently being used for metrology, mask inspection, and resist development [2,3,4]. These applications require especially stable performance in both output power and plasma size and position.

Over the last 6 years Energetiq has made many source modifications which have included better thermal management to increase our brightness and power of the source. We now have introduced a new source that will meet requirements of some of the mask metrology first generation tools and this source will be reviewed.

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[2] Horne, S. F., Besen, M. M., Smith, D. K., Blackborow, P. A., Dagostino, R., 2006. Application of a high-brightness electrodeless Z-pinch EUV source for metrology, inspection, and resist development. In: Proc. SPIE. Vol. 6151.

[3] Blackborow, P. A., Gustafson, D. S., Smith, D. K., Besen, M. M., Horne, S. F., D'Agostino, R. J., Minami, Y., Denbeaux, G., 2007. Application of the Energetiq EQ-10 electrodeless Z-Pinch EUV light source in outgassing and exposure of EUV photoresist. In: Proceedings of SPIE. Vol. 6517.

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8166-98, Poster Session

Improve the efficiency of the inspection process via a thorough control of the scanning focus

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Requirements coming from the customer, as well as internal needs of improvements consequent to the increasing complexity of the layout of the newest devices, lead to the necessity of explore all the potential improvements achievable at the mask manufacturing inspection process.

A key point to manage for the better DB inspections is that of being able to achieve a proper matching between the images to be compared, tasks which is accomplished by the tool architecture by means of a pre-swath calibration process on which the quality of the focus is playing a relevant role. From here the decision to focus on this parameter aiming of working out and evaluate a different approach to be used to set the scanning focus on the inspection tool moving from the vendor theory based on the edge speed on a specific test plate to a new one based on intensity measurements into specific features on a purposely designed test vehicle.

A matter of relevant importance for mask makers, either for the smoothness of the inspection process or for the homogeneity of the delivered products, but on which any tool vendor like providing official commitments, is that of correlating the overall performance of similar tools. This was accomplished with the new approach with two different tools achieving optical images with a similar grey scale distribution into the most critical features. Moreover, the improvement of the matching of the images being compared allows extending the usage of the tool for products for which the complexity of the layout forced the inspection with different pixels or with more advanced tools, with a positive impact either on costs or on the cycle time of the masks being delivered.

A carefully assessment-verification of the shadowing limitation induced by the frame of the pellicle was another task successfully carried out with the new methodology, with some improvement regarding the inspectable area.

The extended its usage the wider the field of application will become, but few advantages can be appreciated since the beginning: the focus will be set on a production like layer, its choice will be less depending on a human decision, it will be a simple, fast and reliable process runable at any time and at any operating level.

8166-100, Poster Session

Efficiency and throughput improvement on defect disposition through automated defect classification: enhancing yield and throughput of sub-32-nm mask technology

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The routine use of aggressive OPC at the advanced technology nodes, i.e., 40nm, and beyond, has made photomask patterns quite complex. The high-resolution inspection of such masks often results in more false and nuisance defect detections than before. Traditionally, each defect is manually examined and classified by the inspection operator based on defined production criteria. The significant increase in the number of total detected defects makes the manual classification costly and non-manufacturable. Moreover, such manual classification is also susceptible to human judgment and hence error-prone.

Luminescent's Automated Defect Classification (ADC) offers a complete and systematic approach to defect disposition and classification. The ADC engine retrieves the high resolution inspection images and uses a decision-tree flow based on the same criteria the human operators use to classify a given defect. Some identification mechanisms adopted by ADC to characterize defects include defect color in transmitted and reflected images, and background pattern criticality based on pattern topology. In addition, defect severity is computed quantitatively in terms of its size, impacted CD error, transmission error, defective residue, and also contact flux error. The ultimate classification uses a matrix decision approach to reach the final disposition. The experimental results reveal that ADC achieves production valuable performance with >90% defect code matching ratewhen compared to operator classifications, together with run-rates of 250 defects classified per minute. The automated, consistent and accurate classification scheme not only allows for faster throughput in defect review operations but also enables the use of higher inspection sensitivity and success rate for advanced mask productions with aggressive OPC features.

8166-101, Poster Session

Electron-beam EUV patterned mask inspection system

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EUV lithography is expected to begin production in 2014. Production of successful EUV photomasks requires patterned mask inspection (PMI). The ultimate PMI tool is expected to utilize actinic (EUV) illumination. Development of such a tool is expected to require three years after funding. Current test EUV masks, such as 22 nm, can be inspected using 193 nm wavelength deep UV (DUV) inspection tools similar to those currently being used for DUV masks. The DUV inspection tools may be extended for the 16 nm node. However EUV production is expected to start with 11 nm node masks which cannot be inspected with proposed DUV inspection tools. Therefore E-beam inspection (EBI) is discussed as the interim PMI method.

EBI has the advantage of high resolution and the disadvantages of low inspection speed and relative insensitivity to ML defects (in the multi-layer material). EBI inspection speed is limited by the pixel size, pixel capture rate and the number of electron columns. The pixel rate is limited by the detector time-resolution and the beam current and the detection efficiency.

Technical improvements in beam focus, secondary electron detection, and defect detection and analysis provide good performance for 22 nm node masks. We discuss the advances and show that performance can be extrapolated for 16 and 11 nm node patterned mask inspections.

We present sensitivity and false-defect frequency results of using the Holon EBI tool on 22 nm test masks and a roadmap for extending its operation for use on 16 and 11 nm node masks for inspections requiring 2-5 hours per mask.

8166-103, Poster Session

Productivity of femtosecond DUV-laser photomask repair in a real-world mask house

T. E. Robinson, RAVE LLC (United States); J. Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

A number of new technologies and processes have been developed for deep ultraviolet (DUV) wavelength and femtosecond pulsed laser repair of photomasks. These advances have been shown to improve and extend the repair of both pelliclized and non-pellicilized photomasks for both hard and soft (or nano-particle) in exhaustive testing at the factory and the end-user site. However, even the best testing is only a simulation of what a repair tool will see when brought into full production. The purpose of this work is to review some of the knowledge and experience gained in bringing the repair processes defined with manufactured defects to the more variable defects encountered in the real world. The impact of the repair technology on increases in mask house throughput and decrease in costs will also be compared to other (another laser and an advanced FIB) repair tools.

8166-104, Poster Session

Nanomachining repair for the latest reticle enhancement technologies

T. E. Robinson, RAVE LLC (United States)

In keeping with technology trends that have allowed the use of 197 nm wavelengths for nodes well beyond its intended limits, a number of new RET's have come to significant adoption in advanced lithography. These enhancement technologies include Source-Mask Optimization (SMO) and Opaque MoSi on Glass (OMOG), which are of particular focus for examination of their applicability to nanomachining photomask repair. Historically comparative repair results are shown for the OMOG absorbers which can contain a multi-layer potentially in combination with small (phase-correcting) quartz over-etches. The implementation of nanomachining with SMO photomasks encompasses a larger set of new technologies introduced in a nanomachining repair tool. These include tip shape deconvolution for improved accuracy and reproducibility in large complex patterns, many of which are non-orthogonal, and automated import of mask design data to seed the repair polygon for a pattern which may be unique on the entire mask area (i.e. no pattern reference).

8166-105, Poster Session

Parallelized automatic false defect detection using GPUs during mask inspection

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The mask inspection and review process is a vital part of mask preparation technology and consumes a significant amount of mask preparation time. As the patterns on a mask become smaller and more complex, the need for a highly precise mask inspection system with a high detection sensitivity and low number of false defects becomes greater. A low number of false defects is desirable as the results of the mask inspection are typically reviewed manually by an operator in the mask shop. However, due to various reasons, the probable mask defects identified by any mask inspection machine could include significant number of false defects. The false defects could be due to registration or focus errors between the defect and reference images (Die-to-Die or D2D comparison), CCD errors in the camera, noisy pixels etc. These false defects cannot be ignored and require the operator to review them manually before classifying them as false defects. This takes valuable time and effort of the mask inspector and increases the turn-around-time of mask inspection.

We propose a software tool which automatically detects most of the false defects generated due to registration and focus errors in the mask inspection system. It is quite common to find several thousands of defects (real as well as false defects) during mask inspection. We have observed that significant percentage of these false defects are due to registration and focus errors between reference and defect images during D2D inspection. Automatic detection of registration and focus errors requires image processing to be done on the defect images. This process is typically, time consuming. However, image processing algorithms are well suited for parallelization.

We explore the use of GPUs to speed up the false defect detection process by analyzing the defects in parallel on multiple cores of a GPU. In addition, GPUs are inexpensive, readily available and can be plugged in to any desktop computer which makes it easier to adopt. The proposed GPU based parallel false defect detection feature is integrated into Mask Defect Analysis tool - NxDAT.

8166-106, Poster Session

Studies of test pattern of electron-beam inspection for sub-2x-nm nano-imprint template development

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NIL (nano imprint lithography) template manufacturing involves chromium hard mask etch, quartz etch using chromium hard mask, remove of chromium and clean. Defectivity control is one of most challenging issues of NIL application of IC production. EBI (electron beam inspection) is the solution of the defect inspection of NIL templates. The main issue of EBI is the throughput. By designing alternating floating and ground in line-space patterns, EBI throughput can be significantly accelerate using voltage contrast (VC) defect detection.

In this study, we designed line-space EBI test patterns with different half pitch (HP) and different length. We also designed normal patterns on the template. We put some program defects on the test patterns to check the sensitivity of the EBI. EBI results show that we can

significantly improve throughput of NIL template EBI in for the process development in chromium etch and quartz etch with chromium hard mask.

8166-107, Poster Session

EUV mask e-beam inspection working conditions study

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EUV E-beam pattern mask inspection (EBPMI) have been proposed as a cost effective EUV pattern mask inspection solution for high volume manufacturing in mask shops and fabs by Applied Materials.

Electron beam inspection technology is available at present for wafers and successful feasibility sensitivity study for EUV mask, by a technology demonstration platform, published recently [1]. The feasibility study is now continues with e-beam extreme conditions verification which intends to proof the use of EBPMI for high volume manufacturing (HVM).

We examined common assumptions in the field of radiation research, regarding inelastic and elastic scattering, in relation to the accumulated radiation dose and the ebeam deposited energy on the sensitive EUV blank surface.

We concluded the study with strong evidences and provided guide lines regarding EBPMI in high volume manufacturing environment.

[1] SPIE BACUS 2010

8166-110, Poster Session

Optimization of mask shot count using MB-MDP and lithography simulation

G. Chua, GLOBALFOUNDRIES Singapore (Singapore); Y. Zou, GLOBALFOUNDRIES Inc. (United States); K. Hagiwara, D2S, KK (Japan); I. Bork, A. Fujimura, D2S, Inc. (United States)

1. Optimizing mask manufacturability (MRC & shot count) for 20nm CA/Vx

2. Criteria for trade-off between complexity of optimized mask, mask write time & lithographic performance (eg for contact holes CDU)

3. Using D2S's MB-MDP to "simplify" the complex OPC shapes as ebeam simulated target and verify its lithographic performance

4. Determine PVBand-shotcount-runtime trade-off for best lithographic performance

5. Work with maskhouse to compare the fracturing data-size and time between the conventional fracturing method for conventional shapes and MB-MDP's technique for complex (or SMO) shapes

8166-111, Poster Session

Shot-based mask optimization

A. D. Adamov, Stanford Robotics (United States)

We propose a pioneering approach in mask optimization that minimizes CD variability due to process variation(depth of focus, exposure latitude, mask error). The fundamental difference of our approach is selecting mask shots as basic element of optimization. On the most visual level, one can think of our method as simply iterating through all possible masks with the given number of shots, discounting ones violating mask rules and picking one that has the lowest CD variability.

Our method guarantees conformity to mask rules, minimization of the shot count and CD variability. We contrast it with other known methods, such as OPC (poor CD variability control), ILT (poor shot count control) and pixel based mask optimization (poor mask rule compliance).

We proceed to demonstrating results of our optimization on the standard cell patterns for 2X technology node. Using standard non-overlapping VSB shots,The improvement of 40-60% in CD variability (PV band) vs. OPC results is observed, while shot count increase is less than 20%. We also consider the non-standard and overlapping e-beam shapes showing that additional CD variability can be achieved while decreasing shot count.

Finally, we demonstrate scalability of the approach to the full chip. Our data demonstrates that economical cluster system can process 1cm2 size of the full chip within a day. Paths for up to an order of magnitude reduction in process time in both algorithmic and hardware improvements are outlined.

8166-151, Poster Session

Assessment and comparison of different approaches for mask write time reduction

T. Lin, E. Sahouria, S. F. Schulze, Mentor Graphics Corp. (United States)

The extension of 193nm exposure wavelength to smaller nodes continues the trend of increased data complexity and subsequently longer mask writing times. We review the data preparation steps post tapeout, how they influence shot count as the main driver for mask writing time and techniques to reduce that impact. The paper discusses the application of resolution enhancements and layout simplification techniques; the fracture step and optimization methods; mask writing and novel ideas for shot count reduction.

The paper will describe and compare the following techniques: generalization of shot definition (L-shot), multi-resolution writing and model based fracture techniques. The comparison of shot count reduction techniques will consider the impact of changes to the current state of the art using the following criteria: computational effort, CD control on the mask, mask rule compliance for manufacturing and inspection, software and hardware changes required to achieve the mask write time reduction; overall turn-around time. The paper will introduce the concepts and present data preparation results based on process correction and fracturing tools.

8166-113, Poster Session

Joint research on scatterometry and AFM wafer metrology

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The development of sophisticated dimensional metrology is essential to meet the metrology requirements for future technology nodes. CD-metrology in particular is identified by the ITRS as an essential challenge. For production measurements scatterometers and CD-SEMs are key metrology tools. Although measurement results of these different tools usually show a good correlation, systematic offsets are often observed. Universal product-related reference standards

for characterisation and calibration of scatterometers are currently unavailable.

Within the European Metrology Research Program [http://www.emrponline.eu] (EMRP) a joint research project (JRP) with 10 participants from European national metrology institutes, universities and companies is jointly supported by the European Commission and the participating countries within the European Association of National Metrology Institutes (EURAMET e.V.) [http://www.euramet.org]. The aim of this project is to overcome current challenges in optical scatterometry. This JRP will significantly improve and extend scatterometry methodically and regarding application areas. These extensions include the application of short wavelengths down to X-rays, a stringent exploitation of the polarisation degree of freedom, phase information of the scattered field and new detection schemes together with the development of improved or new concepts for modelling and data analysis.

For further refinement of the scatterometric algorithms, the impact of the structure form and local deviations must be taken into account. The necessary input on structure details will be provided by high resolution SEM and AFM methods, which have to be expanded to provide comparability to scatterometric measurements.

Finally a scatterometry reference standard will be designed, developed, characterised and calibrated to face the tough specifications demanded by the semiconductor industry for future technology nodes. As a first step towards a “golden reference standard” suitable for calibration of scatterometers this standard will be designed and developed to be suitable also for testing of AFMs and SEMs, so that the matching of these different tools will be possible.

Thus not only a comparability of these methods is introduced but also a mutual support of the partly redundant and partly supplementing information obtained by the different methods is provided. The sophisticated data analysis schemes will be developed in this JRP to reach levels of measurement uncertainty for different measurands significantly beyond the uncertainty levels reachable for each individual metrology method.

Additionally this project combines and extends the current scatterometry application fields towards surface roughness, periodically structured surfaces and diffractive optics, so that the synergy between metrology for semiconductor industry and for optics industry will be exploited.

8166-114, Poster Session

The mask CD control (CDC) using OCD applications

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As the pattern size of DRAM cell shrinks, requirements for Critical Dimension (CD) Uniformity control have become a critical issue. Mask CD Control (CDC) corrects CD level by scratching Photomask directly using Laser. Thus, this process is irreversible. It is important to measure CD distribution in wafer due to the accurate mask correction. In general, CD-SEMs have been used for CD corrections. But it takes long time to measure and includes many measurement issues such as focus issue, PR slimming, R&R (repeatability and reproducibility) problems to utilize the E-Beam sources. Therefore, it is difficult to figure out exact CD distribution in wafer.In this research, we prepared for two contact masks on 3X node condition and proceeded CDC by using CD-SEM data and OCD data to examine the effectiveness.The measurement time of OCD has reduced 40% more comparing to CD-SEM. In wafer the correction effect for CD-SEM has improved only 5% (before: 3.22nm-> after: 3.16nm), however, in the case of OCD, it has enhanced 71% (before: 3.9nm -> after: 1.14nm).

8166-115, Poster Session

Reticle CD uniformity on 2x-nm logic photomasks

A. Dayal, KLA-Tencor Corp. (United States); J. Richter, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); A. Pokrovskiy, G. Cong, A. Khemka, KLA-Tencor Corp. (United States)

Critical Dimension uniformity (CDU) is still one of the most critical parameters for the characterization of photomasks for the 2x nodes. Recent work has shown that the completely new approach of CD inspection, the process of gathering CDU data during reticle inspection, corresponds very well with established CD measurement techniques that use the CD-SEM, and offers a significant number of advantages over the CD-SEM methodology.

The CD inspection technique is now in an early stage to become a real alternative to classic CD SEM measurement methods. In this paper we will show a very generic approach towards CDU measurement that will work on any photomask, be it logic or memory. By using a feature template we are able to tune precisely which features will be analysed by CD inspection and which features will be excluded. This allows for completely new CD investigations and promises to provide an in-depth understanding of the mask process.

The template approach has several parameters that describe the desired CD size to be investigated, the proximity of the relevant structures and the length of the features. Thus the approach allows the user to are able to choose a very specific structure of interest for the CDU measurement. A design of experiment is done to thoroughly test the template approach and the results are used for detailed understanding of various parameters: the comparison of CD inspection and CD-SEM on the very same pattern, the number of available structures on 2x logic designs and the influence of optical proximity effects for CD signature evaluation.

Our experiments reveal not only an excellent correlation with the CD-SEM but also demonstrate clear advantages of CD inspection over the CD-SEM approach.

8166-116, Poster Session

The application of logic CD uniformity maps from a reticle inspection tool for wafer intra-field CD correction

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We have entered a phase where the mask Critical Dimension Uniformity (CDU) specification is fast approaching the limits of the capability of the current POR (process on record) process tools for 2X and 3X technology node reticles. Thus, the CDU specification is becoming an increasingly critical parameter for the characterization of reticles for the 3x and 2x technology nodes. Mask shops and Wafer Fabs have started exploring reticle inspection tool based CDU measurements as a means of improving the uniformity on reticles as well ultimately on wafers. Wafer Fabs are actively exploring applications for inspection-based CDU for scanner intrafield CD correction to improve parametric yields, as well as to monitor CD change over time. CDU inspection data provide the user with a rapid and very dense sample of CDU measurement points on a reticle. These data can be applied easily to a number of different applications.

In this paper we will present the method of operation and results of a CDU study using the KLA-Tencor Teron inspection tool, on multiple 28nm Logic reticles. We will present preliminary reticle CDU maps and

correlate the measurements with conventional reticle metrology results, as well as with wafer intra-field (IF) metrology results. We will also present a technique for applying a reticle CDU map for wafer intra-field CDU correction using Dose MapperTM (DOMA). Finally we will quantify the improvements in CDU on the wafer as a result of applying (feeding forward) the reticle CDU maps.

8166-118, Poster Session

In-die mask registration measurement with existing inspection tools

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The demand for aggressive image placement accuracy is being increasingly accelerated by DPT deployment. The ratio of residual errors caused outside of mask writing tool is increasing.

Advanced optical scanner is now having a capability to correct those errors. This technology requires in-die metrology function.

We have reported in-die CD and registration metrology capability of mask inspection equipment. However existing inspection machines, which are already in use, do not have such features as to perform this function as they are not not designed for such purpose.

We are developing a method to improve measurement accuracy by incorporating registration mark data obtained by conventional metrology tool, and will report the result of evaluation of this method.

8166-119, Poster Session

The influence and improvement of through pellicle image placement

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As technology move forward, the layer-to-layer overlay requirement becomes a serious challenge on wafer process. It also causes more difficult overlay control on mask process. Hence, the mask image placement has been required tighter and tighter.

Currently, most of mask houses measure image placement before pellicle mounting. However, foundries always exposes wafer by post pellicle mask to avoid particle falling on image plane to cause defect on wafer. The before pellicle mask image placement can't fully represent the real mask image placement during wafer process. Therefore, we need to evaluate the image influence of image placement on through pellicle mask.

Some testing was checked on our production masks. We find that the image placement is difference between post pellicle and before pellicle. It means that the registration had been changed after pellicle mounting. The result outstrips our suspect. Therefore, reducing the influence of image placement after pellicle mounting becomes more and more important. We found that the image placement of through pellicle should be impacted by three main factors. These three factors are pellicle frame, mask adhesive and mounting process. We cooperate with mask vendor to evaluate these factors and reveal the improvement result in this paper. Finally, the image placement difference between post pellicle and before pellicle is reduced to 3nm.

8166-120, Poster Session

Fabrication of 20-nm half-pitch quartz template by nano-imprinting

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Nano-Imprint Lithography (NIL) is one of the promising candidates for the next generation lithography in semiconductor process. We have studied the NIL template fabrication for the next generation technology of sub-20 nm line width fabrication, especially the duplication of quartz templates from a Si master. In general, it is considered that imprinting of narrow line patterns results in shortage of the height of the imprinted resist pattern because of insufficient resist filling. We investigated the fine pattern imprint technology focusing on resist filling and shape of the imprinted resist in the narrow pattern.

The pattern was fabricated on a Si wafer by a XY-stage Electron Beam (EB) writing and Reactive Ion Etching (RIE). The pattern on Si master was transferred to a quartz template by UV-NIL and RIE with a specially prepared UV-NIL resist.

Through the development of UV-NIL resist, we found that the formability of UV-NIL resist pattern depends on the monomer structures. In case of using the UV-NIL resist with poor formability (Resist A), the pattern height lowers when the line width narrows. On the other hand, in case of using the UV-NIL resist with good formability (Resist B), the pattern height does not lower. We investigated the representative physical properties of UV-NIL-resist related to fluid dynamics. But against our expectation, there is no considerable difference between the Resist A and the Resist B on the parameters. As a result, the formability of the resist pattern cannot be explained by fluid dynamics. We observed the micrographs of cross-sectional SEM of UV-NIL resist imprinted patterns. The Resist B had the good rectangular-shaped pattern. On the other hand, the Resist A had the round-shaped pattern and its height was low. In order to make clear the mechanisms of resist filling and formation of resist pattern, we observed the cross-sectional SEM images of the stack of the Si master and the UV-NIL resist before release. As a result, space patterns were filled with either the Resist B or the Resist A, and there seemed no difference about the filling to the Si master. We found that the shrinkage after Si master's release made the difference on the pattern formability. Therefore, to fabricate the quartz templates, we used the UV-NIL resist which has the best formability of resist pattern. As a result, we succeeded in fabrication of 20nm half pitch quartz line patterns with this duplication process. And, we demonstrated fabrication of 17.5nm half pitch UV-NIL resist line patterns.

8166-121, Poster Session

Releasing material screening and continuous nano-imprinting in mold replication for nano-imprint lithography

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Patterned media is one of promising technologies for HDD areal density growth. Groove size required for Discrete Track recording Media (DTM) is 17nm in 50nm track pitch in 2011, and bit size required for Bit Patterned recording Media (BPM) is 12.5nm in 25nm tack pitch in 2013, for 1Tbit/inch2 areal density on 2.5inch HDD media. That is feasibility demonstration target as the first generation of patterned media which all the media and the HDD makers are aiming at. Such extremely fine patterns need to be transferred to a wide and large area of a 2.5inch diameter media, also with an extremely high throughput of over 1000 media per hour for a large-scale production. Therefore, Nano-Imprint Lithography (NIL) and a mold (imprint mask) are essential. And, mold replication from an EB master is also a key for the production since EB writing takes so much long time then a high cost.

In nano-imprinting, since it is contact printing, there are some difficulties reported in general, such as huge void due to surface particles and/or UV resist pulling out (lift-off or plug), and mold sticking to replica wafers due to a rise in separation force with increasing pattern density. Particularly a higher separation force might cause damages to the master mold as well as to an imprinting tool, degradation in pattern quality possibly as well. Those difficulties also work to retard continuous imprinting for the mold replication. Then, we focused on a releasing material to facilitate clear and easy separation between cured resist (replica) and the mold.

The releasing material needs to have PFPE (Per-Fluoro-Poly-Ether)

main chain obviously. Then, we looked at terminal-group. We tried to characterize several candidates in contact angle for surface free energy, in force curve and friction curve by AFM for adhesion (release) and friction, in film thickness by XRR, and so on. Then, we found that a releasing material with hydroxyl terminal-group at one side in molecule showed the best performance in the characterization. We also found that the new releasing material we chosen showed a higher durability, i.e. less film loss, in continuous imprinting especially when a higher temperature baking applied after spin-coating.

We finally carried out continuous nano-imprinting for the mold replication to see a real performance of the new releasing material, in a comparison with the other PFPE releasing materials, by using an EB master mold full surface patterned on a 2.5inch diameter. And, we successfully demonstrated over 100 continuous replica imprinting with no mold cleaning and/or change at all. Particularly, we found that the new releasing material we selected prevented particle transferring from the replica wafer to the master mold. Repeatable imprinting defect did never happened with the new releasing material, while the others did. Finally multiple mold fabrication, 1 master to 1 sub-master, 1 sub-master to 100 of 2nd sub-master, then 100 of working replica for media imprints, was successfully carried out.

This paper describes a novel releasing material we chosen, and continuous nano-imprinting feasibility study result with it for 10,000 (1x1x100x100) of working replica mold fabrication from an EB master for the patterned media application.

8166-122, Poster Session

Layout decomposition and mask synthesis for double and triple exposure with image reversal in a single photoresist layer

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Double Patterning (DP) is the most promising lithography solution for 22 nm technology node and beyond. It can both increase the pitch density and print intricate 2D patterns reliably, far beyond the capabilities of the conventional Double Exposure (DE) methods. The key idea is to break up the desired layout into two masks such that sub-resolution configurations are separated between the masks into simpler, printable patterns. Recently, a double exposure method in a single photoresist (PR) layer using image reversal DESIR [1] has been proposed which matches the printing capabilities of the DP technology while using only one PR layer instead of two and a hard mask - affording thus a significant process simplification. While conceptually straightforward, layout decomposition, in general, poses a major obstacle in terms of layout complexity, layout verification overhead, and decomposability related design issues. Here, for the first time, a layout decomposition and mask synthesis for the DESIR approach that can be easily implemented in any mask design tool is proposed. The method is distinctly different from extant layout decomposition techniques because of the intricate PR properties subjected to several exposures and the critical image reversal baking step. The challenge in the layout decomposition and mask synthesis for DESIR is that many combinations of mask 1 and mask 2 layouts lead to the same desired overlay pattern. At the same time, the challenge constitutes a welcome benefit and it is exploited by the proposed method to provide the optimum combination of masks given the specific strengths and weaknesses of the lithography in use. First, the desired pattern is broken down into blocks. The image reversal resist properties are such that only areas/blocks exposed the 2nd time after the reversal bake are soluble when developed. For blocks that are insoluble, multiple mask combinations are available, the areas of interest in: mask 1 and mask 2 opaque (PR never exposed), mask 1 and mask 2 transparent (PR exposed twice), mask 1 transparent and mask 2 opaque (exposed 1st time only). Next, the combination of mask layer 1 and mask layer 2 that generate undesired final patterns are eliminated using a logic operation: where A and B are the mask layers 1 & 2 respectively. Next, the mask layout combination which results in optimum pattern printability is selected by using an internal corner counting algorithm. A corner is counted with a reference to each block when two adjacent blocks have the same value (opaque/transparent) and are opposite to the value of the referenced block. A product is formed by multiplying the number of corners of layer layout 1 and 2. Using the following Figure of Merit FoM= min[(corners from mask 1 + 1) * (corners from mask 2 + 1)], the optimum combination of mask 1 and mask 2 is the one with smallest value of FoM. Finally, from the remaining choices of the determined minimum (FoM), the layer layout with the largest area of blocks forming a contiguous rectangular or square shape is selected.

[1] C. Ndoye, M. Orlowski, SPIE Advanced lithography Conference San Jose, 7970-52 (2011)

8166-123, Poster Session

Hotspot detection for indecomposable self-aligned double patterning layout

H. Zhang, Y. Du, M. D. F. Wong, Univ. of Illinois at Urbana-Champaign (United States); R. O. Topaloglu, GLOBALFOUNDRIES Inc. (United States)

Self-aligned double patterning (SADP) lithography is a novel lithography technology that has the intrinsic capability to reduce the overlay in the double patterning lithography (DPL). Although SADP is the critical technology to solve the lithography difficulties in sub-32nm 2D design, the full SADP decomposition flow - the key factor for mask preparation - is not yet mature. Besides the quality requirement of the decomposed core and trim mask, one big challenge in this process is the hot spot detection to help SADP friendly layout design. An efficient hot spot detection algorithm is necessary not only for the decomposability check but also to provide important information to help designer improve the layout. It can also be used to bridge the gap between the mask rule and design rule, which exists in current SADP design and process.

This paper targets on the hot spot detection based on our state-of-the-art decomposition algorithm. In our previous work, the layout is first processed with an ILP based decomposition algorithm. With the solution of the decomposition process, we can have an initial decomposition result and further polish it with better manufacturability and less complexity. If layout is indecomposable, we should find the hotspot to where the violation is, which is already solved in our previous paper.

However, the problem comes from the situation that for a certain hotspot, it usually can be categorized into different feature-violation, which demands different fixing requirement. To targeting on this issue, we will need to find a novel method to help designer modify their design with minimum/reasonable modification. Since the decomposition result is not obvious, this decomposition hotspot detection with fixing suggestion has significant necessity.

The basic process is described as follows. For any pre-decomposition layout, the first step is to check its decomposability. If it is indecomposable, the slack insertion algorithm will locate the violation first, then characterize the violation and classify it into different types, such as space violation, pattern violation, and width violation. We can further analyze this information by a combinational algorithm to detect the hot spot with minimum modification requirement. This work would be efficient for a decent DRC process and show its significance for the SADP friendly design.

8166-124, Poster Session

Layout decomposition and mask preparation for pitch quartering process

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Since the EUV technology is still lagging behind, which has been recently reported unavailable before 2014, there is a huge gap between the design and lithography capability that needs to be solved for the following 3 years and probably for the 14nm or 10nm technology nodes. We need find solutions for the upcoming challenges that the single exposure does not capability to conquer. One alternative way other than EUV is the pitch quartering process, which is a further extension from the self-aligned double patterning (SADP).

In the pitch quartering process, similar to the SADP process, the critical features are all automatically aligned to the feature from one single exposure, indirectly. Thus the process can largely avoid overlay. There are two sidewall generating processes, which we name them sidewall 1 and sidewall 2. In the first sidewall generating process, sidewall 1 is deposited aligned to the cores on the wafer. Once cores are removed, we can further deposit sidewall 2 aligned to sidewall 2. After the sidewall 1 is finally removed as well, sidewall 2 will define the final critical features. After so called trim/block mask is applied, we can generate the final 2D pattern as designed.

In this paper, similar to the 2D layout decomposition problem for SADP process, the algorithm for layout decomposition and mask preparation for core and trim/block will be introduced, which needs input of layout and design rules. We further extend the existing SADP decomposition algorithm [1] for pitch quartering process. In the process, we first pixelize the layout and insert variables on each tile. By applying the two types of sidewall adjacency rules for both sidewall 1-core and sidewall 1-sidewall 2 self-aligned relationships, we can reconstruct the process using ILP or SAT formulation. We can adopt the similar process to solve the decomposition for pitch quartering process.

The difference mainly comes from the variation control process. As the critical dimensions in pitch quartering process have different correlations, such as S1-S3 and S2-S4, and different CD variation on different line width and space, a careful decomposition with optimal process variation mitigation is needed. We need not only to consider the variations on overlay, but also to deal with the large variations and correlations between different line width and space. Novel criteria and combinational algorithm is needed based on the basic circuit analysis. Design features will be characterized by two criteria - noncritical/critical, and matched/nonmatched. For the critical features in the circuit, we will need to assign them on the less varying position and vice versa. For the circuit, where matching is important, the matched and correlation will also be taken into consideration. Finally, a practical solution and extension will be shown based on the previous combinational algorithm, and the optimality on the variation control will also be provided. This would be the first ever published decomposition algorithm for pitch quartering process.

Reference

[1] Hongbo Zhang, Yuelin Du, Martin D. F. Wong, Rasit Topaloglu. “Self-Aligned Double Patterning Decomposition for Overlay Minimization and Hot Spot Detection”. DAC 2011. (Accepted, to appear.)

8166-125, Poster Session

Determination of CD variance factors of 28-nm 1x-metal layer hot spots using experimental and simulated CD contours

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The 28nm technology node is very challenging for the production of large chips with very aggressive design rules. For the 1x metal layers especially it has been observed that some layout configurations known as hot spots have very limited lithographic process window. Such hot spots detected by litho simulations or flagged as yield detractors are not easy to characterize due to their asymmetric and two-dimensional nature. Almost all of them appear to be either pinching or bridging configurations leading to voids, leakages or shorts. In addition to their intrinsic complex geometry they are very sensitive to any variation of experimental parameters like dose, focus, mask error, lens aberrations, resist... As a consequence the transition from good patterning to failing one lies in a continuum and thus is very difficult to identify. On top of that the measurement noise and variability are important for two-dimensional patterns.

The first purpose of this study is to present an original methodology to characterize these hot spots after lithography with good statistics. The principle is to use many SEM pictures taken by combining many measurements of the same feature sharing the same experimental conditions. Afterwards the pictures are aligned and stacked to improve the signal-to-noise ratio and to average uncontrolled source of CD variation. With such high quality images it is then possible to extract contours of high accuracy giving much more information that single point measurements.

The second scope of this work is to take advantage of the extracted contours to identify some of the main contributors to CD variations and try to characterize them separately. The design of our experiments allows us to have repetition of hot spots clips along the scanner slit and in the field. Additionally for each site we get various mask sizings to evaluate the MEEF. To assess further the impact of mask error we gathered SEM pictures of the mask itself. Varying or not the focus dose conditions across wafer give us the latitude to study precisely the behavior of the hot spots through process window and also to perform a detailed analysis of the CD uniformity detractors (intra- or interfield location, mask error). Later the SEM contours are compared to simulated ones not only to estimate the model prediction capability but also to help calibrating Optical Rule Check limits.

Finally we propose to investigate with more details the criticality of some hot spots by analyzing the way the lithographic patterning is transferred after the different etch steps.

8166-126, Poster Session

Yield optimization through MLR techniques

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Some chip manufacturing steps lead to non-negligible process variation at wafer level. Typically, chemo-mechanical planarization, known as CMP, is a non-homogeneous process and thickness variations can be measured depending on the distance of the die from the wafer center. These variations have an impact on chip performance and thus on the final yield. This effect may be amplified by the fact that thickness variations on processed wafers introduce focus issues during later photo-lithography steps.

Original chip layouts are modified by inserting dummies to correct thickness variation issues due to CMP, but these correction are based on models only depending on average values.

In this paper, we propose a methodology to replace a single instance of the field written on the mask by multiple instances of this field as commonly used for Multi Layer Reticles. In the described methodology, each field of a same mask does not consist in different layers of the same chip, but of an optimized image of the same layer of the chip. The layout optimizations performed on the chip take into account, not only the average parameters of the process, but also an additional parameter, which is the distance of the die from the wafer center. This optimization can be applied either for the dummy insertion procedure or for optical proximity corrections.

In the first case, the goal is to lower thickness variations across the wafer. In the second case, the goal is to take into account existing thickness variations in the OPC model. In both cases, variants of the original layout will be built and placed on the same mask as different fields.

In this paper, we will analyze the thickness variations measured on wafers with standard processes and their impact on the yield. We will propose a die placement driven methodology to adjust the models used for both dummy insertion and OPC. A detailed analysis of the final cost will be presented. This cost depends on one hand on the extra cost of chip manufacturing and on the other hand on the benefits brought by yield improvement. The extra cost of chip manufacturing is due to the smaller fields used as done for Multi Layer Reticles. This detailed cost analysis reveals whether, depending on expected variations, a two-field or a four-field reticle should be chosen. Finally, a procedure to automatically generate the step plan to shoot each optimized field on the wafer will be described.

Thanks to the combination of classical mask techniques: MLR, model based CMP and model based OPC, we propose an original methodology to improve wafer processing yield that do not need any specific equipment and at a restricted extra cost.

8166-127, Poster Session

Can fast rule-based assist feature generation in random-logic contact layout provide sufficient process window?

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A two-step full-chip simulation method for optimization of sub-resolution assist feature placement in a random logic Contact layer using ArF immersion Lithography is presented. Process window, characterized by depth of focus, of square or rectangular target features is subject to optimization using the optical and resist effects described by calibrated models (Calibre nmOPC, nmSRAF simulation platform). By variation of the assist feature dimension and their distance to main feature in a test pattern, a set of comprehensive rules is derived which is applied to generate raw assist features in a random logic layout. Concurrently with the generation of the OPC shapes for the main features, the raw assist feature become modified to maximize process window and to ensure non-printability of the assist features. In this paper, the selection of a test pattern, the generation of a set of “golden” rules of the raw assist feature generation and their implementation as well as the assist feature coverage in a random logic layout is presented and discussed with respect to performance.

8166-128, Poster Session

Dynamic feedback controller for optical proximity correction

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A dynamic based feedback controller for Optical Proximity Correction (OPC) in a random logic layout using Arf immersion Lithography is presented. The OPC convergence, characterized by edge placement error (EPE) is subjected to optimization using optical and resist effects described by calibrated models (Calibre nmOPC simulation platform). By memorizing the EPE and Displacement of each fragment from the preceding OPC iteration, a dynamic feedback controller scheme is implemented to achieve OPC convergence in a lesser number of iterations. The OPC feedback factor is calculated for each individual fragment taking care of the cross-MEEF effects. Due to the very limited additional computational effort and memory consumption, the dynamic feedback controller is reducing the overall run time of the OPC compared to a conventional constant feedback factor scheme. In this paper, the dynamic feedback factor algorithm and its implementation as well as testing results for various full chip random logic layouts are compared and discussed with respect to OPC convergence, consistency and performance.

8166-129, Poster Session

Anticipation of dimensional issues caused by topography during photolithography

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The nominal thickness for a material to be used for photolithography in given process conditions, is typically monitored on test wafers with a completely flat surface. Therefore material’s specification is often limited to thickness uniformity, reflectance, refractive indexes and chemical properties. Our study indicates that topography plays a major role in coating and lithography performance.

NVM embedded IC’s integrating a variety of devices within the same chip may lead to challenging topography at gate level. Tight control of transistors CD, coherent with model based OPC treatments precision, is hard to achieve in circuitry regions with small surface before etch and high poly-silicon step. The proposed model is based on reflectance increase in areas where observed CD is small with respect to the target. The observed root cause on such components is linked with materials’behavior -thickness gradient- in the proximity of edges of poly-silicon blocks and with the overall thickness reduction when the blocks are smaller than a given dimension.

A set of test patterns is defined and substrates are prepared with planarizing and conformal BARC’s in order to quantify the influence of topography on gate CD’s. The geometries provide a good sampling in terms of pre-etch surface. After some lithography steps, the dimensional effects are quantified by top view SEM. A model describing materials thinning can be computed from CD behavior data in the case of the inorganic BARC.

The study shows the limitations of both types of BARC’s and suggests that Optical Proximity Correction could be used to compensate the effects of topography on transistors final CD. Some recommendations are made in order to fulfill 65nm and smaller technology nodes’ requirements. Several components of the study can be combined to master topography effects in complex process flows.

8166-130, Poster Session

Fast DoF awareness inverse SRAFs generation by using interference guidance map

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As Moore’s law marches on and semiconductor manufacturers make the push towards the 22nm technology node and beyond, the challenges faced by microlithography are ever increasing. The need to print such small features using 193nm illumination -- which is way beyond the Rayleigh diffraction limit -- has made resolution enhancement techniques (RETs) mandatory.

Depth of focus (DoF) which is relative to working range for exposing patterns become the most critical parameter in such critical optical lithography node. Optical Proximity Correction (OPC) incorporating sub-resolution assist features (SRAFs) is the most-widely-used RET for pattern fidelity enhancement and DoF improvement, and has been a standard industry practice since the 90nm node. Nevertheless, as the reachable solution space lies strictly in the vicinity of the original layout for OPC and the rules limit SRAF placements, OPC with SRAFs is often not expressive enough and does not exploit the full range of possible mask configurations to get the best possible pattern fidelity and DoF.

To overcome this limitation in advanced CMOS processes, inverse lithography (IL) are proposed to promise better patterning fidelity and DoF than conventional mask correction techniques due to the nature of reverse mask optimization. Several promising research works are widely studied recently including optimization algorithm, cost function behavior and hardware verification. However the IL computations are always time consuming. Especially, to optimize the DoF, not noly nominal optical models are required but also the defocus models. Therefore at least double time will elapsed as both nominal and defocus model join the IL calculation. Hence development of the efficient IL algorithms that concern both accuracy and speed for DoF joining inverse optimization should be demanded immediate attention and far studied.

In this paper, we do the mask correction by using a general steepest descent algorithm in nominal condition. After obtaining the promising IL patterns, the defocus model is incorporated to generate a DoF awareness interference guidance map. According to this map, the intensity distributions of variation impacts to cost function of all mask pixels are overall explored. Then we quickly allocate the accurate model-based SRAFs including size, position and orientation by referring the interference guidance map without other complicated calculations.

8166-131, Poster Session

Iterative source mask optimization incorporating Abbe's method and Hopkins' approach

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Lithography technique is the cornerstone of the semiconductor industry. With advances in microlithography now pushing towards 20 nm and beyond, the engineering of how to print circuit layouts on wafers has become more intricate and complicated. Resolution enhancement techniques (RETs) are demanded to improve lithography performance including pattern fidelity, process window (PW), edge-placement error (EPE) and image contrast.

Mask and source correction are the most widely used RETs due to the cost and hardware flexibility. Optical proximity correction (OPC) and off-axis illumination (OAI) are the first mask and source correction technique in early age. OPC that is a segment-based correction technique has been the general industry approach and has proven successful through many CMOS generations. Because it only modifies existing edges in the layout, segment-based OPC has the advantage of being easy to implement, particularly in iterative algorithms. In like manner, OAI applies the easy building source shape such as annular, dipole, C-quad and quasar, to enhance the resolution and contrast via constructing and destroying interference of optical wave.

However, as the Critical Dimension (CD) becomes ever smaller, this edge-only compensation technique is not expressive enough to exploit the full range of possible mask corrections. For example, sub-resolution assist features (SRAFs) which are placed in the ambient region of main patterns to assist exposure and not developed, can not generate via OPC. Therefore the pixel-based inverse mask design, or named inverse lithography (IL) that optimizes the cost function, has been proposed as an alternative due to its more relaxed constraints and full-mask approach. Indeed IL provides lots of promising solutions for inverse mask correction due to the full mask space calculation. Hence SRAFs can be automatically generated when IL calculation, which OPC is not competent.

Nevertheless, the shrinking CD and highly dense configures of drawn mask, ex : Dynamically Random Access Memory (DRAM), limit the correction space of IL. Moreover the IL generating SRAFs change the topology of mask that also leads the optimal source changing. The IL incorporating source optimization (SO) or generally called Source Mask Optimization (SMO) is recently widely studied. Actually the SMO can be seen as another inverse technique for resolution enhancement like IL. All algorithms used in IL can be applied to SMO and have similar thorny issues. The local minimum, slow convergence and other issues in IL still exist. So far SMO still need more developments and studies to become a conventional RET.

In this paper, we propose an iterative SMO algorithm which iteratively applies Abbe's method and Kopkins' approach to source optimization (SO) and mask optimization (MO). Due to the different image formation mechanisms of source and mask, SO and MO are suitable for different optimization algorithms where SO is belonging to linear programming and MO is non-linear programming. Theoretically, SO and MO can be iteratively performed until aerial image attain to the required quality. Moreover, because SO and MO are different parts, the IL optimization algorithm can be various choices where the conjugate direction descent algorithm is for SO and the steepest descent is for MO in our calculation.

8166-132, Poster Session

Total source mask optimization: high-capacity, resist modeling, and production-ready mask solution

M. Fakhry, Y. Granik, K. Adam, Mentor Graphics Corp. (United States); K. Lai, IBM Corp. (United States)

As the demand for taking Source Mask Optimization (SMO) technology to the full-chip level is increasing, the development of a flow that overcomes the limitations which hinder this technology's moving forward to the production level is a priority for Litho-Engineers.

The aim of this work is to discuss advantages of using a comprehensive novel SMO flow that outperforms conventional techniques in areas of high capacity simulations, resist modeling and the production of a final manufacturable mask.

We show results that indicate the importance of adding large number of patterns to the SMO exploration space, as well as taking into account resist effects during the optimization process and how this flow incorporates the final mask as a production solution.

The high capacity of this flow increases the number of patterns and their area by a factor of 10 compared to other SMO techniques. The average process variability band is improved up to 30% compared to the traditional lithography flows.

8166-133, Poster Session

A validation of source mask optimization for logic device through experiments

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As the manufacturability of chip design size continuously shrink in the low-k1 regime, Source and Mask co-Optimization (SMO) plays an increasingly important role in advanced Resolution Enhancement Technology (RET)s. Compare to other alternatives, it is already shown that the simultaneous co-optimization of both source and mask gives significant process window improvement over the conventional iterative optimization method. Also recently SMO become a cost-effective counterproposal of double patterning technique, as an enabling technology for low-k1 design node. It is clear that intensive optimization of the fundamental degrees of freedom in the optical system allows the creation of non-intuitive solutions both in the source and the mask, leading to improved lithographic performance.

In this work, we study the Process Window Analysis (PWA) for multiple critical layers in 2X nm node logic device SRAM cells. We studied three layers (one clear-field, and two dark-fields) with two different cell sizes for a total of 6 different cases to compare the results of the baseline source and the mask with the parametric Diffractive Optical Element (DOE) and freeform source. The optimization method is to minimize Edge Placement Error (EPE) through process conditions (focus, dose and mask error) as the cost function. We compare the process window and Mask Error Factor (MEF) for all cases. In this early development stage, there was no resist model available. We therefore also studied the impact of applying a simple aerial image blur on the optimization performance.

The theoretical results clearly show that the optimized Freeform source and parametric DOE solutions produce significant (52% improvement in DoF@0%EL and 33% improvement in MEF for one of the clear-field layer case - values are from Freeform source results) improvement over the baseline case. Since mask manufacturing rules (MRC) are considered as part of the optimization, the resulting masks show good mask fidelity for all patterns. Based on the simulation results, the improvements will be validated "on wafer" using ASML's FlexRay feature to define the freeform source. The results will be investigated to verify the performance advantage of SMO.

8166-134, Poster Session

Performance and variability driven guidelines for BEOL layout decomposition with LELE double patterning

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Litho-etch-litho-etch (LELE) double patterning lithography (DPL) is a strong candidate for BEOL patterning at the 20nm logic half-node (sub-80nm pitch). In LELE, layout patterns are decomposed into two masks (colors) such that all polygons satisfy a minimum coloring spacing requirement. When there is a coloring conflict during decomposition, a polygon (net) can be split into two different-color segments to resolve the spacing requirement, introducing a stitch where the two segments are overlapped to avoid a disconnection from overlay and/or line-end tapering. Each split segment has different parasitic resistance and capacitance (RC), and a stitch also affects total (RC) values of the net, depending on its color, geometrical dimensions, overlay, stitching location and length, etc.

In this work, we propose guidelines on stitching insertion to minimize circuit timing variation (induced from best-case to worst-case RC parasitic). In our experimental setup, we perturb geometrical dimensions of test layout patterns to emulate overlay error and bimodal CD distributions. After that, we extract interconnect resistance and capacitance of the patterns for circuit level simulation. We use FO1 inverter chains with the extracted interconnect RC network as test circuits. Finally, we measure delays of the circuit with various stitching locations and lengths using SPICE simulation. We use 45nm technology parameters obtained from a commercial library in our experiments, and scale to future nodes according to ITRS projections.

(1) Our experimental results show that stitching length is not a significant variation source. This can be explained by the fact that interconnect at advanced technology has high aspect ratio and thick inter-layer dielectric. Therefore, width variation, and thus ground capacitance variation induced by overlap length, is not significant compared to spacing variation between interconnects. This implies a design guideline for routing and mask decomposition.

(2) Further experimental results show that delay varies by 4% when stitching location sweeps from driver side to receiver side along an interconnect. Delay variations are higher at both driver and receiver sides but lower at the middle. This is because the split segments have different colors and their RC values deviate in opposite direction under lithography variations. Due to the averaging effect across the segments, the delay deviations compensate each other and reduce overall variation on the interconnect. This implies a design guideline for timing critical routes in dense patterns should preferentially receive stitches to reduce delay variation in the regime of combined CD bimodality and overlay error.

(3) We also report experiments and design guidelines related to stitching of neighbor wires of a given timing critical route.

8166-135, Poster Session

Integrated advanced hotspot analysis techniques in the post-OPC verification flow

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Improvements in compact lithography models have allowed EDA suppliers to keep up with the requirements for each new technology node. Compact lithography models are derived from the Hopkins method to calculate the image at the wafer. They consist of the pre-calculated optical kernel set that includes properties of projection and source optics as well as resist effects. The image at the wafer is formed by the convolution of optical kernel set with the mask transmission. The compact model is used for optical proximity correction (OPC) and lithography rule checking (LRC) due to their excellent turnaround time in full chip applications. Leading edge technology nodes, however, are inherently more sensitive to process variation and typically contain more low contrast areas, sometimes resulting in marginal hotspots. In these localized areas, it is desirable to have access to more predictive first principle lithography simulation. The Abbe method based lithography simulation includes full 3D resist models that accurately solve from first principles the reaction/diffusion equation of the post exposure bake. These rigorous models have the ability to provide added insight into 3D developed profile in resist at the wafer level to assist in disposition of hotspots found by LRC using compact models. This paper will explore the benefits of a tightly integrated rigorous lithography simulation during the post OPC flow at the LRC hotspot application step. Multiple user flows will be addressed along with methods for automating the flows to maximize the imaging predictability where needed while keeping the impact to turn around time to a minimum.

8166-136, Poster Session

Double patterning for a 56-nm pitch metal layer test design using inverse lithography

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Lucas, et. al(1) have published a metal layer pattern that is suitable for testing double patterning approaches. While this pattern can be imaged with single layer 193 nm immersion lithography at 112 nm pitch, it requires decomposition into two layers to be patterned at 56 nm pitch. Initial results, using the layers described by Lucas, resulted in a problem area that was resolved by splitting an additional rectangle between the two layers. Adjusting the split layer overlaps improved lithography relative to the initial result, although the depth of focus (dof) was only 30 nm with a 5% exposure latitude (el) for brightfield exposure, too small to be practical for manufacturing.(2) Biasing the pattern and simulating “etchback” increased the dof once a problem area was resolved by increasing a line end offset. With these improvements dof was increased to 40 nm with a 12.5% el. Darkfield simulation of this pattern increased the depth of focus to 60 nm with a 7.5% exposure latitude. The line end offset increased the overall pattern area by only 1.6%.

In the limits of this approach, the pattern could be imaged at 40 nm pitch with a 30 nm depth of focus and 5% exposure latitude.

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8166-137, Poster Session

Using custom features to check OPC model performance

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Model Based Optical Proximity Correction (MB- OPC) is essential for the production of advanced Integrated Circuits (ICs). As the speed and functionality requirements of ICs production always require reducing the Critical Dimension (CD), the demand is continuously increasing for more accurate and representative OPC models.

The current known best practice is to calibrate OPC models with measured test patterns. Test patterns are selected to represent the final designs to be printed in any specific technology that will use the OPC solution. The accuracy of the OPC models is critical to obtain the right product pattern dimension and consequently to the success of the IC production process. During the model calibration process, the modeling engineer usually builds several different OPC model candidates and then based on some verification metrics selects the

best OPC model from these candidates to be the final OPC model representing the lithographic process.

In this paper we are proposing an additional technique for judging the accuracy of the OPC model. The technique is to intentionally add custom features that when placed with certain configuration on the test mask, during the model build stage, have marginal printability, i.e. may print or not and based on the wafer image the OPC model prediction maybe tested to verify the accuracy of the OPC model. We have tested the technique and we are going to include some sample results in the paper.

The study is important to the modeling engineers as well as to the OPC algorithm builder as it gives better assessment to the accuracy and limitation of the OPC model.

8166-139, Poster Session

A new method to optimize CD uniformity for photomask in the HP 3x node

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As the pattern feature sizes on the memory devices move toward smaller, the requirement for the CD uniformity has becomes a critical issue. Photomask CD error sources come from an electron beam writer, developing and etching process. And these sources are consisting of a symmetric (fogging, etch loading effect) and a non-symmetric (nozzle scan direction, plasma uniformity and etc.) uniformity. Even if non-symmetric sources are tuned well by a recipe or a hardware modification, small portion still remains. Generally, the correction method is feed-back process from the result including both sources. In the both errors, the symmetric error component has studied well and it is modeled by a Gaussian function as a pattern density, but the non-symmetric error is not well defined as a related thing.

In this study, we analyze CD uniformity by separating a symmetric and a non-symmetric component. Especially, we focus on the behavior of a non-symmetric uniformity as a pattern density and a field size for the memory devices. It is found out that there is a rule of a non-symmetric uniformity, and this rule is adopted to correct the CD uniformity using the dose modulation of electron beam writer. The CD uniformity of the memory devices is effectively reduced using this modulation.

8166-140, Poster Session

Development status of EUVL mask blank and substrate

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Asahi Glass has been developing of the EUVL (extreme ultra violet lithography) mask blank and polished substrate since 2003, including the developments of all essential materials and processes: the low thermal expansion material (LTEM), the material developments of the reflective, capping and absorber films, the process developments of the substrate polishing, the cleaning, the film deposition and the resist film coating processes. In this paper, we present the current development status of the full-stack EUV mask blank and polished substrate which are the most suitable for the EUV lithography process development with EUV pre-production exposure tools. We are going to report the development progress of the reflective multilayer-coated LTEM substrate by showing the critical performances with those of 2010 achievements, which include the substrate flatness, the EUV optical properties of the Mo/Si reflective layers and the defect of LTEM substrate and reflective layer. The performances of the Ta-based absorber and the resist films will be explained as well to show the readiness of the EUV mask blank suitable for any kinds of process developments of the EUV lithography.

8166-142, Poster Session

Attenuated phase-shift mask with high tolerance for 193-nm radiation damage

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In the semiconductor technology, radiation damage on photomask is caused by using the 193nm ArF excimer laser and advancement in the exposure tool. This phenomenon is regarded as serious issue for semiconductor device fabrication. Some approaches have been tried to prevent the radiation damage. One of reports indicates that the radiation damage can be reduced by using an exposure tool with ultra extreme dry air. However, it is difficult to adopt dry air into all exposure tools due to high cost. In our previous work, we ascertained two facts; radiation damage is caused by MoSi film oxidation, and depends on MoSi film composition.

In this work, we optimized MoSi film composition for att. PSM in consideration of repair processability, cleaning durability, and mask defect. By this new att. PSM, we confirmed that the radiation damage can be suppressed. And we also investigated CD and lithography performance of new att. PSM and compared with conventional att. PSM. We developed new att. PSM that has high tolerance for radiation damage.

8166-143, Poster Session

The trade-offs between thin and thick absorbers for EUV photomasks

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Changes in the EUV mask absorber film affects both imaging and mask making. These changes will be investigated through experiment and simulation. Fundamentally, thinning the absorber generally increases the intensity of light reflected from the absorber while changing its phase. Simultaneously, there is a decrease in the influence of feature edge topography.

Each of these effects has multiple ramifications. If the absorber induces a 180° phase shift, an increase in reflected intensity will cause the mask to behave more like an attenuated phase shift mask. Thus, a slight increase in the image slope at a feature edge for certain features can become an advantage. On the other hand, a larger reflected intensity can increase sensitivity to thickness variations on the mask, causing changes to both the amplitude and phase of reflected light. A typical thickness variation of 2nm range is observed in a photomasks produced today. The potential impact of this variation will be analyzed. Additionally, increased reflected intensity increases the required flare correction and the degree to which edge die are affected. Various mitigation and correction strategies that are being developed to address this issue will be considered.

The decrease in feature edge topography also has multiple consequences. First, due to electromagnetic effects, slightly more light will propagate through an identically sized opening on the mask. It can be shown that, for a constant mask CD, a thinner mask can result in lower MEEF. However, this is simply a by-product of this effect and the MEEF change can be rectified with a simple mask bias. Second, the required shadow correction will be smaller for a thin absorber. These corrections are necessary for any practical mask thickness and EDA vendors are making good progress on various model based shadowing correction strategies.

The decision to deploy a thinner absorber depends on which imaging effect has a smaller impact after practical mitigation and correction strategies are used. Any imaging advantage gained with the thinner absorber must be balanced against the primary mask-making consequence: the need for an opaque border. The additional mask processing associated with any opaque border solution will add

complexity, and potential defects, to the mask process. These options will also be reviewed in sufficient detail to weigh against the imaging trade-offs.

8166-144, Poster Session

A study of closed-loop application: WLCD-CDC for 32nm and beyond reticles

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Optical lithography stays at 193nm with a numerical aperture of 1.35 for several more years before moving to EUV lithography. Utilization of 193nm lithography for 32nm and beyond forces the mask maker to produce complex mask designs and tighter lithography specifications which in turn make process control more important than ever. High yield with regards to chip production requires accurate process control.

Critical Dimension Uniformity (CDU) is one of the key parameters necessary to assure good performance and reliable functionality of any integrated circuit. There are different contributors which impact the total wafer CDU: mask CD uniformity, resist process, scanner and lens fingerprint, wafer topography, etc.

In this study the newly developed wafer level CD metrology tool WLCD32 of Carl Zeiss SMS is utilized for CDU measurements in conjunction with the CDC200 tool from Carl Zeiss SMS which provides CD uniformity correction. The WLCD32 measures CD based on proven aerial imaging technology. The CDC200 utilizes an ultrafast femto-second laser to write intra-volume shading elements (Shade-In Elements) inside the bulk material of the mask. By adjusting the density of the shading elements, the light transmission through the mask is locally changed in a manner that improves wafer CDU when the corrected mask is printed.

The objective of this study is to evaluate the usage of these two tools in a closed loop process to optimize CDU of the mask before leaving the mask shop and to ensure improved intra-field CDU at wafer level. Main focus of the study is to investigate the correlation of applied attenuation by CDC and the resulting CD change, the impact of CDC process on CD linearity behavior and the correlation of WLCD32 data and wafer data. Logic and SRAM cells with features having designed line CD's at wafer level, ranging from 27nm to 42nm have been used for the study. The investigation provides evidence that the applied attenuation by CDC200 shows a linear correlation to CD change at wafer level measured with WLCD32. Additionally, WLCD data shows that the CDC application does not impact the CD linearity for the tested feature range. The WLCD32 measurement data in turn show an excellent correlation to wafer print CD data indicating cost effective use case of closed loop WLCD/CDC application.

8166-145, Poster Session

Dry etching technologies for the advanced binary film

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We have developed a highly integrated methodology for patterning on Advanced Binary Film (ABF) photomask, which was developed and manufactured by HOYA for leading edge photomasks, using Shibaura Mechatronics ARESTM mask etch system and its optimized etch process.

ABF photomask is promising the best optical lithography performance beyond the 32nm half-pitch generation because of its advantages of relatively low thickness of blanks films and being chemical durability in mask cleaning process which leads to reducing overall mask cost.

It requires a quite new patterning technique for the thinner opaque layers which are completely different materials compared with the conventional phase shift mask (PSM) using dry etch process. The dry etch process, however, has generally faced technical challenges such as the difficulties in CD control, etch damage to quartz substrate and low selectivity to the mask resist.

In this study, the TaOx and TaNy layers were etched in ARESTM mask etch system with our optimized plasma produced by certain source power and bias power. The etch rates for those layers and mask resist were calculated by measuring etched step. The characterization of etch profiles and CD shift is performed by cross sectional SEM views with the line and space patterns consisting of various feature size.

As a result, ARES and its optimized etch process have demonstrated the maximal CD performance such as CD uniformity and CD linearity at patterning of ABF photomask without any etch damage to quartz substrate. In particular, our gas chemistries chosen at this work has a capabilities of adjusting CD shift from negative to positive or even zero shift by controlling sidewall protection film. And it has an advantage of high selectivity to mask resist, which realizes thinner mask resist process.

Present status of the development and evaluation results of the system will be shown on our poster session.

8166-146, Poster Session

Impact of mask corner rounding on wafer printing

C. Pierrat, IC Images Technologies, Inc. (United States)

The adoption of more complex resolution enhancement techniques such as inverse lithography and source mask optimization results in extremely complicated CAD shapes with tighter specifications. As the size of the CAD shapes gets closer to the resolution limit of the mask making process, substantial distortions of the final mask can be observed, in particular corner rounding.

In this paper we will investigate the effect of mask corner rounding on simulated wafer images in the case of complicated CAD shapes.

8166-147, Poster Session

Prediction of pattern collapse hotspots for full-chip layouts

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Critical aspect ratio induced pattern collapse has been a concern for lithography process engineers since before the 180 nm node. This has driven a steady reduction in photoresist thickness, as well as accelerated the introduction of hard mask materials and processes. There have been multiple studies and proposed models for the fundamental forces which lead to pattern collapse, with consensus being that differential capillary forces across opposing sides of a developed photoresist line during the water rinse/dry step are responsible for line bending. This line bending can lead to pattern deformation or complete substrate adhesion failure. Several process improvements, such as surfactant-laced final rinse, have been proposed to alter surface energies and increase the critical aspect ratio for collapse. The mechanical models which have been proposed to explain this phenomenon have all been effectively two-dimensional, characterizing the aspect ratio (Z/X) for an idealized pattern assumed to be semi-infinite in the Y dimension. While these models are very helpful for guiding materials/process understanding and improvement, they are not as helpful in predicting real random logic "hotspots": pattern locations most likely to fail through the manufacturing process window. This work proposes a framework for full-chip prediction of pattern collapse failure by use of a semi-empirical model and an efficient geometric checking engine. Idealized test patterns are studied initially, in order to reproduce behaviors commonly reported in the literature for semi-infinite Y patterns, then more complex layout configurations are introduced. It is shown that full-chip pattern collapse can be efficiently and accurately predicted. Such a capability can prove valuable in setting design rules, and in refining RET solutions.

8166-148, Poster Session

Rigorous EMF simulation of the impact of photomask line-edge and line-width roughness on lithographic processes

O. H. Rudolph, P. Evanschitzky, A. Erdmann, E. Bär, J. Lorenz, Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany)

Line edge roughness (LER) and accordingly line width roughness (LWR) are typically studied in photoresists on the wafer level [1]. Depending on the specific dry etch process, this roughness is being transferred in more or less extent to the etched layers below the resist [2, 3]. Yet, this is not only true in the fabrication of devices, but also during production of lithographic photomasks. This work aims at exploring the magnitude and hence relevance of these mask non-idealities on the subsequent lithographic process by rigorous EMF simulation. The simulations are all carried out using Dr.LiTHO [4].

LER, i.e. surface roughness of the mask feature sidewalls, is modeled using known approaches for the description of self-affine surfaces of solids employing the height-height autocorrelation function [5, 6] and an appropriate convolution algorithm based on the Wiener-Khinchin theorem [7, 8]. Surface roughness properties can be controlled via three parameters, namely amplitude, correlation length and fractal dimension. LWR depends on the LER of two opposing lines and ranges from zero (totally correlated) to twice the LER (totally anti-correlated) and is easily simulated by cloning a given line or sampling the opposing line structure anew.

Starting from lines with sidewall roughness only, complexity of the features is further increased by introduction of sidewall tapering and an additional roughness on top of the absorber, hence resulting in position-dependent transmittance, and in case of phase-shift masks (PSM) fluctuation of the phase-shift angles. The lithography simulation is performed using the waveguide rigorous EMF solver [9, 10] in contrast to the finite integration technique (FIT) employed in [11]. Hence, the mask absorber structure has to be given in rectilinearized pieces prepared by suitable algorithmic treatment of the modeled rough surface, which will be presented here.

The free parameters of the mask model (morphological surface parameters, LWR, taper angle, roughness on top of features, line density) are being varied and the resulting near-field distributions, aerial images and process windows of a state-of-the-art lithography step (MoSi absorber, 193nm unpolarized light source at 0-angle incidence, 4X reduction) for 45nm isolated and dense lines (on the substrate) are being analyzed. Furthermore, applicability of the complex mask model in EUV simulations will be tested, experimental knowledge for comparison is available from [12].

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8166-149, Poster Session

Accurate prediction of 3D mask topography induced best focus variation in full-chip photolithography applications

P. Liu, Brion Technologies, Inc. (United States)

As semiconductor feature sizes continue to shrink, the allowable error margins for critical dimension (CD) control are getting increasingly tight due to decreased process window. One of the limiters to the process window is best focus variation among different device features. When different features have different best focus locations, the common process window is reduced even if each individual feature has a large depth of focus of its own. Therefore it is extremely important for a lithography simulator to predict this effect accurately so that potential problems can be identified and corrected at the design stage.

Although the best focus can be affected by many factors, 3D mask topography is the leading cause to best focus variation among different device features. 3D mask topography produces phase “errors” between zero-order and higher-order mask diffractions. These phase errors vary from feature to feature, causing best focus variation among these features. Oblique incidence also plays an important role in determining these phase errors. It should be noted that these effects are completely absent in the thin mask model of Kirchhoff approximation, therefore it cannot be used to predict the related best focus variation. Although rigorous 3D mask models based on methods such as Finite Difference Time Domain (FDTD) and Rigorous Coupled Wave Analysis (RCWA) can model these effects accurately, they are computationally too expensive for full-chip applications such as full-chip Optical Proximity Correction (OPC), Source-Mask Optimization (SMO) and verifications. These applications require approximate 3D mask models that are sufficiently fast (runtime < 2x of thin mask model) as well as capable of accurately modeling 3D scattering effects under oblique incidence.

In this paper, we first discuss the origin of best focus variation and its modeling requirements. We then describe the Illuminator-Aware M3D, a fast 3D mask model developed by ASML Brion that takes into account oblique incidence effects of the illuminator. We will evaluate its accuracy in predicting of best focus variation among various 1D and 2D features by comparing the results with those of rigorous 3D mask model based FDTD method.

8166-150, Poster Session

Improving the accuracy of the bimetallic grayscale photomasks using a feedback controlled flat-top beam

G. H. Chapman, R. Qarehbaghi, Simon Fraser Univ. (Canada)

Bimetallic grayscale photomasks contain two thin layers of metals (Bismuth-on-Indium or Tin-on-Indium), 15-300nm thick on transparent substrates. Laser exposure converts the films by thermal reaction into transparent alloy oxides. The Optical Density changes from ~3.0OD (unexposed) to <0.22OD (fully exposed), creating either binary or grayscale masks applications. OD is controlled by the power and duration of the laser spot. Using previously presented direct-write raster-scan photomask system with a multiline CW Argon-ion laser, 64 gray-level mask was achieved. Important limitations are stability of the laser power and beam shape creating fluctuations in the gray-levels. Writing open-loop creates average error of ±4.2 gray-levels that limits the resolution to 6-bit accuracy. Variations in the laser power distribution, especially in the focused Gaussian profile spot, influences the resulting mask pattern and makes fluctuations in the achieved gray-levels. To reduce mask nonuniformity, the closed-loop approach is used for writing the mask. Adding sensors to the beam path before and after the mask turns the system to a real-time OD and beam measurement feedback system. This feedback compensates for changes in film parameters: film thickness and characteristics plus laser power fluctuations. Although using a feedback control reduces

the amount of error to ±0.3 gray-levels and yields to a potential 256 gray-level mask, nonuniformity due to the Gaussian shape still limits resolution. Partially exposed spaces between the patterned lines combined with the laser's Gaussian distribution makes the feedback control system overestimate the writing parameters and cause variations in gray-level across the line. An interlaced raster-scanning approach reduces these variations. To further remove the Gaussian fluctuations, a diffractive beam shaper creates a nearly flat-top power distribution. To profile the beam shape we first image the transmission patterns of exposed spots in the Bi/In film. Best result was a beam with a 5.8% SD variation in its flat-top and edges with a 5.3 aspect ratio. To remove nonlinear characteristics of the film a beam profiler for these small spots is being developed. Using the shorter Argon lines (458 and 365nm) makes the OD measurements replicate those experiences during lithography. The OD system also allows us to profile the grayscale levels in more detail after writing. To further reduce variations, a beam optical stabilizer is added to maintain power within 0.03% which enhances the feedback effectiveness. A full 8-bit picture was written on a test mask with the feedback system showed significant improvement in the number of gray-levels. Some fluctuations were observed at the final pattern due to spaces between lines and nonuniformity of table speed. The same test pattern is written on the mask using flat-top beam combined with the feedback system to demonstrate the accuracy and grayscale abilities of the bimetallic thin-films. In addition, multiline patterns are written on the mask to compare the results of the flat-top and Gaussian shaped focused laser beams using interlaced raster-scanning and OD feedback control.

8166-210, Poster Session

Improvement of polymer type EB resist sensitivity and line-edge roughness

M. Otani, Yamaguchi Univ. (Japan)

In order to improve sensitivity and line edge roughness (LER) for electron beam (EB) lithography, the positive-type polymer resists with various molecular weights and controlled dispersion were newly synthesized and examined. The synthesized resists have the same composition as ZEP520A (Nippon Zeon). With the low molecular and the narrow dispersion resist, improvements of both the sensitivity and LER are confirmed by obtaining the SEM images of line and space resist patterns exposed by EB writing system at an acceleration voltage of 100 kV. The polymer resist with molecular weight (Mw: 30k) and dispersion (1.4) exhibited 22 nm hp resolution, 20 % improved LER and 15 % improved sensitivity compared with original ZEP520A.

8166-211, Poster Session

22-nm node ArF lithography performance improvement by utilizing mask 3D topography: controlled sidewall angle

H. Watanabe, Dai Nippon Printing Co., Ltd. (Japan)

No abstract available

8166-212, Poster Session

In-die job automation for PROVE

D. Beyer, Carl Zeiss SMS GmbH (Germany)

The increasing demands for registration metrology for repeatability, accuracy, and resolution in order to be able to perform measurements in the active area on production features have prompted the development of PROVETM, the next-generation registration metrology tool that utilizes 193nm illumination and a metrology stage that is actively controlled in all six degrees of freedom. PROVETM addresses full in-die capability for double patterning lithography and sophisticated inverse - lithography schemes. Innovative approaches for image analysis, such as 2D correlation, have been developed to achieve this demanding goal.

8166-213, Poster Session

Solution for silicon performance using large field of mask images

R. Matsuoka, Hitachi High-Technologies Corp. (Japan)

No abstract available

8166-214, Poster Session

EB resolution capability with CP exposure

M. Kurokawa, Advantest Corp. (Japan)

Better resolution capability of CP exposure technology, which is one of advantages of the technology, is evaluated. With CP-technology, 14nm~20nmHP 1:1 LS patterns are resolved. And this is the first report of 6025-Quartz substrate exposure of MCC-POC exposure tool.

CP exposure is not only a valuable technology to improve the throughput of EB-lithography tool combining with the Multi-Column-Cell technology, but also expected to have a better image resolution capability. Because CP is different form VSB which has two object planes, it is a simple optical system to project an object plane to an image plane.

The evaluation is performed with 10-times magnification CP-pattern openings etched through a 2-micrometer thickness membrane SOI CP-mask fabricated by DNP. 50nmt ZEP520 resist on 6025-Quartz blanks and 20nmt HSQ resist on 300mm Si wafers are used as exposure substrates.

Each set of 10-LS patterns are exposed by a single-line rectangle CP apertures which is 80nm~100nm width and 4 micrometer length. 10-sequential exposure with appropriate position stepping by electro-static deflector makes 10-LS patterns.

As a result, 14nmHP 1:1 LS patterns are resolved by HSQ resist on Si-wafer, 20nmHP 1:1 patterns are resolved with ZEP on 6025-Quartz blanks.

This evaluation is performed by a MCC-POC tool which is developed as a NEDO project and authors express a gratitude for their support.

8166-215, Poster Session

Elimination of lithographic hotspots which have been waived by means of pattern matching

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A persistent problem in verification flows is to eliminate waivers defined as patterns that are known to be safe on silicon even though they are flagged by the verification recipes. The difficulty of the problem stems from the complexity of these patterns, and thus, using a standard verification language to describe them becomes very tedious and can deliver unexpected results. In addition, these patterns have a dynamic nature, hence, updating all production verification recipes to waive these non critical patterns becomes more time consuming.

In this work, we are presenting a new method to eliminate waivers directly after verification recipes have been executed, where a new rule file will be generated automatically based on the type of errors under investigation. The core of the method is based on pattern matching to compare generated errors from verifications runs with a library of pattern waivers. This flow will eliminate the need to edit any production

recipe, and complicated coding will not be required. Finally, this flow is compatible with most of the technology nodes.

8166-216, Poster Session

Efficient method for SRAF rule determination

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No abstract available

8166-217, Poster Session

MRC optimization for EUV high-NA imaging for the 32-nm HP technology node

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EUV is considered as the most promising candidate for manufacturing advanced semiconductors at the 32nm HP technology generation and beyond. It has been demonstrated that the ASML TWINSCAN NXE:3100 is able to print 27nm lines and spaces and 32nm contact holes with NA0.25. Moving forward, higher NA EUV system such as the ASML TWINSCAN NXE:3300B can generate a higher contrast aerial image due to improved diffractive order collection efficiency and is expected to achieve a greater percentage of under-exposure or dose reduction via mask biasing. In this work, we study by simulation the benefit of EUV high NA imaging in the MRC (Mask Rule Check) trade-offs required to achieve the viable manufacturing solutions for two device application scenarios: 6T-SRAM contact layer for the logic 14 nm technology node, and 32nm half pitch NAND Flash contact layer. The 3D mask effects versus Kirchhoff mask for these two applications are also investigated.

8166-218, Poster Session

Durability of Ru-capped EUV blanks cleaned with CO2 cryogenic aerosol

C. W. Bowers, Eco-Snow Systems (United States)

No abstract available

8166-219, Poster Session

CD-metrology of EUV masks in the presence of charging: measurement and simulation

S. V. Babin, Abeam Technologies (United States)

No abstract available

8166-31, Session 11

Advanced electron-beam resist requirements and challenges

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High end photomask manufacturing relies heavily on chemically amplified resists (CARs) for electron beam lithography. Historically, an electron beam CAR material could cover many process nodes. However, as photomask CD requirements have scaled to where they're approaching wafer dimensions, electron beam resist process development and optimization has become more challenging. Today, nearly every node requires a new resist, largely to balance resolution and exposure dose requirements.

Intel Mask Operations has a long history with CAR materials, and has active programs in evaluating and optimizing new resists. This paper will discuss the performance metrics that Intel investigates as it screens new resist candidates, and show relative capabilities between the resists of our various manufacturing nodes. We'll consider basic performance metrics such as exposure dose requirements, resolution, profile, linearity, line edge roughness and process windows. We'll also discuss materials requirements unique to mask manufacturing, especially the need for low sensitivity to processing conditions (post-coat delay, post-exposure delay, amine levels, duration under vacuum, etc).

We'll investigate practical manufacturing considerations of materials performance, such as the need for in-house materials coating and corrections schemes for process sensitivities. In addition, we'll investigate fundamental aspects of electron beam materials formulations, and their similarities and differences to optical CAR materials. Finally, we'll look at future trends and discuss where additional work is most needed.

8166-32, Session 11

High-resolution mask process and substrate for 20-nm and early 14-nm node lithography

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The lithography challenges posed by the 20 nm and 14 nm nodes continue to place strict minimum feature size requirements on photomasks. The wide spread adoption of very aggressive Optical Proximity Correction (OPC) and computational lithography techniques that are needed to maximize the lithographic process window at 20 nm and 14 nm groundrules has increased the need for sub-resolution assist features (SRAFs) down to 50 nm on the mask. In addition, the recent industry trend of migrating to use of negative tone develop and other tone inversion techniques on wafer in order to use bright field masks with better lithography process window is increasing the need for mask makers to reduce the minimum feature size of opaque features on the reticle such as opaque SRAFs. Due to e-beam write time and pattern fidelity requirements, the increased use of bright field masks means that mask makers must focus on improving the resolution of their negative tone chemically amplified resist (NCAR) process.

In this paper we will describe the development and characterization of a high resolution bright field mask process that is suitable for meeting 20 nm and early 14 nm optical lithography requirements. Work to develop and optimize use of an improved chrome hard mask material on the thin OMOG binary mask blank[1] in order to resolve smaller feature sizes on the mask will be described. The improved dry etching characteristics of the new chrome hard mask material enabled the use of very thin (down to 65 nm) NCAR resist. A comparison of the minimum feature size, linearity, and through pitch performance of different NCAR resist thicknesses will also be described. It was found that the combination of the improved mask blank and thinner NCAR could allow achievement of 50 nm (and smaller) opaque SRAFs on the final mask. In addition, comparisons of the minimum feature size performance of different NCAR resist materials will be shown. A description of the optimized cleaning processes and cleaning durability of the 50 nm opaque SRAFs will be provided. Furthermore, the defect inspection results of the new high resolution mask process and

substrate will be shared. Lastly, examples of early wafer printing results achieved with the new bright field masks will be shared.

[1] “Development and Characterization of a Thinner Binary Mask Absorber for 22 nm Node and Beyond,” T. Faure et. al., Proc SPIE, 7823, 7823J1-J12, (2010).

8166-33, Session 11

Phase-shifting effect of thin-absorber EUV masks

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Thin-absorber EUV masks have been proposed in the past [1, 2]. The discussions have been mainly focused on the shadowing effect. Thinner absorber is preferable to reduce the horizontal to vertical (H-V) line width bias on wafers. However, it should be noted that the phase-shift value of the EUV mask depends on the absorber thickness. For TaN absorber the value becomes 180 degrees around 65 nm absorber thickness. The reflectivity ratio between the absorber and the multilayer also depends on the absorber thickness. The value is about 2% at 65 nm absorber thickness. Therefore thin-absorber EUV masks should be considered as a kind of embedded attenuated phase-shifting masks (EPSMs).

EPSMs have several lithographic advantages over binary masks. EPSMs enlarge the process window of contact holes [3, 4]. The masks also enhance the image contrast of line patterns with off-axis illumination [5]. These effects will be reduced if the mask has a phase error [6]. For this reason 180 degree phase shift is selected for the conventional optical EPSMs.

When we vary the thickness of the absorber on the EUV mask the phase-shift value also changes. We studied the effect of the phase error on the lithographic performance both by simulations and printing tests using the alpha demo tool at IMEC. Among all lithographic performance the process window of the contact holes is the most sensitive to the phase error. We confirmed that the process window became the largest when the 180 degree phase-shift mask was used. We also studied the process window of the line patterns and H-V bias. We conclude that the best lithographic performance can be obtained by adjusting the absorber thickness to 180 degree phase shift.

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8166-34, Session 11

Closed-loop registration control (RegC) using PROVE as the data source for the RegC process

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At sub 4X nm nodes in memory and Sub 3X nodes in logic devices mask registration (Reg) is becoming a significant yield limiting factor. This is especially true for Double Patterning Technologies (DPT) where mask to mask overlay on the wafer is heavily influenced by mask registration error. Getting advanced mask registration in to specification is a challenge for all mask shops as the tight registration specs are driven by tight wafer overlay specs.

The first step in meeting the registration spec challenge in the mask shop is to be able to measure registration with the required specifications. With PROVE Carl Zeiss SMS has recently introduced into the market a new registration and overlay metrology system which utilizes 193nm illumination for high resolution and a six axes controlled stage. The second step in meeting the registration spec challenge is to actively correct for intrinsic registration errors on the mask. For this Zeiss SMS has developed the RegC tool. The RegC tool is based on writing strain zones with the help of an ultrashort laser in the bulk of the mask. The strain zones induce deformations in the mask which practically push the misplaced features to a new location that after removing the scale and orthogonality (SO) reflects smaller residual registration error.

By combining the RegC tool with data generated by PROVE it is possible to close the loop on the registration control process in the mask shop without wafer print or mask re-write. The closed loop solution works like this:

1. After completing the mask manufacturing process the mask is measured on the PROVE tool. A Pre RegC error map is prepared.

2. The Pre RegC map is loaded to a special software (SW) that calculates a registration correction job

3. The registration correction job is loaded to the RegC tool together with the mask and the RegC process is run

4. The mask is then measured again on PROVE which generates a Post RegC map.

5. The improvement in registration in terms of residual registration error in nm and % improvement is calculated and reported.

In this paper we report the results of a first demonstration of a closed loop process between PROVE and the RegC tools

8166-35, Session 11

Negative-tone e-beam resist processing for bit-patterned media NIL template

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Nanoimprint lithography (NIL) is the one promising candidate for fabricating a patterned media to be used in the next generation of hard disk drives (HDD). It is expected that the pitch will become as small as about 20 nm for more than 1 Tbit/in.2 bit-patterned media (BPM) in 2014 or 2015. Electron-beam (EB) lithography techniques realize to fabricate NIL template, and the developments with positive-tone EB resist, which are ZEP-520A or chemically amplified resist (CAR), have been mainstream so far. However, negative-tone EB resist process is necessary when we consider master or replica mold fabrication process. So negative-tone EB resist processes were developed. In this paper, we will discuss three kinds negative-tone EB resist (Nega-A, Nega-B and Nega-C) patterning performances with 100kV xy-stage EB writer (Jeol/JBX-9300FS) for NIL template process development. Three kinds EB resist are as follows:

(1) Nega-A: It is non-CAR targeting high resolution. The sensitivity is around 2500 uC/cm2. So it is not suitable for large area writing for development or trial fabrication of BPM. 25 nm pitch pillar array were resolved as shown in Figure 1. Higher packing density process is under development with thinner resist thickness.

(2) Nega-B: It is non-CAR targeting higher sensitivity around 1000 uC/cm2 for full-area patterning. 24 nm pitch land and groove was resolved as shown in Figure 2. Resist material is being improved for better edge roughness and better sensitivity.

(3) Nega-C: It is high sensitivity CAR and the sensitivity is 100~150 uC/cm2, which is higher than ZEP-520A. The minimum resolution of pillar pitch is 32 nm as shown in Figure 3. The target is for guide patterning for directed self-assembly of BPM patterning.

8166-36, Session 12

The requirements for the future e-beam mask writer: statistical analysis of pattern accuracy

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As semiconductor features shrink in size and pitch, the extreme control of CD uniformity, MTT and image placement is needed for mask fabrication with e-beam lithography. Among the many sources of CD and image placement error, the error resulting from e-beam mask writer becomes more important than before. CD and positioning error by e-beam mask writer is mainly related to the imperfect of optics and the charging and contamination of column. To avoid these effects, the e-beam mask writer should be designed taking into account for these effects. Unfortunately, the writing speed should be considered for machine design with the highest priority, because the writing time of mask with e-beam machine is too slow. Because of this constraint, the trade off study between throughput and beam quality of e-beam mask writer is needed with detail analysis of CD and position error.

In this study, the statistical approach on CD and position control ability with e-beam mask writer is applied. It is estimated for various design node including the intrinsic error of VSB writer. The limit and the size of error resulting from e-beam size and position controllability are simulated taking into account for the real effect on mask pattern quality. Based on the estimation and simulation, the required e-beam control accuracy by electromagnetic optics and the size of field covered by deflector are calculated for 22nm node and beyond. The current density to achieve relevant writing time is also studied. Consequently, the requirements for the future e-beam mask writer are suggested and it is discussed what is the promising technology among the conventional VSB and the multiple columns or beams for future mask writing.

8166-37, Session 12

The trouble starts with using electrons: putting charging effect correction models to the test

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Improvement of pattern placement accuracy is essential to solve upcoming challenges in mask making. Placement errors are driven by multiple effects with electron mediated resist surface charging being a major error source. Modeling this systematic effect thus allows the determination of the placement errors before plate processing. This opens the door to an effective charging compensation.

In this paper we study the simulated benefit of two distinct charging compensation models in the context of full-scale mask production layouts. The potential pattern placement improvements are evaluated using actual placement results obtained without charging effect corrections. An in depth comparison of the two models is presented, demonstrating the differences in placement error prediction between using a static or a dynamic charging model. We find that substantial improvements can be achieved using the dynamic charging model. Productive implementation of this functionality is the natural next step.

8166-38, Session 12

EBM-8000: EB mask writer for product mask fabrication of 22-nm half-pitch generation and beyond

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Many lithography candidates, such as ArF immersion lithography with double-patterning techniques, EUV lithography and nano-imprint lithography, show promising capability for 22 nm half-pitch generation lithography but still lack the conclusive evidence as the practical solution for actual production. On the other hand, each of the prospective lithography techniques at 22 nm half-pitch generation requires masks with improved accuracy and increased complexity.

We have developed a new EB mask writer, EBM-8000, as the tool for mask production of 22nm half-pitch generation and for mask development of 16nm half-pitch generation, which is necessary for the practical application of these promising lithography technologies.

The development for EBM-8000 was focused on increasing throughput and improving beam positioning accuracy. Three major new features of the tool are: higher brightness electron gun to achieve current density of 400 A/cm2, high speed DAC amplifier for beam deflection, and additional environmental controls.

Other features were carried over from EBM-7000 to EBM-8000; these include acceleration voltage of 50 keV, variable shaped beam with vector scanning, continuous moving stage, VSB12 data format, direct reticle handling, and reticle handling system with SMIF-Pod, among others.

The improved image placement accuracy and repeatability, and higher throughput of EBM-8000 have been confirmed by actual writing tests with our in-house machine tool.

8166-39, Session 13

In-die photomask registration and overlay metrology with PROVE using 2D correlation methods

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According to the ITRS roadmap, semiconductor industry drives the 193nm lithography to its limits, using techniques like double exposure, double patterning, mask-source optimisation and inverse lithography. For photomask metrology this translates to full in-die measurement capability for registration and critical dimension together with challenging specifications for repeatability and accuracy. Especially, overlay becomes more and more critical and must be ensured on every die. For this, Carl Zeiss SMS has developed the next generation photomask registration and overlay metrology tool PROVE which serves the 32nm node and below and which is already well established in the market. PROVE features highly stable hardware components for the stage and environmental control. To ensure in-die measurement capability, sophisticated image analysis methods based on 2D correlations have been developed. Moreover, PROVE enables different illumination settings for structure-dependent contrast optimisation.

In this paper we demonstrate the in-die capability of PROVE and present corresponding measurement results for short-term, long-term and accuracy for feature sizes down to 120nm and different illumination modes. It is shown that a suitable illumination setting

enhances the contrast of in-die features and consequently improves the measurement repeatability. Moreover, we directly compare standard measurement methods based on threshold with the new 2D correlation methods to demonstrate the performance gain of the latter.

In addition, mask-to-mask overlay results of typical box-in-frame structures down to 200nm feature size are presented. It is shown, that from overlay measurements a reproducibility budget can be derived that takes into account stage, image analysis and global effects like mask loading and environmental control. The parts of the budget are quantified from measurement results to identify critical error contributions and the corresponding improvement strategies.

8166-40, Session 13

Evaluation of KLA-Tencor LMS IPRO5 beta system for 22-nm node registration and overlay applications

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Using various technical tricks, 193nm lithography has been pushed for the 22nm node. For optical and EUV lithography, the International Technology Roadmap for Semiconductors (ITRS [1]) requests a registration error below 2.7 nm for masks for single-patterning layers. Double patterning further reduces the tolerable pattern placement error to < 1.9 nm for each mask of a pair that forms one layer on the wafer. For mask metrology on the 2x node, maintaining a precision-to-tolerance (P/T) ratio of 0.25 will be challenging. The total measurement uncertainty has to be significantly below 1.0nm.

In this work, results obtained during the LMS IPRO5 beta system evaluation at the AMTC mask shop are presented. LMS IPRO5 beta system evaluation is part of the CDUR32 project, funded by German Federal Ministry of Education and Research.

Position measurement uncertainty as function of critical dimension (CD) is evaluated using an analysis of variance (ANOVA) methodology. In addition, the new center of gravity (CofG) measurement algorithm, important for in-die measurement capability, is evaluated in terms of repeatability, reproducibility, isotropy and manufacturability (e.g. recipe setup). The results are compared with results obtained using the traditional edge detection algorithm.

A major improvement to previous LMS IPRO generations is the new 266nm laser illumination system, which significantly improves optical resolution and contrast (especially on EUV substrates). Therefore, optical resolution and measurement capability are evaluated using standard registration targets and arbitrary shaped features on different substrates comprising EUV and binary MoSi masks. Furthermore, through-pellicle measurement results using a new adaptive mask bending model are presented.

[1] ITRS: International Technology Roadmap For Semiconductors 2010 Update

2010 Tables, 2010Tables_LITHO_FOCUS_D_ITRS.xls

URL http://www.itrs.net/Links/2010ITRS/Home2010.htm;

8166-112, Session 13

Measuring critical dimension in SEM mask images

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In semiconductor industries, controlling and measuring critical dimension (CD) are two important issues to design masks. However, measuring the critical dimensions with physical tools are almost impossible since the range of the size becomes smaller towards the wave length of the light, like in scanning electron microscopy (SEM) images. Also, the traditional method of measuring is complicated and has many processes though it is accurate. This paper suggests a method that measures the critical dimension length accurately in short time using only SEM images based on the digital image processing.

Our proposed method consists of two stages: image enhancement and CD measurement. In the first stage, this paper suggests that the noise in SEM images cannot be modeled as a simple Gaussian but it is rather close to speckle noise. Speckle noise is defined as a granular noise that inherently exists in other signals such as the active radar and synthetic aperture radar (SAR) images. Speckles are spread over and affect the entire SEM images and make the intensity curve too rough to fit our model function. Also, the speckles cannot be simply removed by window filters. Therefore, we applied non-linear anisotropic diffusion filtering to smooth the intensity curve modestly, while preserving the location of edges.

In the next step, we fit our model function which is Gaussian mixture to the refined intensity curve. For fitting and estimation of the parameters, we use Levenberg-Marquardt algorithm. Then we can calculate the positions where the peak intensity occurs very accurately by solving the fitted curve equation. Here, we assumed the distance between the peaks to be CD although there are many other criterion about CD.

In our experiment and implementation, the filter worked quite well since the smoothed curves were smooth enough to fit the model function while maintaining the position of the peak. Also, the fitting results were good because the RMS errors, which show how far the model curve is deviated from the actual data curve, were below 0.1 for all samples and obtained CDs were accurate.

In conclusion, we suggest a method by combining two algorithms: image enhancement and curve fitting. Since the entire process starts from only SEM mask images, our method is very easy to implement and does not need special devices Also, the process is fast and the results are good.

8166-42, Session 14

Repair of natural EUV reticle defects

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Extreme ultra-violet lithography (EUVL) is the leading candidate for 22nm half-pitch device manufacturing as well as the only technique considered extendible beyond 16nm half-pitch. Reticle defectivity remains a very critical challenge before EUVL can be considered fully ready for use in future production of such integrated circuits.

Whereas EUV reticle defectivity has many aspects, this paper will focus on repair, both of absorber defects and the defects of the EUV-specific multi-layer mirror (so-called ML-defects). The former are overcome by the conventional type of repair, but require a dedicated process, which also needs to be confirmed by printing. The ML-defects (either bumps or pits) are very challenging as they print from just a few nanometer height, respectively depth, onwards. Additional efforts are required to have sufficient detection sensitivity during dedicated blank inspection. Activities of the blank vendors are ongoing to minimize the density of natural ML-defects. Another mitigation approach shifts the pattern to assure that the few remaining ML-defects will be underneath the absorber. Now we report about additional mitigation by repair, anticipating that not all printing ML-defects are satisfactorily detected on the blank, nor successfully mitigated by the pattern shift technique. Because removing the defect itself is not possible, repair of ML-defects is done by compensation of the absorber pattern for their presence. The feasibility was previously shown by simulation, but the present talk will include experimental results.

Whereas the input for absorber repair can be fully obtained by mask review using CD-SEM, this is not satisfactory for ML-defects. Their very shallow nature makes them often even totally invisible. Atomic Force Microscopy (AFM) is extremely helpful for visualization, but this is restricted to the surface of the ML mirror. As to optimize the compensation repair through-focus printing behavior is considered

additional input. Repairs are performed using the ebeam based Carl Zeiss MeRiT (R) repair technology. Wafer printing on the ASML EUV Alpha Demo Tool (ADT) installed at IMEC is used to determine the success rate of the repairs.

The paper will start from the printability of natural defects and their characterization on mask by SEM and AFM. Subsequently, the success of absorber defect repair (both opaque and clear type) will be illustrated. For compensation repair of ML-defects we report first experimental proof of the technique, with very promising results for both natural pits and bumps. We apply simulation to investigate the limitations of such compensation repair, based on the residual printability determined experimentally. As an example it was identified that alignment of the compensation repair shape with the ML-defect position is very critical. The integration of an AFM capability into the repair tool will be discussed as a measure to improve this.

8166-43, Session 14

EUVL mask inspection using 257-nm and 193-nm wavelengths for 30-nm node and beyond

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In this paper, we studied the performance of EUVL masks using both 257nm and 193nm inspection tools. We discussed both image contrast and detection sensitivity on programmed test masks. Among three blanks, the thin absorber showed the best detection rate. It was very difficult to get high image contrast due to the lack of reflective light as the pattern size reduced. These phenomena were critical in HP 30nm as well as HP 25nm. We stretched the image signal to increase the image contrast to overcome the limitation of the 257nm wavelength system. The result showed that the image contrast was significantly improved about four times. Although we tried to increase the image contrast to obtain higher detection sensitivity, the result was not good enough to satisfy the all wafer printing lines. With the result, we conclude that our 257nm wavelength inspection system cannot cover the HP 30nm.

In 193nm wavelength system, we tested influences on focus offset and illumination optic condition and considered to increase the capability of detecting small defects. We tested detection sensitivity on through focus and we found that it was still not satisfied all wafer printing lines. However we confirmed that OAI could solve this problem. We saw the smallest isolated defect on C/H pattern at HP 30nm and the size was about 25nm. And the defect was not printed on the wafer. The size of the defect printed on the wafer was measured to be 37nm, which is the smallest one we have found. For HP 24nm, we found that focus variation could change the image contrast significantly however the detection sensitivity did not fully increased by the image contrast. Further study is needed in order to confirm whether current optical inspection tools can cover HP 30nm and beyond.

8166-44, Session 14

Printability and detection of backside defects on photomasks

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Defects on the backside of photomasks are usually considered as uncritical and thus do not receive much attention. Such defects are out of focus during wafer exposure by the mask thickness and cannot be directly imaged on wafer. However, reticles are contaminated during its lifetime and can catch particles as large as several tens of microns. Although out of focus, the shadow of such particles locally changes the illumination of the mask patterns and may result in a long-range CD variation on wafer depending on NA and pupil shape.

There have been only a few investigations on printability of backside defects in the past, and no data are available for the most advanced technology nodes. Reticles are regularly scanned for particles on the glass side in the wafer fab but limits for acceptable defect size are based on estimations. Detection of particles beyond that limit causes either delay or rework of exposed wafers with impact on throughput and cost performance. It is therefore important to gain better understanding of critical sizes of backside defects and of appropriate detection capabilities.

We have designed and manufactured a test mask with repeating patterns of 20nm, 28nm and 40nm technology node ranging from contact and line/space critical layers to non-critical implant layers. Programmed chrome defects of varying size are placed on the backside opposite to the repeating front side patterns in order to measure the spatial variation of wafer CD in respect to defect position. The test mask was printed on a bare Silicon wafer and the size of printed features was measured by spatial sampling. Wafer CD variation for different backside defect sizes are demonstrated and compared for several layers.

The opaque chrome defects on the backside are considered as worst case compared to real particles. The study aims on deriving a print threshold for backside particles based on actual wafer data. After such critical size of backside defects is obtained the reticle was also utilized to investigate the detection ability of backside defects by reticle or wafer inspection tools, respectively.

8166-45, Session 14

Clean and repair of EUV photomasks

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Regardless of at what technology node it will be implemented, extreme ultraviolet (EUV) lithography appears to be the most likely successor to 193 nm wavelength lithography. However, EUV photomasks present new and different challenges for both repair and clean processes. Among these are, different and more complex materials, greater sensitivity to smaller topography differences, and no pelliclization of critical pattern areas. Solutions developed and recently refined to meet these challenges are reviewed as an integrated solution to make the manufacture and maintenance of this mask type feasible. This integrated solution includes both nanomachining and laser processes applied for hard (missing pattern) and soft (nanoparticle) removals with no damage to underlying multilayers.

8166-46, Session 15

Challenges associated with advanced mask cleaning

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Historically, photomask and wafer cleaning have been considered trivial tasks. The primary challenge has been simply the removal of particles that may have an impact on final product yield. As wavelengths decrease and energy on the image plane of the reticle increase the degree and complexity of surface contaminants on the reticle become more complex. The result is that the mask fabricator is faced with two new challenges; reducing and identifying the types of contaminants on the reticle prior to exposure in the wafer fab and eliminating contaminants that have been deposited in the fab. These contaminants are often different in that 193nm exposure produces higher molecular weight contaminants that can be more difficult to remove. While the effects of these contaminants may not be serious for transmissive lithography, their effects can be catastrophic for reflective lithography, such as Extreme Ultra Violet (EUV) lithography.

We will provide results showing the types of contaminants commonly found on various types of reticles and the respective challenges associated with their removal.

8166-47, Session 15

Study on the soft defects related to dry etch process of phase shift mask

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Soft defect, generated during the photomask manufacturing process requires additional cleaning, repair and inspection process and it affects on MCT (manufacturing cycle time) and PTS(performance to schedule) negatively. Especially, soft defects related to vacuum chamber process such as dry etching are hard to remove in conventional cleaning process. Some soft defects on MoSi layer with round shape, smooth surface, and very thin thickness showed higher transmittance than MoSi layer and looked like half-tone pin-hole. Also, the defect was hard to detect in conventional PSM inspection tool because of its special characteristics mentioned earlier. We found that the defect is caused by co-interaction of dry etch and cleaning process in PSM manufacturing process.

In this paper, we studied on the root cause of the dry etch process related soft defect and its control method.

8166-48, Session 15

Effect of cleaning POR upon EUV mask performance

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EUV lithography uses light reflected from the mask surface, whereas optical lithography uses the light transmitted through a mask substrate for the patterning of features on the wafer. As such, the materials used to build the mask have to be changed from transparent to reflective. EUV mask structures include many different layers of various materials rarely used in optical masks, and each layer of material has a certain role in enhancing the performance of EUV lithography. Therefore, it is crucial to understand how the original properties and surface topographies change during mask fabrication, EUV exposure, storage, or maintenance processes.

Mask cleaning is the process that a mask is subject to more frequently than any other fabrication or maintenance processes. The fact that a pellicle is not allowed to be utilized for mask surface protection in EUV lithography signifies that EUV masks may have to go through more cleaning cycles during their lifetime. The requirement of more frequent cleaning cycles, combined with the adoption of new materials for EUV masks emphasizes that mask manufacturers should closely examine the performance change of EUV masks during cleaning process.

In this paper, we will investigate how EUV mask layers are affected by cleaning POR combined with EUV exposure. In this investigation, film loss of the ruthenium capping, tantalum-based absorber and ARC layers will be determined. Also, changes in the chemical composition and adhesion property of each layer during cleaning and exposure processes will be addressed. Finally, whether mask performance can be maintained following multiple cleaning cycles by way of EUV patterning or actinic inspections will be discussed.

8166-49, Session 15

Study of tolerance of the patterned EUV masks to the megasonic cleaning by scanning probe microscopy

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EUV lithography (EUVL) is considered as the most attractive solution for semiconductor device manufacturing beyond 22nm HP node. Lack of pellicle makes EUV masks prone to particle contamination. Mask cleaning processes should remove all of defects larger than 25nm without any damage to 78nm and even smaller patterns for 23nm Flash HP node according to ITRS [1]. In addition EUV masks introduce new materials and multilayer structure that is different from Cr on glass used in traditional optical mask. Physical forces applied by the megasonic cleaning for particle removal on an optical mask might damage EUV mask patterns. Therefore, it is important to determine the magnitude of the physical forces which result in patterned absorber line (TaN or TaBN) separation or even breakage from surface of Ru capped MoSi multilayer film. Meantime adhesion of particles of interest for EUV to surfaces of Ru capped multilayers and TaN, TaON absorber and TaBON anti reflective coating should be measured. In the complex structure of a EUV mask, adhesion forces of particle top surface are modified with presence of different layers underneath of the surface.

Therefore, it is crucial to directly measure adhesion forces of the particles to the surface as well as force required for removal of a particle from the surface and compare it to the force required for pattern damage to determine process window for the cleaning process.

We utilized Scanning Probe Microscopy (SPM) technique to quantify these forces. Figure below shows an example for the breakage force measurement of 74 nm width pillar pattern. As one can see in the AFM images before and after scanning, the pillar pattern was successfully removed from the surface by a diamond probe using the nano-manipulation option of the SPM tool. Breakage force can be calculated from deflection of SPM probe as a function of time as it is shown in the right graph in the figure.

In this paper, we will present the measured breakage forces for absorber patterns as a function of their size on Ru capped EUV blanks and compare them with removal forces of 50nm and 100nm SiO2 and PSL particles. Based on these data and our analysis we will demonstrate available process window for successful cleaning of EUV masks for beyond 22nm HP node.

8166-50, Session 15

Effects of repetitive acid-based cleaning on EUV mask lithography process and lifetime

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As EUV transitions into high volume manufacturing, a cleaning method must exist for reticles capable of removing the molecular and particle contamination resulting from storage, handling and exposure cycles. Current acid-based cleans have been shown to satisfy these requirements; however, the durability of EUV reticles as regards repetitive processing (>30x) has not been fully investigated in terms of changes in EUV reflectivity, LER and wafer print imaging performance, until now.

In this study, the impact of repetitive cleaning of EUV masks on reflectivity, surface roughness and imaging performance was evaluated. Two reticles were fabricated using commercially available EUV blanks and patterned with the same layout; one was subjected to multiple cleaning and the other one was kept as a reference. Wafers were patterned using both reticles on the SEMATECH Berkeley 0.3

NA micro-field exposure tool (MET) and the exposure data was used to determine lithographic performance (process window, line edge roughness, etc.) at regular intervals between cleans processing. Additionally, surface roughness and EUV reflectivity were also measured.

8166-51, Session 16

In-die registration metrology: advanced marking solution

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Traditionally the mask data information communicated to the mask registration tool via a job recipe file was relatively simple typically consisting of the coordinates of the measurement targets and one or two dimensions of those targets. However, this easy approach on registration targets is not applicable anymore when significantly tighter mask-to-mask overlay specification will require in-die registration measurement.

In order to meet the requirements of in-die registration metrology an application interface for registration job generation must adapt and provide additional capabilities including finding the best suitable registration targets from a large number of potential targets.

As a continuation of in-die registration metrology advancement effort, this paper introduces new Synopsys marking interface for creating KLA-Tencor LMS IPRO5 job recipe file and describes a model for an advanced in-die marking application for the LMS IPRO5 registration system and how it fits within a production environment flow as an automated and flexible solution.

8166-52, Session 16

EUV and x-ray scattering methods for CD and roughness measurement

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Scatterometry is a common technique for the characterization of nano-structured surfaces. Currently, its main application in semiconductor industry is relative metrology for process control and process development. The goal is to establish scatterometry as traceable and absolute metrological method for dimensional measurements. Numerical methods can be used to calculate the reflected and diffracted light intensities from the geometry of the object. Inversely, the properties of the object are derived from an optimization which minimizes the difference between the measured and calculated intensities. Scattering with short wavelength radiation using higher diffraction orders from a periodic test field in principle increases the sensitivity to structure details. Consequently, the use of X-rays for CD measurements on wafers was proposed [1] . We have recently shown that higher diffraction orders in scatterometry at rough structures are subject to a Debye-Waller-like exponential damping as the Bragg-peaks in classical X-ray diffraction due to thermal oscillations [2] . In an analysis of experimental EUV and DUV scatterometry data [3] for an EUV photomask, it was also shown that the influence of this roughness induced intensity damping dominates any other uncertainty in the structure reconstruction using angular resolved scatterometry [4] .

We will demonstrate that the inclusion of the roughness induced intensity damping simultaneously provides access to the structure roughness and improves the quality of the structure reconstruction. This is complementary to the use of diffuse scatter for the determination of roughness as previously proposed [5] . Small angle X-ray scattering (SAXS) was used in transmission mode for CD measurements at wafers. For photomasks, it is not useful because the mask substrate is too thick for transmission measurements. Therefore, we used grazing incidence SAXS, i.e. the measurement of the scatter around the reflected X-ray beam in total reflection geometry. The disadvantage of this method regarding investigations on photomasks is that it requires rather large test fields because of the elongated footprint of the photon beam under grazing incidence. We will demonstrate the GISAXS diffraction pattern of periodic lines for large optical diffraction gratings to point out how generally structure parameters show up in these measurements. The example of an EUV test mask is also shown. Here, the beam overfilled the test fields and the scatter figures became rather complex due to contributions from adjacent areas of the mask. The evaluation of the diffuse scattered light is therefore strongly compromised. The evaluation of the coherent orders of the test grids, however, is possible and yields an estimation of the roughness using the Debye-Waller-like damping factor.

It is shown that structure roughness and non-regularity strongly influences the structure reconstruction from angle resolved short-wavelength scatterometry. Inclusion of the roughness into the model provides simultaneously a better structure reconstruction and information on the roughness from the discrete diffraction orders rather than the diffuse background.

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8166-53, Session 16

Investigation of 3D patterns on EUV masks by means of scatterometry and comparison to numerical simulations

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Extreme ultraviolet (EUV) lithography at a wavelength of about 13 nm is expected to replace DUV photolithography for semiconductor manufacturing of integrated circuits at the 16 nm technology node and beyond. With the decreasing feature sizes the tolerance budgets of mask pattern dimensions get tighter. High-throughput and high-accuracy metrology of such structures at mask and wafer level has to be performed for characterization and process control.

In previous works we have shown that EUV scatterometry is a fast and robust method for characterizing lines profiles within 1D-periodic test patterns (line masks) [1]. In this contribution we extend our research to the characterization of 2D-periodic patterns (e.g. arrays of contact holes) which potentially also include real IC production structures.

Briefly, in our method we compare the measured intensity distribution of EUV light scattered off the sample to the results from numerical simulations of the setup with different sets of geometrical input parameters. Mask geometry is then determined by optimizing geometrical input parameters of the numerical simulations such that differences between measurement and simulation are minimized.

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8166-54, Session 16

Addressing 3D metrology challenges by using a multiple detector CDSEM

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In NGL for the 22nm node and beyond, the 3D shape (SWA, Height) measurements of the photomask pattern become critical for controlling the exposure characteristics and wafer printability. Until today, cross-section SEM and AFM methods are used to make 3D measurements, however, these techniques require time consuming preparation and observation.

This paper presents an innovative technology for 3D measurement using Multiple Detector CDSEM and reports its accuracy and precision.

8166-55, Session 16

The assessment of the impact of mask pattern shape variation on the OPC-modeling by using SEM-contours from wafer and mask

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Hitachi High-Technologies has continued to develop “Technology for improving OPC model quality by using SEM-contours”. Many challenges of contouring for a hybrid modeling have been the subject of various articles. Advanced SEM contouring technology which is combined with CD-gap-free contouring, Fine SEM Edge (FSE) technology, alignment and averaging method on 2D arbitrary structures was developed. CD-gap-free contouring makes smaller bias between Top-down CD and SEM-contour CD. FSE makes an equal SEM edge quality for horizontal and vertical edges from a SEM image. Alignment and averaging method eliminates rotation and XY shift error between Wafer SEM-contours for averaging and reducing roughness impact. In SPIE2010, Contour-based OPC-modeling by using Advanced Wafer SEM-contours on 2D arbitrary structures was examined, and shown that OPC model quality on 2D was significantly improved to RMS 1.32nm.

Yet there are still several error factors over the whole OPC calibration procedure. We think Input Design Data, other than the factors that we reported in SPIE2010, would be a negative impact for OPC calibration. A regular hybrid method is calibrated with conditions of an optical model, a resist process model and a mask process model, 1D CD measurements and 2D Wafer SEM-contour. However the pattern shape on Design Data is square. It is quite different shape from the actual pattern shape on a wafer especially at corner rounding. Therefore it may be a big error factor for OPC model calibration. Thereby, Mask SEM-contours instead of Design Data for 2D area were input into calibration in this study. We call this new method an advanced hybrid method.

Mask SEM-contours are expected to improve the model quality at corner rounding, because they are close to the pattern shape on the wafer on which Mask SEM-contour is an actual unlike Design Data. Hitachi High-technologies has produced CG4500 which is a Mask CD-SEM and CG4100 which is a Wafer CD-SEM. SEM-contours can be created with same algorithm for both of Mask and Wafer on DesignGauge-Analyzer.

In this study, three OPC models are compared by using these technologies. First model is created with a CD-based calibration procedure with 1D and 2D CD measurements. Second model is created with a regular hybrid method using CD measurements for 1D and Wafer SEM-contour for 2D. Third model is created with an advanced hybrid method using additional Mask SEM-contour instead of Design Data for 2D. Moreover Verification is done and the quality of three models is compared by CD error and corner fitting.

8166-56, Session 16

X-ray metrology for characterizing shape of nanostructure of bit-patterned medias

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The use of patterned media is extensively studied in order to overcome superpar-amagnetic problem and to increase the areal density of magnetic disk drives. In patterned media, the magnetic layer is created as an ordered array of isolated bits. The size, shape, and pitch of those bits are directly related with signal intensity and noise of the media, and they are expected to be highly controlled for better read/write performance [1]. However it poses serious challenges for metrology tools to characterize the crucial structure of those patterns with only few-tens of nanometer or smaller dimensions.

In the above situation, we have been developing a nanoscale metrology by employing x-ray scattering (diffraction) technique. Traditionally, x-ray metrology is used for determining an atomic scale structure of materials. In addition, it is also useful for determine secondary structure of nanometer scale such as segregation of met-allic alloys, nanoparticles, nanopores, and so on. The former is so called small angle x-ray scattering (SAXS). When x-rays irradiate surface of substrate on which periodic patterns are fabricated, diffraction peaks originated by the structure can be observed. We have already confirmed that the structure of surface gratings with having hundred-nanometer pitch could be characterized by this technique [2]. We have observed a number of diffraction peaks and every peak has a characteristic feature which is reflected the grating structures, such as pitch, line width, height, sidewall angles, rounding of the edges. In addition, x-ray diffraction also has sensitivity for the distribution of the pitch, line width, and height of the grating [3].

X-ray diffraction is applicable not only for grating structure but also for surface two-dimensional patterned structure formed by nanometer size dots. It can characterize the packing conformation, such as hexagonal closed packing, simple square packing, deformation of those packing structures, and so on, from the diffraction patterns. In addition, the average shape (radius, height, sidewall angle, deformation from the circle, etc.) of the dots and their distributions can also be determined. Non-destructive characterization is possible and no sample pre-preparation is needed for x-ray method. We will present how we can analyze the above structural parameters from the x-ray diffraction patterns.

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8166-57, Session 17

Fabrication and recording analysis of bit-patterned media generated by rotary stage electron-beam lithography

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The hard disk drive industry faces a number of challenges as area recording densities continue to push towards 1 Tbit/in ^{2}. Beyond this point, new recording approaches are needed to overcome limitations encountered in the continuous granular perpendicular

magnetic recording (PMR) media used in today's drives. Bit patterned media (BPM) stands as one of the most promising technologies for overcoming such limitations at ultra-high recording density. However, the low defect densities and tight fabrication tolerances of 5-10% sigma required by BPM present a number of challenges on the road to commercialization. Above densities of 1 Tbit/in ^{2}, lithographic features sizes scale below 10nm, making pattern generation and pattern transfer difficult with conventional techniques. Many believe the only viable way to achieve such bit patterns in mass production is via high throughput nanoimprint lithography using templates generated by highly accurate electron beam mastering tools coupled with self-assembled nanostructures. In this work, we experimentally demonstrate the merits of rotary stage electron beam mastering by directly writing circumferential bit and servo patterns on 2.5" CoCrPt PMR media starting at a density of 366 Gbit/in ^{2}. The fully circular staggered tracks were written with bit patterns having 42nm downtrack pitch and 42-84nm crosstrack pitch using an EBR-401 electron beam writer developed by Pioneer Corporation. During formatting, servo patterns were integrated with the bit arrays to generate 256 sectors for spin stand testing. Throughout this talk, we will discuss the achievable tolerances of such a system as well as the effects of direct pattern transfer into the CoCrPt media layer using highly selective C/SiN $_x$ mask structures and a novel Al protective layer designed for use with etching methods such as reactive ion etching (RIE) and ion milling. Good magnetic pattern fidelity is confirmed through post process recording analysis performed on a spin stand as well as a contact recording tester designed to scan a commercial recording head in contact with the media for writing and reading. Using the results of the above analysis, we will discuss the limitations of the aforementioned processes and experimentally demonstrate methods for moving forward to densities as high as 4 Tbit/in ^{2}. The discussion will include evidence of nanoparticle guided-self assembly processes for pattern generation, as well as advanced methanol based reactive ion etching processes for direct pattern transfer of sub-10nm features into various magnetic alloys.

8166-58, Session 17

30-nm full-field quartz template replicated from Si master for FLASH active layer NIL

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To alleviate the cost burden in template fabrication the template replication is an inevitable approach in nanoimprint lithography (NIL). Upto now the master template which is used as a mother pattern for replication is made by quartz using the e beam lithography and subsequent dry etching. However the critical dimension required for CMOS application is getting smaller and NIL template uses 1x pattern because it is contact lithography. The quartz master template suffers from defining such fine pattern as sub-20nm line and space pattern in full field area. In this study we propose the Si master template to overcome the hurdle. In case of using Si wafer for patterning we can take variety of patterning tools not only the e beam lithography but also the ArF multiple patterning, interference lithography, directed self-assembly and so on. In etching process it can also take advantage in wider material selection range in pattern layer and hardmask. And it is possible to introduce the etch stop layer. Thus the Si master template has its strong point in fine patterning in full field area with low cost.

In this study the Si master template was fabricated by using the ArF immersion lithography and the master pattern was replicated to quartz template in a conventional UV-NIL tool. By using the replicated resist pattern, quartz template was dry-etched to make the working template. The template quality was verified with imprinted pattern of the replica template.

The poly Si pattern layer with Si oxide etch-stop layer was deposited on Si wafer to make the Si master template. In this study we used ArF lithography and subsequent dry etching for 30 nm grating pattern in full field area. Etch depth of poly Si was 60nm and sidewall angle was larger than 85 degree. In case of quartz blank template for replication, we introduced a hardmask layer which has both high selectivity to quartz and high UV transmittance for UV exposure in replication process. We used Imprio-100 and Imprio-300 from Molecular Imprints Inc. to replicate the master pattern. These tools are not a dedicated replication tool but a usual UV-NIL tool. It is another strong point of our replication approach. The replicated pattern showed residual layer thickness (RLT) uniformity as following; average RLT=21.8 nm, 3sigma=3.6 nm, range=3.3 nm with pattern height of 53.2nm. The pattern quality and defectivity of the replicated template was measured indirectly from imprinted pattern. It was found that CD uniformity and pattern quality of the replicated quartz template after dry etching showed strong dependency on RLT uniformity.

8166-59, Session 18

Dry etching performance of novel EUV blanks

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Mask defectivity is often highlighted as one of the barriers to a manufacturable EUV solution. As EUV lithography matures, other components of mask making also emerge as key focus areas in the industry: film variability, feature profile and critical dimension (CD) control. Mask materials and specifications continue to evolve to meet the unique challenges of EUV lithography, creating the need for etch capabilities that can keep pace with the latest developments. The Ta-based absorber, Ru capping layer, and Mo/Si multilayer films which have become the industry standard for EUV mask blanks already present unique challenges beyond those typically seen with optical masks. These challenges include high etch selectivity to the Ru capping layer, film uniformity and smoothness, and stringent defectivity requirements. Along with the ever-present need for improved CD performance, these factors are important constraints in developing a successful mask etch process for whichever mask blank is utilized in EUV production.

In this study, the performance of a new EUV mask etch system will be evaluated using a variety of mask blanks. Specifically, an industry standard EUV blank will be compared to new blanks with different film stack configurations to determine the relative performance of each blank type. Etch contributions to CD bias, CDU, linearity, selectivity, film uniformity, LER, profile quality and defectivity will be characterized to determine tool performance. Film changes will be characterized with AFM and reflectivity measurements. Etching of the Mo/Si multilayer is important for two EUV applications: alternating phase shift masks (PSM) and dark frame open. The new system will also be used to demonstrate capability in this emerging area and the performance assessed in the same manner as the new blank types. A comprehensive summary of the etch performance of various EUV films and the readiness for manufacturing applications will be provided.

8166-60, Session 18

Development of sub-20-nano patterning technology using new hard mask in NIL

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NIL(nano-imprint lithography) is expected to be one of the leading candidates for the next generation lithography. This technology has

many advantages such as low cost, high resolution, simple process. Among the many issues for realizing the NIL, obtaining the stamp with fine pattern resolution for sub 20-nm becomes more important.

For the fabrication of a stamp structure, the plasma etching characteristics of the hard mask layer need to be investigated. As a result, oxygen-based plasma used for transferring sub 20-nm patterns is not compatible with the conventional mask. In this paper, we take new hard mask to obtain the fine pattern resolution for 20nm and beyond. By optimizing the material, its thicknesses, and the etching process, we have achieved sub 20-nm patterning by using the new hard mask materials to approve its selectivity of hard mask to PR.

8166-61, Session 18

The impact of a thinner binary mask absober on 22 nm and beyond mask inspectability and defect sensitivity

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A new thinner absorber version of the OMOG binary blank has been successfully developed for use for the 22 nm and 20 nm logic node masks and beyond. Many benefits have been realized through the use of thinner OMOG including improved film stress, flatness, image placement and cleaning durability compared to the standard thickness OMOG. In addition, it was demonstrated that use of 100 nm thick PCAR and NCAR e-beam resists in conjunction with the thin OMOG blank could meet the CD uniformity and minimum feature size requirements for 22 nm and 20 nm node critical level masks.

Concurrent with the development of processes and methods for the successful build of 20 nm and 22 nm masks on thin OMOG, was an in-depth evaluation to determine the impact of this thinner film on mask inspection. Differences in attenuator reflectivity for thin-OMOG as compared to standard OMOG posed new challenges relative to a loss of defect sensitivity at the same inspection conditions (calibration, sensitivity). It is surmised that the reduction in sensitivity is due to a lower reflected light contrast on thin-OMOG. This characteristic was noted for both 257 nm and 193 nm inspection wavelengths. The reduction in defect sensitivity manifests itself more on edge and isolated defects than on critical dimension defects.

In addition to the reduction in sensitivity, an unexpected phase interference was noted at the image edge for Standard OMOG, but not for Thin OMOG. This interference, or undershoot is due in part to the low difference in reflectivity and phase between the quartz and the attenuator on the Standard OMOG substrate. This difference is more than five times greater for the Thin OMOG attenuator. This paper explores how that lack of undershoot contributes to the reduced sensitivity with Thin OMOG.

Despite the apparent loss of defect sensitivity, the reduction in residual image quality non-uniformities with the thin OMOG absorber resulted in an improvement in mask inspectability. This reduction in non-uniformities led to less modeling errors in the mask inspection database and as such, lower residual noise during the inspection - primarily in the reflected light difference image. This lower level of residual noise enabled optimization of inspection conditions to achieve similar, or better sensitivity compared to standard OMOG without an increase in nuisance detections.

The primary focus of this paper will be on the characterization of thin OMOG relative to the interaction between attenuator reflectivity, image quality, database modeling and tool calibrations as they relate to mask inspectability and defect sensitivity. This paper will also address the changes required to compensate for the loss of sensitivity induced by the introduction of the thin OMOG absorber.

8166-62, Session 19

Pattern placement error due to resist charging effect at 50kV e-beam writer: mechanism and its correction

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In e-beam lithography, electron exposure results in charging of the insulating resist. The deposited charge in resist layer generates electric field and it deflects the path of electron beam. Many previous studies have reported the effect of resist charging on the pattern displacement error but they have focused on the charging effect in low energy e-beam lithography. Although a few papers have reported recently the resist charging effect in 50kV e-beam lithography, they also have the limitation when understanding the charging effect in photomask for mass production. Here, we present the charging effect in FEP-171 resist at e-beam writer with accelerating voltage of 50kV and its effect on pattern placement error of photomask. Based on simulation and experiment, we propose the model to describe resist charging effect in photomask and the pattern placement error. Furthermore, we present the pattern qualities such as line edge roughness and uniformity of pattern size also can be affected by resist charging effect.

8166-63, Session 19

Enhancement of global CD correction in EB mask writer EBM-8000

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We report our development of fogging effect correction method aimed for EBM-8000, our newest series of EB mask writer for mask production of 22nm half-pitch generation and for mask development of 16nm half-pitch generation. Our EBM series has been employing the FEC method to reduce irradiated dose to compensate for excessive dose brought by the fogging effect. Conventionally, a simplified equation based on global pattern density has been used for FEC calculation since the calculation must be completed preceding to drawing within a limited calculation time.

We have refined our method of FEC and developed the new software ‘iKBR’ for EBM-8000. Major improvement in iKBR is the more precise FEC calculation that takes account of proximity effect correction (PEC) and loading effect correction (LEC).

Recently, a new method for FEC has been proposed which takes into account of PEC to greatly reduce calculation errors [1], and we have applied this method to iKBR. According to the method, the amount of dose reduction for FEC is calculated from the distribution of imaginary dose irradiated on a photomask if FEC were not applied. We have equipped iKBR with the function of PEC dose estimation to calculate dose distribution. As has been proposed [1], we tried reducing the calculation time for PEC dose in exchange for calculation accuracy by using mesh size as coarse as FEC error allows. We investigated the FEC error in several patterns using coarse meshes for PEC dose calculation. We found that the mesh size of 10 microns brings FEC error of 0.5 nm at most, even in such worst case that the error in estimated PEC dose for each mesh are not compensated by each other.

We have modified the formula of the above method so that FEC also takes account of LEC. The LEC function for EBM series is realized by modulating PEC parameters so that PEC controls the pattern size to have the same amount of deviation from the pattern design regardless of local pattern density to compensate for the Cr-loading effect. Our new equation calculates amount of dose reduction for FEC, taking account of the dose level at the pattern edge adjusted by PEC.

Drawing experiment was carried out to survey the applicability of the threshold dose model that our method bases. We surveyed CD

variations for dose modulation for chips with and without background patterns. We found that threshold dose model and our FEC method is basically applicable except that fogging effect not only yields to excessive dose but also increases dose latitude.

As a result, we obtained a method for global CD correction that is theoretically flawless, i.e., corrections of PEC, LEC and FEC are accordant to each other as long as the dose threshold model holds. We consider theoretical accuracy and consistency of our method is useful for GCD correction where usually ambiguous CD variations need to be corrected.

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8166-64, Session 21

Efficient large-volume data preparation for electron-beam lithography for sub-45-nm node

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Electron Beam (e-beam) lithography is used in the IC manufacturing industry to sustain optical lithography for prototyping applications and low volume manufacturing. It is also applied at a larger scale in mask manufacturing. As semiconductor technologies are now moving towards the 32nm node and beyond, the specifications in terms of resolution and process control become tighter for direct write on silicon and mask writing. The dose modulation, the method used to apply standard proximity effect corrections in current e-beam lithography, shows difficulties to provide the required process window for patterning structures designed below CDs of 45nm.[1] A new correction approach was developed to improve the process window of e-beam lithography and push its resolution at least one generation further using the same exposure tool.[2] An efficient combination of dose and geometry modulation is implemented in the commercial data preparation software, called Inscale, from Aselta Nanographics.

The developed data preparation software was tested to process a large variety of data and applications, such as logic or DRAM designs at 32nm node and complementary e-beam exposures. The test exposures were performed at Fraunhofer CNT using a Vistec SB3050DW tool dedicated to the 45nm node. The test patterns were examined with an Applied Materials Verity 4i CD-SEM.

In simulations, which comparing the efficiency of the different correction strategies on a metal 1 level of a 32nm node design with a pitch of 67nm, the combination of dose and geometry modulation allows printing the memory cell with higher quality compared to no correction and standard dose only modulation. The comparison of observed pattern exposures according to the different corrections shows that the dose-geometry modulation corrected pattern has a higher exposure quality with significant gains in CD uniformity, reduction of line-end shortening and corner rounding. An improvement in energy latitude is also realized in the dose-geometry modulation corrected pattern.[3]

In this paper, we will present the requirements for data preparation in e-beam lithography for practical applications with large volume data, especially with sub-45nm nodes. The application of complementary exposures for sub-40nm designs using Inscale will be discussed.

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8166-65, Session 21

eMET POC: realization of a proof-of-concept 50-keV electron multibeam mask exposure tool

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Based on a massively parallel beam writing strategy (Bacus 2010) a mask writer proof-of-concept tool will be realized in 2011. The eMET (electron Mask Exposure Tool) POC column is designed to provide ca. 262-thousand (512 x 512) programmable beams of 50 keV energy and 20 nm or 10 nm beam size. The total beam current through the column is up to 1 µA. The eMET POC is equipped with a laser-interferometer controlled stage for exposure of one cm2 test pattern fields on 6” mask blanks. First eMET POC exposure results will be presented.

8166-66, Session 21

CD error budget analysis of CP exposure

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CP exposure technology has many advantages. Originally, the technology is developed as a throughput improvement technology of EB writer because it can reduce the number of the shots. The technology can also be used together with multi column cell (MCC) technology which is another promising throughput enhancement technology. CP exposure technology also has an advantage for resolution capability because the CP projection simply uses only one object plane and almost is free from the blur which comes from the illumination part of optical system, while the VSB uses two object planes.

Another advantage of the CP technology, namely, the CD stability is reported. With the CP technology, for writing the pattern of specific size, the pattern can be exposed with an appropriate fixed width opening of the CP mask. As a result, the higher CD stability is observed because the beam size is completely defined by the size of CP openings, and the CD only depends on electron gun capability.

In the MCC proof of concept (POC) tool, we evaluate the fidelity and stability of CP technology with the support by a CP mask vendor. We prepare the CP mask of simple line or hole with additional structure. On the CP mask, a set of patterns for uniformity evaluation is also distributed in whole of the CP mask and measured by CD-SEM.

Comparison of exposed pattern size by the CP and the CP mask openings sizes measured beforehand clarifies the projection fidelity from the CP mask to the substrate. It provides the valuable basic data to estimate the error budget of CD for the CP exposure tool and the CP mask.

Each CC of MCC tool uses individual CP openings set. In case of MCC-POC tool, the CP mask for 4CC is made of a 200mm SOI wafer and the CP mask pattern sets are repeated in 4 times in 75mm by 75mm pitch which is the same as the distance of CCs. If there is an unfavorable CD error distribution on the CP mask, it is necessary to correct the size of openings or to apply some counter measure for achieving the necessary CD uniformity level.

We report that the CP mask provides sufficient uniformity for multi column system, and in case of using a CP mask with inferior uniformity for some reason, the non-uniformity can be corrected by a simple dosage control.

We will report other topics, for example, the effort for an increase of the current density. CP mask of 2 micrometer membrane can endure even

in the case of the CP pattern which has large region for shading the e-beam and very narrow heat sink routes for 300A/cm2 beam.

8166-67, Session 21

Mask aspects of EUVL imaging at 27nm and below

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EUVL requires the use of reflective optics including a reflective mask. The mask consists of an absorber layer pattern on top of a reflecting multilayer, tuned for 13.53 nm. The EUVL mask is a complex optical element with many parameters contributing the final wafer image quality. Specifically, the oblique incidence of light, in combination with the small ratio of wavelength to mask topography, causes a number of effects which are unique to EUV, such as an HV CD offset. These so-called shadowing effects can be corrected by means of OPC, but also need to be considered in the mask stack design.

In this paper we will present an overview of the mask contributors to imaging performance at the 27 nm node and below, such as CD uniformity, multilayer and absorber stack composition, thickness and reflectivity. We will consider basic OPC and resulting MEEF and contrast. These parameters will be reviewed in the context of real-life scanner parameters both for the NXE:3100 and NXE:3300 system configurations.

The predictions will be compared to exposure results on NXE:3100 tools, with NA=0.25 for different masks. Using this comparison we will extrapolate the predictions to NXE:3300, with NA=0.33.

Based on the lithographic investigation, expected requirements for EUV mask parameters will be proposed for 22 nm node EUV lithography and below, to provide guidance for mask manufacturers to support the introduction of EUV High Volume Manufacturing.

8166-68, Session 22

Defectivity status for jet and flash imprint lithography

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Nanoimprint lithography continues to make progress towards meeting high volume manufacturing requirements for semiconductor devices. Demonstrations have shown that it meets, or is close to meeting, 22nm node requirements for resolution, critical dimension uniformity, line width roughness, and template pattern placement. Even overlay, once considered a major roadblock, has improved to within a factor of two of the requirement for 22nm flash specified in the International Technology Roadmap for Semiconductors. However, defectivity is still identified as a leading technical challenge to the implementation of nanoimprint lithography in high volume manufacturing. The lack of confidence in nanoimprint's ability to meet defect requirements originates in part from the industry's past experiences with 1X lithography and the shortage in end-user generated defect data. SEMATECH has therefore initiated a defect assessment aimed at addressing these concerns. The goal is to determine whether nanoimprint is capable of meeting semiconductor industry defect requirements.

Several cycles of learning have been completed in SEMATECH's defect assessment. Proof of concept for process random defectivity of < 0.1 def/cm2 has been demonstrated using a high quality, large field, 120nm half-pitch template. Template and particle defects were removed during the analysis to demonstrate process capability under ideal conditions. Template defectivity has also improved as shown with a pre-production grade template at 80nm pitch. Additional experiments are being conducted to demonstrate defectivity on feature sizes down to 22nm. Results from SEMATECH's nanoimprint defect assessment, in conjunction with recent industry achievements, will be used to provide a comprehensive evaluation of Jet and Flash Imprint Lithography defectivity. The latest tools, templates, and processes will be discussed, and requirements for a low defect nanoimprint process will be explored.

8166-69, Session 22

Imprint lithography template technology for bit patterned media (BPM)

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Magnetic recording bit patterned media has emerged as a promising technology to deliver thermally stable magnetic storage at densities beyond 1Tb/in2. Insertion of this technology into the manufacturing of hard disk drives will require the introduction of nanoimprint lithography and other nanofabrication processes for the first time in the fabrication of magnetic recording media. In this work, we focus on nanoimprint and nanofabrication challenges that are being overcome in order to produce patterned media on a massive scale.

Patterned media has created the need for new tools and processes. Generation of patterned media templates has required some new tools, such as an advanced rotary e-beam lithography tool, a new template replication tool, and a high-throughput media imprinting tool. A new process that has attracted wide attention is the integration of block copolymer directed self-assembly into the creation of the master template for nanoimprint. Our integration is focused on the generation of a chemical contrast pattern on the substrate which guides the alignment of di-block copolymers. I will discuss the nexus between a wise choice of materials and process conditions which facilitates the formation of directed block copolymers patterns on the template. Incidentally, these large area, self-assembled structures are helpful for applications outside magnetic recording.

Most of the work on directed self assembly for patterned media applications has, until recently, concentrated on the formation of circular dot patterns in a hexagonal close packed lattice. However, interactions between the write head and media favor a bit aspect ratio (BAR) greater than one. This design constraint has motivated new approaches for using self-assembly to create suitable high-BAR master patterns and has implications for the template fabrication process, which will also be covered.

8166-70, Session 22

Mask replication using jet and flash imprint lithography

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The Jet and Flash Imprint Lithography (J-FILTM) process uses drop dispensing of UV curable resists to assist high resolution patterning for subsequent dry etch pattern transfer. The technology is actively being used to develop solutions for memory markets including Flash memory and patterned media for hard disk drives. It is anticipated that the lifetime of a single template (for patterned media) or mask

(for semiconductor) will be on the order of 104 - 105 imprints. This suggests that tens of thousands of templates/masks will be required to satisfy the needs of a manufacturing environment. Electron-beam patterning is too slow to feasibly deliver these volumes, but instead can provide a high quality “master” mask which can be replicated many times with an imprint lithography tool.

For the case of the semiconductor market, a variety of feature types must be resolved, although for most memory applications, the dominant feature set consists of 1:1 line/space patterns for critical front-end layers, particularly Flash. In the case of Flash memory, the most aggressive production designs are now pushing to half pitches of 25nm. For such designs, mask critical dimension uniformity (CDU) must be less than 10 percent of the minimum device half pitch, mask image placement must be below 5nm and defectivity of the mask is required to be less than 1 defect/cm2. In this paper, we review the development of the mask form factor, the imprint tool, the imprint process and pattern transfer specifically for semiconductor replica masks.

The requirements needed for semiconductors dictate the need for a well defined form factor for both master and replica masks which is also compatible with the existing mask infrastructure established for the 6025 semi standard, 6” x 6” x 0.25” photomasks. Complying with this standard provides the necessary tooling needed for mask fabrication processes, cleaning, metrology, and inspection. The replica form factor has additional features specific to imprinting such as a pre-patterned mesa. A schematic of the 6025 replication process is shown in Figure 1. A PerfectaTM MR5000 mask replication tool has been developed specifically to pattern replica masks from an e-beam written master. The system specifications include a throughput of four replicas per hour with an added image placement component of 5nm, 3sigma and a critical dimension uniformity error of less than 1nm, 3sigma.

A key component of the replication process is image placement. Image placement errors were evaluated by measuring both a master mask and an imprinted mask and comparing the image placement vectors. Measurements were made on a Leica IPRO1. Gauge error on this tool is estimated at 3-4nm. The added image placement error vector plot is shown in Figure 2. The added contributions to image placement are 5.12nm in x and 3.56nm in y. It should be noted that modeling indicates that the error contribution from compressing the mask is not more than 0.07nm per ppm of applied magnification correction (See Figure 3.). Additional experiments and modeling will be required to identify the key contributors and drive image placement down to acceptable levels.

8166-71, Session 23

Statistical analysis of the effects of mask process on OPC errors

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In the process of optical proximity correction (OPC), the mask patterns are corrected comparing their wafer images with the desired target patterns. However, the final mask patterns designed by OPC are not the same as the patterns printed on the real mask. This is because the processes of mask production such as e-beam scatterings and etching cannot perfectly reproduce the input pattern data. Consequently, this difference results in the distortion of the information in the matching between wafer data and mask patterns in OPC, yielding errors in the correction of the mask patterns.

To overcome such an obstacle and thus to enhance the whole lithography process, we study the contribution of mask errors to OPC and to the total lithography process by using detailed budget analysis based on the statistical correlations. That is, we make a standard scheme of mask correction after OPC, according to the pattern properties and to the types of mask processes.

To do this, we prepare a set of standard OPC patterns that can reflect the expected mask errors most properly. For this, the patterns are chosen to satisfy two conditions. First, the errors from lithography process in printing those patterns should be apparent. That is, we make the mask error the only part contributing the final pattern error as far as possible. Secondly, the patterns need to have categorized shapes and distributions such that the resulting mask errors are classified properly referring to the types of the patterns. Here, the properties from varying mask processes such as mask stacks are considered as well as the geometrical properties such as bias, curvature and densities. This is important in probing the differences in error distributions for the change of mask process during the production of the chip of same design and lithography process.

Once the standard patterns have been setup as input patterns, we perform a real mask process on them and obtain output patterns printed on the mask, which are different from the input patterns. Then, we perform a rigorous lithography simulation on both the original input patterns and on the deformed output patterns so that the error between two resulting wafer patterns represents the mask error portion contributing to the total process error.

Here, the obtained mask errors vary according to the types of standard test patterns and thus contribute differently to the total error. Moreover, the relationship between mask errors and the types of input patterns is not one-to-one correspondences, but complicated cross-connections. Therefore, we represent the two relationships, between mask errors and total error and between mask errors and input pattern types, by correlation matrices and perform matrix multiplication to get the proper correlation between pattern types and total error.

As a result, we obtain the contribution of each pattern type to the final process error and thus can determine the forms and weight of the proximity functions in the mask process model, yielding efficient and enhanced corrections of the mask patterns.

In addition, to apply above result from the standard pattern to the real OPC patterns, we analyze the statistical significance between standard patterns and real patterns so that the degrees of corrections can be extended to the real patterns. Especially, for the complicated OPC patterns from the inverse lithography technology (ILT), the setup of standard patterns and the analysis of significance are more critical and thus the budget analysis is performed separately in more meticulous manner.

To summarize, we develop a method of enhanced mask error analysis in the aid of well-defined categories of test patterns and of statistical correlation methods. Moreover, using the analyzed error budget, we classify those errors according to the application methods to OPC, by which the final OPC patterns can be modified minimizing the mask error factor in the lithography process.

8166-72, Session 23

Exploring the impact of mask making constraints on double-patterning design rules

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In order to achieve an economical design-to-mask (DTM) development cycle in the low k1 domain, designers, lithographers, and mask makers are moving away from many sequentially isolated developmental activities onto one collaborative environment managed by a computational lithography platform that integrates their respective ecosystems. 1,2 A successful development cycle used to be achievable by designers providing designs to lithographers, who then provided RET/OPC solutions to realize designs. Once k1 fell below a certain level, the lithographers could not provide solutions to realize some critical designs, which then required feedback to designers for further redesigns that then needed further lithographic evaluation cycles. So collaboration and automations between lithographers and designers became necessary to reduce feedback loops and development cycle time. RET and design solutions also were impacted by mask making, and so mask maker’s feedback on MRC and other constraints needed to be integrated for all three groups to achieve an economical DTM.

As many lithographers attempt to print sub-80 nm pitches with 193 nm wavelength, it becomes necessary to use double patterning to achieve feature resolution. With the effective pitch doubling on each split layer, there could be significant increased design rule freedom for certain complex design situations. Using an integrated computational lithographic platform, one could find design space sweet spots that could further achieve optimal lithographic performance. In this paper, the optimization of design rules for double pattern designs (~60 nm pitch) will be explored with the mask maker's perspective. The experiment to be presented starts with a 2x nm design set of clips. Each set of clips will undergo size/width/space/pitch variations to generate a design space, and then each design space will undergo SMO with an ILT engine using various mask MRC's and manhattan segmentations. The lithographic results will be analyzed with respect to MRC and manhattan segmentation to show their impact on design space and mask solutions.

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8166-73, Session 23

Freeform source optimization for improving litho-performance of warm spots

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Source and mask optimization (SMO) [1, 2, 3, 4] is becoming a key enabler for extending ArF lithography to advanced technology node [5, 6]. Freeform source (FFS) possesses higher degree of freedom in source optimization for DRAM chip maker to find out the maximum common process window between array and periphery patterns. In this paper we investigated a flow to use freeform source only in optimization to improve observed "warm spots" in an already OPC decorated design area.

Since the goal is to improve the performance of an already existing mask patterns, the only free variables in optimization metric are the source itself and the relative weighting of the "warm spots" locations. The investigation includes two "types" of freeform sources, the traditional pixilated array freeform and Brion's Freeform Plus with a segmented free form pole shape.

The proposed flow was validated with a 50nm node DRAM case. Four representative clips in the case were selected; one cell clip was array used for anchoring the threshold and the other three clips were from the periphery that exhibited "warm spots" for optimization by FFS. From this validation, the simulation results with resist model data input were observed that the "Source Optimization Only" flow successfully enlarged the DOF of these "warm spots" by 15 ~ 46 % respectively without decreasing NILS values. Therefore, this flow indeed improved the warm spots without the need for re-taping out a new mask.

Keywords: source mask optimization, diffractive optical element (DOE), co-optimization, cost function, freeform source, standard DOE

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8166-74, Session 23

A critical impact of model-based SRAF on multiple patterning

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This paper presents a critical impact of sub resolution assist feature (SRAF) on multiple patterning (MP). As many articles have described, the limitation of optical lithography can potentially be extended below 20 nm node. Design rule restriction engages on this extension, at the same time, contrast enhancement technique such as source mask optimization (SMO) with model based SRAF is also key resolution enhancement technique (RET) of this extension. In addition, one of the significant transformations on patterning below the 28 nm node is to implement MP, which is caused by the k1 factor lower than the resolution limit (0.25). Aside from the process complexity, there are several types of issues with MP. One of the examples is the more frequent occurrence of isolated pattern caused by pattern splitting, which has intrinsically negative impact on the depth of focus margin. Also, each patterning step may have a slightly different CD-distribution, resulting in an increase of the overall CD variation. One reason for this is that, if we implement SMO on each MP layer separately, the source shapes will not be identical in each lithography steps. Process margin strongly depends on the source shape; therefore, the MP may suffer from the difference of CD uniformity between each lithography steps.

The increased of concurrency of isolated pattern, however, gives lithographers more physical space on the mask to add SRAF than is the case for single patterning. Therefore, it can act as a new knob to improve lithographic process capability of MP, in other words, SRAF modification could be a key factor to overcome MP specific issue. On the other hand, SRAF increases the complexity of the mask pattern significantly, so a careful consideration is needed on how one implements the SRAF placement. This complexity has been well discussed in past investigations; however, little discussion has been made for the case of MP.

In this paper, we explain the contribution of SRAF on the overall CD-distribution. SRAM and logic circuit were used in this investigation, which has several pitch combination involving the pitch equivalent to the 28-20 nm node. Both SMO and model based SRAF placements were performed by Tachyon-SMO . At first, we define optimum scenario of patterning method as a function of pattern pitch. For example, the limitation of single- or double-patterning is defined. Secondly, quantitative investigation is performed on the MP specific issues. Thirdly, the benefit of different SRAF placement options is investigated, while taking into account mask-pattern size restrictions. Especially, we focus on the difference between free-form and rectangular-shaped SRAF, from view point of pattern complexity. Finally, we conclude the total benefit of SRAF on MP-related CD uniformity issue, from process capability as well as pattern complexity perspective.

8166-75, Session 24

Si stencil masks for organic thin film transistor fabrication

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Organic electronics are gaining increasing interest and attention in electronic device fabrication due to cost advantages and low process manufacturing temperatures, which allow the use of mechanically-flexible polymeric substrates. Different patterning techniques for Organic Thin Film Transistors (OTFT) with sub µm channel length are currently under investigation like inkjet-printing, nanoimprint, optical- and e-beam lithography.

A new approach for OTFT fabrication is the device patterning with stencil lithography. This high resolution shadow mask technique allows the parallel patterning of sub µm features without the use of photosensitive resists or chemical solvents, which could lead to a degradation of the sensitive organic semiconductor layer. At first the device pattern is etched into a thin membrane, creating design-specific sub µm apertures. Subsequent this membrane mask is aligned and clamped to the substrate and material is deposited through the stencil apertures forming the desired device pattern onto the substrate. By repeating this sequence with different deposition materials a classical top contact TFT architecture with a gate electrode, gate dielectric, organic semiconductor and source drain contacts can be achieved.

The key component of the stencil lithography is the stencil mask, which mainly determines the pattern properties e.g. minimal feature size, line edge roughness and therefore the final device performance. Different stencil membrane mask materials e.g. metals, polymers, Si3N4 can be used but suffer from patterning and stability limitations. We focused our work on monocrystalline Si which has distinguished advantages like mechanical stability, lower defectivity, excellent cleanability and nanopatterning capability.

For OTFT fabrication a new Si stencil mask process flow was developed by applying a wafer flow process (WFP) scheme. Thus all critical patterning steps are carried out on a massive wafer substrate and the membrane etching is the final step of the flow and therefore standard semiconductor manufacturing equipment and processes can be applied.

Base substrate is a 150mm SOI- (Silicon on Insulator) wafer. The initial SOI thickness determines the final membrane thickness and the buried oxide layer acts as an etch stop for the stencil etching from the wafer front- and membrane etching from the wafer-backside.

At first the stencil pattern is written in a CAR (Chemically Amplified Resist) by e-beam direct writing and transferred into the SOI layer with a DRIE-(Deep Reactive Ion Etching) process. Subsequently, a dielectrica layer is deposited onto the wafer backside and nine 20mm x 20mm2 membrane windows are patterned. These Si membrane windows are etched in a wet-chemical KOH-solution down to the buried oxide layer. Afterwards, the buried oxide layer is removed and the 150mm SOI wafer is sawn into nine single Si stencil masks with 30mm x 30mm2 outer dimensions. Finally, the stencil masks are cleaned and inspected.

By device patterning with these Si stencil masks single OTFT with sub µm channel length were fabricated with 100x higher switching speeds due to the excellent Si stencil mask stability, resolution and line edge roughness compared to OTFT devices which have been patterned with polymer stencil masks. In addition, a complete stencil mask set consisting of 4 different masks for the fabrication of an organic 6 bit DAC (Digital to Analog Converter) was designed and realized. The achieved electrical results for that 6 bit organic DAC marked a record in speed and compactness to state-of-the-art DAC. These considerable improvements result from an OTFT fabrication process based on Si stencil masks that provide submicron channel length capability and excellent transistor matching.

We will present and discuss in detail our stencil mask process with respect to minimal feature size, line edge roughness and low defects.

8166-76, Session 24

Bottlenecks in data preparation flow for multibeam direct write

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Technical problems with shrinking process node for semiconductor manufacturing has generated considerable interest in the use of multiple beams as an advanced manufacturing technique in the context of direct write to mask / wafer. This paper examines the data preparation bottlenecks associated with this process. The various steps in the data preparation flow are described. Particular attention is paid to the large increase in data volume and the associated issues in processing power, transfer speed, storage requirements, and overall turn-around-time. Further, the use of commercial graphics processing units (GPUs) is examined as a possible solution to some of these issues and results of tests conducted as part of the MAGIC (MAskless lithoGraphy for IC manufacturing) initiative are summarized.

8166-82, Session 27

Simulation-based mask defect printability verification and disposition, part II

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We have reported the first part of the work in 2009 BACUS meeting [1], using primarily SEM mask defect images as input. This paper is the extension of that work using mask optical inspection images with a new image process algorithm.

Simulation has been widely used in overall lithography process, called computational lithography, as an effective way for cost and time reduction. As the industry moves towards 45nm and 32nm technology nodes in production, the mask inspection, with increased sensitivity and shrinking critical defect size, catches more and more nuisance and false defects. Increased defect counts pose great challenges in the post inspection defect classification and disposition: which defect is real defect, and among the real defects, which defect should be repaired and how to verify the post-repair defects. In this paper, we report simulation mask defect printability check and disposition results extending beyond SEM mask defect images [1] into optical inspection mask defects images to demonstrate cost and time reduction by simulation in mask defect management area.

A new algorithm has been developed in the software tool to convert optical inspection mask defect images into “pseudo-defect” polygons in GDS format. Then, the converted defect polygons were filled with the correct tone to form mask patterns and were merged back into the original design GDS. With lithography process model, the resist contour of area of interest (AOI-the area surrounding a mask defect) can be simulated. If such complicated model is not available, a simple optical model can be used to get aerial image intensity of AOI. With build-in contour analysis functions, the software can easily compare the contour (or intensity) differences between real mask (with defect) and ideal mask (without defect). With user provided judging criteria, software can be easily disposition the defect based on contour comparison.

The software has been tested and adapted for production use. We will present some accuracy test results against AIMS tool in defect printability check.

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8166-83, Session 27

EUV multilayer defect compensation (MDC) by absorber pattern modification: from theory to wafer validation

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According to the ITRS roadmap, mask defects are among the top technical challenges to introduce extreme ultraviolet (EUV) lithography into production. Making a multilayer defect-free extreme ultraviolet (EUV) blank is not possible today, and is unlikely to happen in the next few years. This means that EUV must work with multilayer defects present on the mask. A number of methods have been proposed in the past to deal with this problem. One of the most popular takes advantage of degrees of freedom in where the pattern is located on a blank, shifting it so that multilayer defects are covered by absorber to minimize their effects on the image. This method works if the number of multilayer defects is sufficiently small and the mask pattern has large absorber regions that may be suitably placed to cover them. It is therefore best suited to sparse, dark-field patterns. The probability that a solution exists decreases as the number of multilayer defects increases, or the density of absorber in the mask pattern decreases. Whether a solution exists for a particular blank-pattern combination depends on specific coordinates of the defects and absorbers.

The method proposed by Luminescent is to compensate effects of multilayer defects on images by modifying the absorber patterns. The effect of a multilayer defect is to distort the images of adjacent absorber patterns. Although the defect cannot be repaired, the images may be restored to their desired targets by changing the absorber patterns. This method was introduced in our paper at BACUS 2010, which described a simple pixel-based compensation algorithm using a fast multilayer model. The fast model made it possible to complete the compensation calculations in seconds, instead of days or weeks required for rigorous Finite Domain Time Difference (FDTD) simulations. Our second paper at SPIE Advanced Lithography 2011, extended the results from one-dimensional to two-dimensional patterns by formulating the problem with level-set methods.

Progress in MDC is the subject of this paper. A new compensation algorithm covers multiple image conditions, such as defocus, in addition to the nominal condition used previously. This algorithm minimizes the loss of process window caused by multilayer defects by modifying the adjacent absorber patterns. Mask repair tool constraints are also covered by the compensation optimization, so that the compensated absorber patterns can vary depending on repair tools and their physical limitations. One option is to perform compensation only by etching because etching is easier than deposition with e-beam repair tools. Another is to include pixel sizes and step sizes for etching and deposition into the compensation. A third option is to allow a different material to be deposited.

Different multilayer growth models have been used to create the defect structures that serve as input to simulation and compensation calculation. The multilayer deformation inferred from the measured top layer profile depends on which multilayer growth model is applied. An EUV mask with programmed multilayer defects is compensated, and the results are compared to experimental data from a wafer print.

8166-84, Session 27

Performance of EBeyeM for EUV mask inspection

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EB (Electron Beam) inspection system, named EBeyeM, has developed for EUV mask inspection. Design conception of the EBeyeM is to be satisfied with all items in high sensitivity, high throughput and low cost by considering EUV mask inspection tool for production. Target of the EBeyeM was decided that, for the sensitivity, defects having defect size of 20nm must be detected for 2Xnm technology node as shown in ITRS road map and, for the throughput, inspection time for particle and pattern inspection mode must be less than 0.83hours and 13hours in 100mm square, respectively. The target must be achieved by not only improving conventional inspection technique but also designing a new inspection technique. The new inspection technique has PEM (Projection Electron Microscope) technique and image acquisition technique to acquire inspection images with TDI (Time Delay Integration) sensor while continuous stage moving.

Progress of the EBeyeM is that necessary SNR (Signal to Noise Ratio) with correlation of sensitivity, defect sizes and SNR with PDM (Programmed Defect Mask) for 2Xnm EUV technology node with proto-type machine was studied and estimated, and the proto-type machine is remodeled by referring results of the feasibility study. The remodeling points are mainly two times increasing of incident electron number to TDI (Time Delay Integration) for imaging optics and two times increasing of beam current for illuminating optics and improvement of lens alignment and inspection algorithm.

This report will be reported on inspection sensitivity, throughput and stability with the remodeled EBeyeM and be discussed about correlation of the inspection sensitivity and SNR under an inspection condition satisfied with detecting defects of target.

8166-85, Session 27

NPI-7000: a mask inspection tool enabling both EUV and optical mask inspection using DUV (199-nm) laser

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The achievement of next generation process specification (22nm or 1xnm half pitch node) will become technically and physically difficult using the optical lithography technology. EUV mask lithography is a dominant candidate for the next generation lithography. However, it is forecast that the EUV technology will be practically used for production only after 2014. Thus the optical mask lithography will survive together with the EUV mask lithography for several years in the future.

We have developed a new inspection tool, NPI-7000, of DUV (199nm) optical base considering the above situation. NPI-7000 can inspect both optical masks and EUV masks below 1xnm half pitch (hp) node.

In this tool, new technologies and improvements described as follows were implemented to achieve both high sensitivity and throughput. They are adoptions of:

1) an optical system improving lighting quantities,

2) a new TDI sensor,

3) a high speed processing system,

4) a scanner mechanism with optimal mass distribution to enable high speed motion, and

5) a precise positioning system using a laser interferometer.

As for optical mask inspection time, 85 minutes are achieved by 60nm pixel resolution in this tool improved from 2 hours in 70nm pixel resolution in the conventional model (inspection area is 100mm x 100mm). These are effective also for the EUV mask inspection.

For EUV mask pattern inspection, a joint research has been executed for five years from 2006 among Selete (Semiconductor Leading Edge Technologies, Inc.), AMiT (Advanced Mask Inspection Technology, Inc.), and NFT (Nuflare Technology, Inc.). It is known that transmission images cannot be acquired for EUV masks and image contrast greatly falls below 2xnm node for reflection images. Thus in this joint research, an EUV mask pattern defect inspection tool was developed (NT-7000EUValpha), and the following technologies to improve image contrast and inspection sensitivity were implemented to the tool.

1) P-polarized illumination,

2) S-polarized and P-polarized concurrent illumination,

3) Digitizing rate changing of imaging sensor depending on the signal level, and

4) New reference image generator that concerns the 3D effect difference between coarse and fine patterns for EUV masks.

NPI-7000 is equipped these technologies, and it can inspect patterns from hp32nm node to hp1xnm node. The tool can inspect masks with both die-to-die and die-to-database modes.

In this paper, we would like to outline the new inspection tool, NPI-7000. To provide appropriate and effective super-resolution potential to the inspection tool, we have chosen optimal set of an illumination type and conditions. The tool demonstrates the most qualified defect detection sensitivity for next generation optical mask and EUV mask pattern inspection.

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8166-86, Session 27

Outlook and initial results for inspection of flare-corrected EUV masks

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Prevailing industry opinion is that EUV Lithography will enter High Volume Manufacturing (HVM) in the 2013 - 15 timeframe at the 22 and 16 nm HP nodes. One of the unique challenges for EUV masks is the use of flare correction to compensate for non-uniformities in the EUV scanner optical path. It is expected that flare correction will be implemented on the reticle as a critical dimension (CD) offset to the base pattern file structure. Furthermore, on multi-die reticles, the flare correction across the reticle field may be rendered to normally identical die in such a way as to cause challenges for traditional die-to-die inspection.

Collaborating with a leading memory chip supplier, in this work we will explore the impact of flare correction on various aspects of EUV mask inspection. We will consider multiple use cases including initial pattern inspection, outgoing quality inspection (OQC), fab incoming quality inspection (IQC) and re-qualification of the mask. We will explore the use of a commercially -available 193 nm reticle inspector for each of these use cases, examining the optimum inspection strategy for each considering such factors as defect sensitivity, time-to-results and cost-per-inspection. We will also gather empirical data using suitable test reticles to validate the strategies and approaches for inspecting flare-corrected EUV masks.

A secondary aim of this work is to evaluate the impact of flare correction on mask inspection prep and file size, with various mask data formats. Flare correction of EUV masks can significantly increase the figure count and therefore the file size compared to a non flare-corrected mask. We will explore the impact of this correction in terms of file sizes and inspection prep throughput.

8166-77, Session 25

Challenges for 1x device manufacturing using EUVL: scanner and mask

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No abstract available

8166-78, Session 25

Computational lithography in the EUV era

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No abstract available

8166-79, Session 25

Current status and challenges in EUV mask

H. Morimoto, Toppan Printing Co., Ltd. (Japan)

No abstract available

8166-80, Session 25

EUV masks for HVM: progress and challenges

S. Chin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

No abstract available

8166-81, Session 25

Imaging performance and defect printability of 22-nm node EUV mask using EUV exposure tool

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No abstract available