SPIE. ADVANCED LITHOGRAPHY

INTERNATIONAL YEAR OF LIGHT 2015

FORTY-YEAR 40 ANNIVERSARY

2015 TECHNICAL SUMMARIES.

WWW.SPIE.ORG/AL

Conferences & Courses
22–26 February 2015

Exhibition
24–25 February 2015
San Jose Marriott and

San Jose Convention Center
San Jose, California, USA

SPIE. ADVANCED LITHOGRAPHY

Mircea V. Dusa
ASML US, Inc.
2015 Symposium Chair

Bruce W. Smith
Rochester Institute of Technology
2015 Symposium Co-Chair

DATES

Conferences & Courses: 22–26 February 2015
Exhibition: 24–25 February 2015

LOCATION

San Jose Marriott and
San Jose Convention Center
San Jose, California, USA

Contents

SPIE would like to express its deepest appreciation to the symposium chairs, conference chairs, program committees, session chairs, and authors who have so generously given their time and advice to make this symposium possible.

The symposium, like our other conferences and activities, would not be possible without the dedicated contribution of our participants and members. This program is based on commitments received up to the time of publication and is subject to change without notice.

Click on the Conference Title to be sent to that page

Conference 9422: Extreme Ultraviolet (EUV) Lithography VI

Monday - Thursday 23–26 February 2015

Part of Proceedings of SPIE Vol. 9422 Extreme Ultraviolet (EUV) Lithography VI

9422-1, Session 1

EUV for SOC: Does it really help? *(Keynote Presentation)*

Greg Yeric, ARM Inc. (United States)

No Abstract Available

9422-2, Session 1

Progress and challenges toward EUV HVM *(Keynote Presentation)*

Chang-Moon Lim, SK Hynix, Inc. (Korea, Republic of)

No Abstract Available

9422-3, Session 2

Toward 10nm half-pitch in EUV lithography: results on resist screening and pattern collapse mitigation techniques

Tero S. Kulmala, Michaela Vockenhuber, Paul Scherrer Institut (Switzerland); Michael J. Leeson, Ernisse S. Putna, Intel Corp. (United States); Yasin Ekinci, Paul Scherrer Institut (Switzerland)

Extreme ultraviolet lithography (EUVL) is considered as the most promising technology for further increasing the resolution in high-volume manufacturing (HVM) of integrated circuits. Still, some challenges need to be overcome for the introduction of EUVL into production phase. One of the main challenges in EUVL is the development of EUV resists that fulfill strict requirements of sensitivity, resolution, and line-edge roughness (LER). Chemically amplified resists (CARs) have been the major paradigm in the global effort of EUV resist development. Nevertheless, we observe a slow-down in the progress of CARs for EUV. Therefore, new resist paradigms have been explored in recent years with increasing attention, such as inorganic resists incorporating metals or nanoparticles with high EUV absorption.

Here, we present our results on the performance of EUV resists using EUV interference lithography (IL) tool of Paul Scherrer Institute (PSI). In IL aerial images are created without the limitations of projection optics making it a simple and low-cost technique. The gratings for IL are written by electron beam lithography on silicon nitride membranes. As the diffracted beams interfere with each other an aerial image with a period half of that of the grating is created for first order diffracted beams enabling very high resolution patterning. The EUV-IL tool at PSI combines the benefits of the short wavelength and interference lithography enabling resolution down to 7 nm half-pitch (HP).

We report on the recent results of our resist screening efforts with the main focus on investigating a wide range of CARs and inorganic resists in their developmental phase from our collaborators from around the world. We present a detailed analysis of the performance of these materials and discuss the observed trends with a particular focus on identifying the most promising materials when moving towards 10 nm HP resolution. We observed striking differences in the response of EUV and e-beam exposure between the CARs and inorganic resists. In order to gain a deeper insight, we performed comparative studies of CARs and inorganic resists with different flare levels and observe their effect on the resists' LER, exposure latitude (EL), and normalized image log-slope (NILS).

As the patterned feature sizes approach 10 nm HP, pattern collapse becomes a significant challenge. Reducing the thickness of the resist can partially solve this issue but at the expense of an increased LER. Therefore, other approaches that allow for the use of resist layer thicknesses capable of meeting the requested LER specifications have to be developed. Here, we present our results on novel rinsing and pattern freezing methods that significantly mitigate the issue.

9422-4, Session 2

Extending resolution limits of EUV resist materials

Marie E. Krysak, Michael J. Leeson, Ernisse S. Putna, James M. Blackwell, Intel Corp. (United States)

Extreme ultraviolet lithography (EUVL) technology continues to progress and remains a viable candidate for next generation lithography1, which drives the need for EUV resists capable of high resolution with high sensitivity and low LWR. While chemically amplified resists (CARs) have demonstrated the ability to pattern 12nm half-pitch features2, pattern collapse continues to limit their ultimate resolution. We have taken multiple approaches to extend resist capabilities past these limits. Recent results in pattern collapse mitigation using a resist encapsulation and etch back strategy will be discussed. We continue to investigate EUV patterning of semi-inorganic resists to simultaneously increase EUV photon absorption and extend mechanical strength beyond CAR capabilities. Spectroscopic techniques were used to probe the reaction mechanism of inorganic-based nanoparticle photoresists, and have provided key insights to further understanding the mechanism of this class of materials.

[1] Peeters, R., et. al., Proc. SPIE 9048, Extreme Ultraviolet (EUV) Lithography V, 90481J, 2014.

[2]Ekinci, Y., et. al., Proc. SPIE 9048 Extreme Ultraviolet (EUV) Lithography V, 904804, 2014.

9422-5, Session 2

Relationship between information and energy carried by extreme-ultraviolet photons: consideration from the viewpoint of sensitivity enhancement

Takahiro Kozawa, Osaka Univ. (Japan); Julius Joseph S. Santillan, Toshiro Itani, EUVL Infrastructure Development Ctr., Inc. (Japan)

The miniaturization of features in lithography has been achieved by repeatedly replacing the exposure tools with those of the shorter wavelength. After ArF immersion lithography, extreme ultraviolet (EUV) radiation, the wavelength of which is 13.5 nm, is expected to be the next-generation exposure source. The resolution of chemically amplified resists has reached the sub-15 nm (half-pitch) level, assisted by the development of 13.5 nm EUV lithography. With the reduction of wavelength, the energy of photons has been increased. On the other hand, the development of highly sensitive resists is increasingly demanded because of the delay of high power exposure sources. Furthermore, the number of photons used for the fabrication of a pattern has, of course, decreased with the reduction of the pattern size. Thus, the number of photons available for pattern generation has been rapidly decreased. In future lithography, stochasticity will be a serious concern.

In lithography, the role of photons is to transfer information and energy.

The resist patterns are fabricated in accordance with the mask information carried by photons. The energy of photons is used to induce the chemical reactions required to change the solubility of the resist. On the other hand, the role of resist materials is to convert an optical image to a real binary image, namely, a resist pattern. In this study, the relationship between information and energy carried by EUV photons was investigated on the basis of the sensitization mechanisms of EUV resists and the experimental results obtained by SFET of EIDEC. The feasibility and requirement for the development of highly sensitive resists are discussed from the viewpoint of the stochastic effects.

A part of this work was supported by the New Energy and Industrial Technology Development Organization (NEDO).

9422-6, Session 2

New developments in ligand-stabilized metal oxide nanoparticle photoresists for EUV lithography

Christopher K. Ober, Jing Jiang, Ben Zhang, Li Li, Emmanuel P. Giannelis, Cornell Univ. (United States); Mark Neisser, Jun Sung Chun, SEMATECH Inc. (United States); Reyes Sierra, The Univ. of Arizona (United States)

The introduction of EUV lithography to manufacturing requires the development of both new EUV exposure tools and photoresists. The main challenges for photoresists are to achieve high resolution, and low roughness patterning at very high sensitivity given the limited intensity of current sources. A new class of photoresist formed from ligand-stabilized metal oxide nanoparticles shows extraordinary sensitivity for EUV lithography. These nanoparticles are processed in traditional organic solvents for both deposition and development as negative tone resist; positive tone images are possible if the aqueous base developer is used in addition to a post-exposure bake step. This paper presents new developments in the study of ligand-stabilized nanoparticle photoresists for EUV lithography.

It is our current understanding that a key aspect of the solubility change of these photoresists during exposure involves ligand displacement by anions generated from photoactive compounds such as sulfonic acid photoacid generators. Both positive and negative tone patterning are possible and depend on thermal treatment history and choice of developer. On the basis of a non-chemically amplified ligand exchange mechanism, new resist structures were created. Both aromatic and aliphatic carboxylic acids with different functional groups have been studied in the formation of the nanoparticles and include dimethylacrylic acid, isobutyric acid, toluic acid, and nitrobenzoic acid. It has been shown that those nanoparticles with higher binding affinity ligands show better resolution and line edge roughness under EUV exposure. Some formulations demonstrate EUV sensitivity as high as 1.4 mJ/cm2, while other formulations demonstrated that the improved LER to 3-5nm. The overall resolution, sensitivity and roughness tradeoff has been evaluated and provides an understanding of the structure - property relationships.

Aspects of the EHS properties of these new photoresists have been investigated and will be discussed. We have also investigated the dual tone patterning of ligand-stabilized nanoparticle photoresists by dynamic light scattering, zeta potential and hydrodynamic diameter measurements. That the nanoparticle size increases on exposure indicates that the patterning mechanism is more complex than simple ligand exchange.

9422-7, Session 3

Investigating secondary electron behavior in EUV photoresists with experimentation and simulation

Amrit Narasimhan, Bharath Srivats, Justin Turok, Henry C. Herbol, Liam Wisehart, Eric Tsui, SUNY College of Nanoscale Science and Engineering (United States); Mark Neisser, SEMATECH Inc. (United States); Leonidas E. Ocola, Argonne National Lab. (United States); Gregory Denbeaux, Robert L. Brainard, SUNY College of Nanoscale Science and Engineering (United States)

EUV photons expose photoresists by complex interactions including photoionization to create primary electrons (~80 eV), and subsequent ionization steps that create secondary electrons (10-60 eV). The mechanisms by which these electrons interact with resist components are key to optimizing the performance of EUV resists and EUV lithography as a whole.

In this paper, we will present both experimental and modelling results. An electron exposure chamber was built to probe the behavior of electrons within photoresists. Upon exposure and development of a photoresist to an electron gun, ellipsometry was used to identify the dependence of electron penetration depth and number of reactions on dose and energy. We will present the results of this experiment.

We will also present cLESiS, a robust software that uses first-principles based Monte Carlo simulations to track secondary electron production, penetration depth, and reaction mechanisms within materials-defined environments. cLESiS has been refined and validated via comparisons between simulated and empirical electron penetration depths in several PAGs and electron scattering cross-sections in several resists. Users can access cLESiS via the internet, define materials and simulation parameters through an easily navigable GUI, and generate data and graphics output.

9422-8, Session 3

Comparison of shot noise in EUV and e-beam lithography

Suchit Bhattarai, Univ. of California, Berkeley (United States); Shaul Aloni, Weilun L. Chao, Lawrence Berkeley National Lab. (United States); Andrew R. Neureuther, Univ. of California, Berkeley (United States); Patrick P. Naulleau, Lawrence Berkeley National Lab. (United States)

Shot noise in EUV resists was recently studied by comparing LER in EUV and gray-scale e-beam lithography [1], where the latter was demonstrated as a technique for matching the aerial image gradient with e-beam to that with EUV patterning. Despite closely matched resist exposure latitudes and close to equal predicted number of absorbed quanta, LER with e-beam was 2.4x larger than with EUV patterning. Absorption of EUV photon is adequately explained by the Beer-Lambert model, which can be used in conjunction with measured optical absorptivity of resists to obtain accurate prediction for probability of photon absorption in a resist of known thickness. Analytical approximations for energy absorption statistics of 100 keV electrons however are still unclear and need experimental validation. In this paper we demonstrate electron energy loss spectroscopy (EELS) as a technique for measuring the probability of high-energy electron absorption in chemically amplified EUV resists.

EELS is performed by spinning 24 nm thick resist on a 20 nm thick silicon nitride window. EELS spectra for the resist/nitride stack and the nitride by itself are then acquired and normalized by the integrated electron count to obtain the respective energy loss probability density functions (PDF). The energy loss PDF for the resist is obtained by subtracting the PDF for the nitride from that of the resist/nitride stack. Majority of events in the EELS spectra are found to be low-energy (< 2eV) elastic events. The probability of an electron losing at least 2 eV is 0.36 for the resist/nitride stack, 0.22 for nitride by itself, and 0.14 for the 24 nm thick resist.

Results show that plasmon interactions (collective valence electron oscillation) are the most dominant inelastic mechanisms in the resist. For example, probability of an incident electron losing between 10 eV and 60 eV is 0.10, while the chance of the electron losing more than 100 eV is 0.01. Since the valence electron ionization energies of the resist constituent elements are below 50 eV [2], analysis of the role played by plasmon interactions in energy delivery, and their contributions relative to

the less probable higher energy (>100 eV) ionization events is in progress. Repeatability of the weak 5 eV peak found in the EELS spectra is also being investigated to determine whether significant evidence of direct PAG activation exists. We will also provide in-depth shot noise comparisons for additional experimental data on line/space and contact array patterning with gray-scale e-beam, where the EELS data will be used for electron absorption probability calculations.

REFERENCES

[1] Bhattarai, C., Chao, W., Neureuther, A. R., Naulleau, P. P., "Comparative Analysis of Shot Noise in EUV and E-Beam Lithography," Proc. SPIE 9048 (2014).

[2] Chang, R., [General Chemistry: The Essential Concepts (4th ed.)], McGraw-Hill, New York, pp. 251, (2006).

This research was supported by collaboration with the IMPACT+ program.

This work was performed in part at Lawrence Berkeley National Laboratory which is operated under the auspices of the Director, Office of Science, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231.

9422-9, Session 3

Low-energy electron (0-100eV) interaction with resists using LEEM

Aniket Thete, Daniel Geelen, Leiden Univ. (Netherlands); Sander F. Wuister, ASML Netherlands B.V. (Netherlands); Sense Jan van der Molen, Leiden Univ. (Netherlands); Rudolf M. Tromp, IBM Thomas J. Watson Research Ctr. (United States) and Leiden Univ. (Netherlands)

Extreme UV lithography, under development as the next generation lithography technique, makes use of 13.5nm wavelength light with 91.7eV photon energy to achieve sub-10 nm features. However, this high energy radiation gives rise to the generation of lower energy secondary electrons ranging from 0 - 80eV. The mean free path of low energy electrons (LEEs) increases rapidly below ca. 30eV allowing them to migrate several nanometers from their point of origin. These electrons have sufficient energy to further react with the surrounding resist molecules. This gives rise to unintentional exposure of the polymer, and to feature broadening as well as line edge blurring. This can pose a serious problem especially for sub-10 nm resolution features.

Low Energy Electron Microscopy (LEEM) can be extremely useful to investigate the LEE interactions with resist molecules. We mimic the LEEs generated during EUV exposure using LEEM and expose the resist with precise electron energies and doses. This is the first attempt to investigate polymer samples using LEEM, using PMMA as a well-studied model resist. At lower energies we identify an interaction threshold at ~18eV irrespective of the PMMA molecular weight and film thickness. We are able to quantify LEE-resist interactions from which it is possible to calculate reaction rates. The dose was varied over a large window of (1-50000 μC/cm2). Over this large range PMMA changes its tone from positive to negative from low to high electron dose. Experiments on EUV resist are presently underway and first results will be reported.

9422-10, Session 4

Performance optimization of MOPA prepulse LPP light source *(Invited Paper)*

Alexander A. Schafgans, ASML (United States); Daniel J. Brown, ASML US, Inc. (United States); Igor V. Fomenkov, Robert J. Rafac, Daniel J. Riggs, Wayne J. Dunstan, Matthew Graham, Yezheng Tao, Nigel R. Farrar, ASML (United States); Hans Meiling, ASML (Netherlands); Christian Wagner, Ron Kool, Alberto Pirati, ASML Netherlands B.V. (Netherlands); David C. Brandt, ASML (United States)

This paper describes the development and evolution of the critical architecture for a laser-produced-plasma (LPP) extreme-ultraviolet (EUV) source for advanced lithography applications in high volume manufacturing. In this paper we discuss the most recent results from high power testing on our laboratory based development systems, and describe the requirements and technical challenges related to successful implementation of those technologies on production sources. System performance will be shown focusing on prepulse operation with high Conversion Efficiency (CE) and with dose control to ensure high die yield. Specifically, we describe the most effective optimized modes of operation and how specific source dynamics can be controlled at high power. Advances in EUV metrology systems, plasma diagnostics, optics and controls will also be described. Finally, experimental results evaluating technologies for generating stable EUV power output for a 250W HVM LPP source will be reviewed.

9422-11, Session 4

Performance of one-hundred watt HVM LPP-EUV source

Hakaru Mizoguchi, Takashi Saitou, Taku Yamazaki, Gigaphoton Inc. (Japan)

We have been developing CO2-Sn-LPP EUV light source which is the most promising solution as the 13.5nm high power light source for HVM EUVL. Unique and original technologies such as; combination of pulsed CO2 laser and Sn droplets, dual wavelength laser pulses shooting and mitigation with magnetic field have been developed in Gigaphoton Inc.. The theoretical and experimental data have clearly showed the advantage of our proposed strategy. Based on these data we are developing first practical source for HVM; "GL200E". This data means 250W EUV power will be able to realize around 20kW level pulsed CO2 laser. We have reported engineering data from our resent test such around 43W average clean power, CE=2.0%, with 100kHz operation and other data 1).

We have already finished preparation of higher average power CO2 laser more than 20kW at output power cooperate with Mitsubishi electric cooperation2). Recently we achieved 92W with 50kHz, 50% duty cycle operation3). Further improvements are underway, we will report the latest challenge to more than one hundred watt stable operation, around 4% CE with 20 micron droplet and magnetic mitigation.

Reference

1) Hakaru Mizoguchi, et. al.: "Sub-hundred Watt operation demonstration of HVM LPP-EUV source", Proc. SPIE 9048, (2014) [9048-12]

2) Yoichi Tanino et.al.:" A Driver CO2 Laser Using Transverse-flow CO2 Laser Amplifiers" (EUV Symposium 2013, Oct.6-10.2013, Toyama)

3) Hakaru Mizoguchi et al.:" Update of EUV source development status for HVM lithography "Workshop NGL 2014, Japan society of Applied physics (Kuramae hole in TIT,17.July 2014)

9422-12, Session 4

Considerations for a free-electron laser-based extreme-ultraviolet lithography program

Erik R. Hosler, Obert R. Wood II, GLOBALFOUNDRIES Inc. (United States); William A. Barletta, Massachusetts Institute of Technology (United States); Pawitter J. Mangat, Moshe E. Preil, GLOBALFOUNDRIES Inc. (United States)

Recent years have seen great strides in the development of extreme ultraviolet laser-produced plasma (EUV LPP) sources as EUV exposure tools in the field are now capable of meeting the requirements of advanced technology node development. Nevertheless, as the required exposure dose scales for production volumes, EUV sources must provide 500-1000

W to maintain an EUV exposure tool throughput of greater than 125 wafers per hour, given a predicted >50 mJ/cm2 dose requirement. A free-electron laser (FEL) based source offers a cost effective, single-source alternative for powering an entire EUV lithography program at the prerequisite power. Furthermore, lithography program scaling by wavelength or prerequisite source power (number of scanners at a given power) is easily accomplished with FEL technology. [1-3]

Integration of a FEL into a semiconductor Fab will require both unique facility considerations as well as a paradigm shift in lithography operations. In particular, careful consideration must be given to the accelerator design as well as the layout of the Fab and scanner tools such that near 100% light source uptime may be realized. Critical accelerator configurations relating to energy recovery, multi-turn acceleration, and operational mode are discussed from engineering/scientific, cost-minimization, and safety perspectives. Furthermore, the individual components of a FEL (electron injector, RF systems, undulator, etc…) are examined with respect to both design and cost, considering existing technology as well as prospective technological developments. Finally, the technical and scientific challenges facing FEL industrialization for the semiconductor industry are discussed alongside a projected integration roadmap for successful implementation.

[1] Y. Borodovsky, "EUV Lithography at Insertion and Beyond."

[2] K. Cho, H. Nakagawa, K. Maruyama et al., "Key parameters of EUV resists for contact hole applications," Proceedings of SPIE, 8322, 83221B-83221B-9 (2012).

[3] J. Thackeray, J. Cameron, V. Jain et al., "Progress in resolution, sensitivity, and critical dimensional uniformity of EUV chemically amplified resists," Proceedings of SPIE, 8682, 868213-868213-12 (2013).

9422-13, Session 4

Sub-aperture EUV collector with dual-wavelength spectral purity filter

Torsten Feigl, Marco Perske, Hagen Pauer, Tobias Fiedler, optiX fab GmbH (Germany); Uwe D. Zeitner, Robert Leitel, Sven Schröder, Marcus Trost, Stefan Risse, Ralf Steinkopf, Fraunhofer-Institut für Angewandte Optik und Feinmechanik (Germany); Frank Scholze, Christian Laubis, Physikalisch-Technische Bundesanstalt (Germany)

Today's EUV source concepts for HVM focus on laser-induced plasma generation using CO2 lasers in combination with Sn droplets. Different approaches of CO2 laser suppression have been discussed and realized in the past such as binary phase gratings and CO2 AR coatings. While CO2 AR coatings suffer from a significant EUV reflectance loss at 13.5 nm wavelength, binary phase gratings for 10.6 μm show great advantages in terms of EUV reflectance, IR suppression and mechanical stability. Binary grating structures for 10.6 μm are implemented in today's LPP collector mirrors. They significantly suppress the CO2 laser wavelength of 10.6 μm and contribute to clean EUV photons in the intermediate focus.

Since pre-pulse technology significantly enhances the conversion efficiency of EUV generation, source manufacturers use this technique to condition the Sn droplets. Different types of pre-pulse lasers are in operation today: CO2 pre-pulse lasers operating at 10.6 μm and YAG pre-pulse lasers operating at 1064 nm. As a consequence the combination of a 10.6 μm main pulse CO2 laser and a 1064 nm pre-pulse YAG laser would require a spectral purity filter that suppresses both wavelengths at the same time.

This paper discusses a new approach of a dual-wavelength spectral purity filter to suppress 10.6 μm and 1064 nm IR radiation at the same time. The dual-wavelength spectral purity filter combines two binary phase gratings that are optimized for 10.6 μm and 1064 nm, respectively. The dual phase grating structure has been realized on test samples and an elliptical sub-aperture EUV collector mirror having a diameter of 150 mm. IR suppression factors up to 1000 at 10.6 μm and 1064 nm and EUV reflectance levels of more than 60 % at 13.5 nm have been measured on the sub-aperture EUV collector. The optical performance at 13.5 nm and the IR suppressions at 10.6 μm and 1064 μm as well as the manufacturing process of the grating structures will be discussed in the paper. The dual-wavelength spectral purity filter can be used in future EUV collector mirror generations to suppress the pre- and main-pulse IR radiation.

9422-14, Session 4

High-radiance LDP source for mask-inspection application

Yusuke Teramoto, Bárbara Santos, Guido Mertens, Ralf Kops, Margarete Kops, Ushio Inc. (Germany); Gota Niimi, Hironobu Yabuta, Akihisa Nagano, Noritaka Ashizawa, Ushio Inc. (Japan); Felix Küpper, Fraunhofer-Institut für Lasertechnik (Germany); Kiyotada Nakamura, Kunihiko Kasama, Ushio Inc. (Japan)

High-throughput actinic mask inspection tools are needed when EUVL enters into volume production phase. One of the key technologies to realize such inspection tools is a high-radiance EUV source of which radiance, as clean photon with sufficient system reliability, is supposed to be 100 W/mm2/sr. Ushio's laser-assisted discharge-produced plasma (LDP) source had been found to be able to provide sufficient radiance with clean EUV photons, good optical stability and system reliability. Introduction of new techniques and minor modifications to a well-developed LDP source brought radiance level up to approximately 200 W/mm2/sr at plasma.

The LDP source is operated at moderate power level in order to ensure sufficient component lifetime and reliability. Operating condition such as discharge pulse energy, discharge frequency and laser parameter was tuned to maximize radiance. As a result, it was experimentally confirmed that peak radiance of a steady-state, 10-kHz operation was 180 W/mm2/sr at plasma. Dose control was also successfully tested at this frequency showing sufficient dose stability.

One of the unique features of Ushio's LDP source is cleanliness despite liquid tin as fuel material. A well-developed and proven debris shield was installed on an experimental machine for detail testing. It was confirmed that radiance behind the shield was as high as 100 W/mm2/sr at 9 kHz. Optical transmission of the shield was as high as 70 % and there was no unfavorable interaction between the shield and plasma. Radiance behind the shield can be further improved by increasing radiance efficiency or optical transmission of the shield. In order to evaluate the source cleanliness, fast ions and neutrals were measured as sputter rate and deposition rate by placing mirror samples of ruthenium downstream the shield. Samples were exposed for at least 108 pulses and surface of each sample was analyzed with XRF and SEM. Deposition of tin was negligible and sputter rate of ruthenium was a few nm/109pulse, which are equivalent to sufficiently long lifetime of the collector. Stability evaluation and dose control test with the debris shield in place will be carried out soon. Detailed and up-to-date results of the development will be presented at the conference.

9422-15, Session 4

Optimum pre-pulsing and target geometry of LPP for efficient EUV and BEUV sources

Ahmed Hassanein, Tatyana Sizyuk, Purdue Univ. (United States)

Light sources for extreme ultraviolet Lithography (EUVL) are continued to face challenges in the demanding performance for high volume manufacture. Currently EUV and beyond EUV (BEUV) community are focused on the dual-pulse laser produced plasma (LPP) using droplets of mass-limited targets. These systems require extensive optimization to enhance the conversion efficiency (CE) and increase components lifetime that requires significant experimental and development efforts.

We continued to enhance our comprehensive HEIGHTS simulation package and upgrade our CMUXE laboratories to analyze and optimize LPP sources and to make projections and realistic predictions of near future powerful devices. HEIGHTS package includes 3-D detail description of all

physical processes involved in LPP devices. The models continued to be well benchmarked in each interaction physics phase of plasma evolution and EUV/BEUV production as well as in the integrated LPP systems. We simulated LPP sources in full 3-D geometry using tin and Gd droplets and fragmented targets composed of microdroplets as a result of prepulse or from mist of tiny droplets distribution. We studied mass dependence, laser parameters effects, atomic and ionic debris generation, and optimization of EUV/BEUV radiation output, the requirements for mitigating systems to reduce debris effects. Our enhanced modeling and simulation included all phases of laser target evolution: from laser/droplet interaction, energy deposition, target vaporization and fragmentation, ionization, plasma hydrodynamic expansion, thermal and radiation energy redistribution, and EUV/BEUV photons collection as well as detail mapping of photons source location and size. Modeling results were benchmarked against experimental studies for the in-band photons production and for debris and ions generation.

9422-16, Session 5

Magnetron sputtering for the production of EUV mask blanks

Patrick A. Kearney, Tat Ngai, Anil Karumuri, Jung Yum, SEMATECH Inc. (United States); Hojune Lee, SAMSUNG Electronics Co., Ltd. (Korea, Republic of) and SEMATECH Inc. (United States); David Gilmer, SEMATECH Inc. (United States); Tuan Vo, SUNY College of Nanoscale Science and Engineering (United States); Frank Goodwin, SEMATECH Inc. (United States)

Ion Beam Deposition (IBD) has been the primary technique used to deposit EUV mask blanks since 1995. It became the primary choice for deposition due to the early defect results and since 2003 has been the focus technology for development to meeting HVM requirements. But in the intervening years, the defectivity of magnetron sputtering has been greatly improved. This paper evaluates the suitability of modern magnetron tools to produce EUV mask blanks and the ability to support HVM production. In particular we show that the reflectivity and uniformity of these tools are superior to current generation IBD tools, and that the magnetron tools can produce EUV films with defect densities comparable to the current best IBD tool performance. Magnetron tools also offer many advantages in manufacturability and tool throughput; however, challenges remain, including transitioning the magnetron tools from the wafer to mask formats. While work continues on quantifying the capability of magnetron sputtering to meet the mask blank demands of the industry, for the most part the remaining challenges do not require any fundamental improvements to existing technology. Based on the recent results and the data presented in this paper there is a clear indication that magnetron deposition should be considered for the future of EUV mask blank production.

9422-17, Session 5

Alternative materials for high-numerical aperture extreme-ultraviolet lithography mask stacks

Obert R. Wood II, Sudharshanan Raghunathan, Pawitter J. Mangat, GLOBALFOUNDRIES Inc. (United States); Erik A. Verduijn, GLOBALFOUNDRIES Inc. (Belgium); Patrick A. Kearney, SEMATECH Inc. (United States); Christian Laubis, Victor Soltwisch, Frank Scholze, Physikalisch-Technische Bundesanstalt (Germany)

All extreme ultraviolet (EUV) masks are comprised of a multilayer (ML) stack, which ideally provides a high reflectivity for all occurring angles of incidence, and a patterned absorber or shifter layer, which defines the features on the mask. Because EUV reflective masks are illuminated at an oblique angle in order to separate incident and reflected light, their coating structure has an inordinately large impact on image quality and gives rise to a horizontal-vertical print difference due to mask shadowing and through-focus pattern placement errors that vary dramatically with pattern pitch. A variety of options for dealing with these so-called 3D mask effects, e.g., double bi-layers stacks, tuned ML stacks with a wider than normal bilayer period, two types of attenuated phase-shift masks, and embedded-shifter phase-shift masks, have already been explored. In this paper, the performance of masks with alternative materials for the commonly used Mo/Si ML reflector and patterned Ta-based absorber are discussed.

In the talk, we will compare the imaging performance of various options under consideration for high-NA EUV mask stacks: Ru/Si ML with 20 bilayers, standard and tuned Mo/Si ML with 40 bilayers and a new thinner Ni-based absorber layer on each of these ML stacks. We will compare lithography process windows and 3D effects such as shadow bias requirements and telecentricity errors through rigorous simulations. We will show that the Ru/Si ML has both a wider spectral and a wider angular bandwidth and that the effective reflectance plane of a Ru/Si ML is ~110 nm closer to the surface of the coating than the effective reflectance plane of a Mo/Si ML. We will also compare the properties of a 26 nm thick Ni-based absorber with the more common ~2x thicker Ta-based absorber. The use of a Ru/Si ML with its shallower effective reflectance plane and a 2x thinner Ni-based absorber is expected to significantly reduce both shadow bias requirements and mask telecentricity errors. The conclusion of the paper will be supported with the results of both experimental measurements and rigorous simulations.

9422-18, Session 5

Understanding EUV mask blank surface roughness induced LER and associated roughness requirement

Pei-Yang Yan, Guojing Zhang, Intel Corp. (United States); Eric M. Gullikson, Ken A. Goldberg, Markus P. Benk, Lawrence Berkeley National Lab. (United States)

As extreme ultraviolet lithography (EUVL) application is moving toward 10nm and beyond technology nodes, many aspects of EUVL mask blank requirements are correspondingly getting tighter. It drives the EUVL cost of ownership higher due to R&D cost and new tool sets requirement to meet new technology specifications. To effectively control the cost of ownership, it is very important to understand and reasonably define all the process error budgets and technology specification requirements. One of the mask blank specifications that we would like to explore for 10nm and beyond technology node is the EUVL mask multilayer (ML) blank surface roughness. ML blank surface roughness can either be attributed from blank substrate surface roughness or form ML deposition process. The specification for ML surface roughness historically comes from ML blank defect inspection tool requirement. ML surface roughness will cause inspection background noise which reduces the inspection sensitivity. Later, new concerns on ML surface roughness induced wafer pattern line edge roughness (LER) arise. Today, the EUVL blank manufactures are able to produce EUVL mask substrate with surface roughness in a range of 0.06-0.08nm and ML surface roughness in a range of 0.06-0.1nm. The question that we would like to answer in this study is whether further tightening the ML blank surface roughness specification for the purpose of LER reduction will be beneficial. In this study, we have studied wafer level pattern LER as a function of EUVL mask surface roughness via Lawrence Berkeley National Lab High-NA Actinic Reticle Review Tool. The pattern LER is evaluated via actinic aerial images. The advantage of using aerial image evaluation is to separate the ML surface roughness induced LER from resist intrinsic and process induced LER which is a dominant source of the total wafer pattern LER under the current EUV resist process. Our study compares the pattern LER for different surface roughness conditions at different NA and partial coherence values. We found that the blank surface roughness induced LER at current blank roughness level is less than 0.5nm 3-sigma at the best focus condition. Further reducing EUVL mask blank surface roughness down to 0.05nm and below will increase the blank cost with little benefit in improving the pattern LER. In addition to discussing pattern LER response to the blank surface

roughness under different illumination conditions, we will also present detailed analysis and discussion of pattern LER response to the mask blank surface roughness at different defocus and different feature sizes. Finally, based on the experimental results, we will provide our assessment for EUVL ML blank surface roughness specification for future technology nodes.

9422-19, Session 5

Development and evaluation of interface-stabilized and reactive-sputtered oxide-capped multilayers for EUV lithography

Michael D. Kriese, Yuriy Y. Platonov, Jim R. Rodriguez, Rigaku Innovative Technologies, Inc. (United States); Charles Tarrio, Steven E. Grantham, Shannon B. Hill, Thomas B. Lucatorto, National Institute of Standards and Technology (United States)

A critical component of high-performance EUV lithography source optics is the reflecting multilayer coating. The ideal multilayer will have both high reflectance and high stability to temperature cycling. Additionally the capping layers must provide resistance to degradations from exposure to an EUV source, and also be compatible with, or enhance, the systems used for cleaning exposed multilayer coating. We will report on the results of development of C and B4C stabilized Mo/Si multilayers used to increase the as-deposited peak reflectivity (Rp) as well as decreasing the loss of peak reflectivity (Rp) as a function of annealing temperature. Previous results demonstrate that these layers prevent loss of Rp for temperatures up to 600º C. Results of interface-stabilization layers on either the Mo-on-Si interface and the Si-on-Mo interface are individual evaluated, as well as the full four-layer system. Results on the use of reactively-sputtered oxide capping layers such as TiOx and ZrOx will be presented as well, along with results of exposure testing. The deposition is performed in a dual process-chamber inline magnetron system, using reactive sputtering for the production of capping layers. The reflectometer and exposure apparatus at the NIST Physics Laboratory is used for evaluation of the performance. Exposure results on the resistance to oxidation in the presence of water vapor, as well as the hydrogen-cleaning after hydrocarbon growth will be presented.

This effort is supported by a CRADA between Rigaku Innovative Technologies (RIT) and the National Institute of Science and Technology (NIST).

9422-21, Session 6

Understanding of stochastic noise

Seo-Min Kim, Chang-Moon Lim, Mi-Rim Jung, Young-Sik Kim, Won-Taik Kwon, SK Hynix, Inc. (Korea, Republic of); Chang-Nam Ahn, Kyu-Tae Sun, ASML Korea (Korea, Republic of); Anita Fumar-Pici, ASML US, Inc. (United States); Alek Chen, ASML Taiwan Ltd. (Taiwan)

Since photon obeys Poisson distribution, the stochastic dose variation can be easily calculated if we can count the number of photons adequately. Small contact-hole would be no doubt the best pattern for easy counting of photons because all photons used for contact-hole formation will be confined in the contact-hole itself. However, stochastic dose variation is not the unique source of stochastic variability. Since stochastic dose variation is a temporal uncertainty, a spatial uncertainty should be considered in addition. And stochastic CD variation should be written by quadratic summation of temporal variation and spatial variation.

In the statistical point of view, latent image can be considered as a probability density function of the absorbed photons in the resist. Sampling finite photons from the total population has statistical uncertainties on the estimation of sampled mean and standard deviation in space domain. Based on these statistical uncertainties, spatial variation term can be calculated approximately and analytically for all patterns. Consequently LCDU can be estimated.

In this study, stochastic model description will be introduced in detail and model prediction will be compared with experimental results for contact-hole LCDU. As an example, Fig.1 shows the comparison results between model prediction and experimental LCDU for dense contact-hole patterns in 0.25NA EUV lithography. Matching looks good for all different conditions with the same model parameters.

9422-22, Session 6

Negative-tone imaging with EUV exposure for 14nm node and beyond

Hideaki Tsubaki, Wataru Nihashi, Toru Tsuchihashi, Makoto Momota, Takahiro Goto, FUJIFILM Corp. (Japan)

Negative tone imaging (NTI) can be achieved with EUV exposure and organic solvent developer. The NTI process may have advantages over conventional positive tone imaging (PTI) with respect to both line-width roughness (LWR) and, for some lithographic patterns, resolution. This is due in part to lower polymer swelling as well as more favorable dissolution mechanics with NTI development. QCM analysis of partially exposed resist films reveal that when n-butyl acetate (nBA) was used as a developer the negative tone image is achieved with limited swelling compared to an the analogous PTI process using 2.38% aqueous tetramethylammonium hydroxide (TMAH). Using nBA to develop the exposed photoresist gave a surface which was smoother (containing a smaller grain size) compared to photoresists developed using TMAH. Lithographic performance comparisons between NTI and PTI were performed on line/space (L/S), trench, and contact hole (C/H) features using an EUV scanner and a point-beam EB exposure tool.

PTI and NTI L/S patterning resulted in similar resolution (16nm) using NXE:3100 whereas trench patterning gave micro-bridging under PTI but not NTI. This micro-bridging resulted in limiting the ultimate resolution for PTI to >20nm. NTI was able to print sub-20 nm trenches without micro-bridging, which is attributed to the low swelling character of the NTI process. Similarly, NTI was able to print 20 nm dots using NXE:3100 with only a little peeling. These results clearly indicate that NTI is a promising candidate to print 10 nm node patterns. Conversely C/H patterning was significantly worse with NTI compared to PTI, that is, only 36 nm contacts with 60 nm pitch was resolved under EUV exposure.

New NTI process and novel sensitizer for EUV lithography will be also described in this paper in view point of material design.

9422-23, Session 6

Acid generation mechanism in anion-bound chemically amplified resists used for extreme-ultraviolet lithography

Yoshitaka Komuro, Tokyo Ohka Kogyo Co., Ltd. (Japan); Hiroki Yamamoto, Kazuo Kobayashi, The Institute of Scientific and Industrial Research (Japan); Katsumi Ohomori, Tokyo Ohka Kogyo Co., Ltd. (Japan); Takahiro Kozawa, The Institute of Scientific and Industrial Research (Japan)

Extreme ultraviolet (EUV) lithography is the most promising candidate for the high-volume production of semiconductor devices with half-pitches of sub 10nm. An anion-bound polymer(ABP), in which at the anion part of onium salts is polymerized, has attracted much attention from the viewpoint of the control of acid diffusion. In this study, the acid generation mechanism in ABP films was investigated using electron (pulse), r, and EUV radiolysis. On the basis of experimental results, the acid generation mechanism in anion-bound chemically amplified resists was proposed. The protons of acids are considered to be mainly generated through the reaction of phenyl

radicals with diphenylsulfide radical cations that are produced through the hole transfer to the decomposition products of onium salts. On the basis of the revealed reaction mechanisms, a Monte Carlo simulation Code was developed. The acid yield upon exposure to EUV radiation was analyzed using the developed Monte Carlo simulation code.

9422-24, Session 6

Novel EUV resist development for sub-14nm half pitch

Masafumi Hori, JSR Micro N.V. (Belgium); Takehiko Naruoka, Hisashi Nakagawa, Tomohisa Fujisawa, Takakazu Kimoto, Motohiro Shiratani, Tomoki Nagai, JSR Corp. (Japan); Ramakrishnan Ayothi, Yoshi Hishiro, JSR Micro, Inc. (United States); Kenji Hoshiko, JSR Micro N.V. (Belgium); Toru Kimura, JSR Corp. (Japan)

Extreme ultraviolet (EUV) lithography is a promising candidate for the manufacturing of semiconductor devices at the sub-14nm half pitch lines and spaces (LS) pattern for 7nm node and beyond. For the high volume manufacturing of semiconductor devices, significant improvement of resolution and sensitivity is required for EUV resist. It is well-known that the key challenge for EUV resist is the simultaneous requirement of ultrahigh resolution (R), low line edge roughness (L) and high sensitivity (S). We found that both resolution and sensitivity are simultaneously improved by controlling acid diffusion length and efficiency of acid generation using novel resin and PAG. In this paper, we will report the recent progress of resolution and sensitivity improvement of JSR novel EUV resist.

9422-25, Session 7

EUV patterning improvement toward high-volume manufacturing

Yuhei Kuwahara, Tokyo Electron Kyushu Ltd. (Belgium); Philippe Foubert, Anne-Marie Goethals, IMEC (Belgium); Kathleen Nafus, Tokyo Electron Kyushu Ltd. (Belgium); Doni Parnell, Tokyo Electron Europe Ltd. (Netherlands); Koichi Matsunaga, Takeshi Shimoaoki, Shinichiro Kawakami, Tokyo Electron Kyushu Ltd. (Japan)

Extreme ultraviolet lithography (EUVL) technology is a promising candidate of semiconductor process for 18nm half pitch and beyond. So far, the studies of EUV for manufacturability are ongoing in some respects. It still requires fine resolution, uniform, smooth patterns and low defectivity, not only after lithography but also after the etch process.

Tokyo Electron Limited and Imec are continuously collaborating to develop manufacturing quality POR processes to EUV with CLEAN TRACKTM LITHIUS ProTMZ-EUV. This next generation coating/developing system has been upgraded with defectivity reduction enhancements which are applied along with TELTM best known methods. We evaluated defectivity at post lithography and post etch process. Apart from defectivity, FIRMTM rinse material and application compatible with sub 18nm patterning is performed to prevent line pattern collapse and increase process window on next generation resist materials.

This paper reports on the progress of defectivity and patterning performance optimization towards the NXE-3300 POR.

9422-26, Session 7

Toward production ready processing with a state-of-the-art EUV cluster

Karen E. Petrillo, IBM Corp. (United States)

EUV lithography is one of candidates for enabling the next generation of devises by using a cost friendly process. IBM installed the latest tool sets at the IBM EUV Center of Excellence in Albany to accelerate EUV lithography development for production use. IBM has established a processing record, 637 wafer exposures in the 24 hours of operation, with this cluster. It is well known that EUV is still struggling with some major issues including the RLS triangle (Resolution, LWR, and Sensitivity). Also defectivity and pattern collapse need improvement in order to meet manufacturing requirements. We will discuss the baseline cluster performance and the improvement strategy in terms of defectivity and pattern collapse in this paper by utilizing coater/developer techniques based on new track platform.

9422-27, Session 7

EUV contact hole patterning with reverse tone imaging process

Sarohan Park, SK Hynix, Inc. (Korea, Republic of) and IMEC (Belgium); Danilo De Simone , Zheng S. Tao, Geert Vandenberghe, IMEC (Belgium); Seo-Min Kim, Chang-Moon Lim, SK Hynix, Inc. (Korea, Republic of)

To apply the EUV process for contact hole patterning, slow resist are often suggested for better local critical dimension uniformity (LCDU) because the photon shot noise effect is reduced under high dose. A slow resist requires high dose in EUV lithography that is cause of low throughput high cost with current insufficient source power. So the negative tone imaging (NTI) process is considered to decrease Dose-to-Size (DtS) because it has higher average absorbed photon density for pattern area than the positive tone imaging (PTI) process.

In this paper, we will present the simulation and experimental comparison results on contact holes (CHs) and pillars (PLs) patterning in EUV with alternative process. Firstly, we have compared the NILS, LCDU and DtS with respect to PTI and NTI process by EUV stochastic simulation. From the simulation results, we found higher NILS and improved LCDU for NTI process when printing PL patterns compared to PTI process when printing CH patterns with similar DtS. Then, we have experimentally evaluated the pillar patterning process with 0.25NA EUV scanner system with PTI process and compared the process margin, LCDU and DtS to the same parameters of the CH pattering process. Further, we have demonstrated the contact patterning as process reverse from pillars by using the Dry Development Rinse Process (DDRP). In spite of the simulation results, the LCDU of pillar patterns and CH patterns after DDRP show worse values compared to the reference resist CH patterns. To analyze these results, we have investigated the flare effect of the experimental conditions. Furthermore, we have evaluated the pillar patterning with NTD process.

9422-28, Session 7

EUV processing and characterization for BEOL

Nicole Saulnier, Yongan Xu, IBM Corp. (United States); Wenhui Wang, GLOBALFOUNDRIES Inc. (United States); Lin L. Cheong, IBM Corp. (United States); Romain Lallement, STMicroelectronics (United States); Lei Sun, Genevieve Beique, GLOBALFOUNDRIES Inc. (United States); Bassem Hamieh, STMicroelectronics (United States); John C. Arnold, Nelson M. Felix, Matthew E. Colburn, IBM Corp. (United States)

The successful demonstration of 637 wafer exposures in 24 hours on the EUV scanner at the IBM EUV Center for Excellence in July, marked the transition from research to process development using EUV lithography. Early process development on a new tool involves significant characterization, as it is necessary to benchmark tool performance and process capability. This work highlights some key learning from early

EUV process development with a focus on the evolution of trench and via patterning through the patterning process. Numerical data will begin with CDU and LER/CER. The LER/CER in EUV resist will be compared to the post etch value to determine the effect of processing. While these numbers are generally used to describe the robustness of 1D trenches or circular vias, the need to accurately evaluate the printability of irregular 2D features has become increasingly important. In the past 5 years, models built from CDSEM contours has become a hot topic in computational lithography. Applying this methodology, the CDSEM contour technique will be used to assess the uniformity of these irregular patterns in EUV resist and after etching. CDSEM contours also have additional benefits for via pattern characterization. While a via is circular, the diameter on a particular axis and the overall area of the hole can be more important than the circularity and CER. Our analysis will compare the traditional CDU/CER approach with the diameter/area approach.

Acknowledgements: This work was performed by the Research and Development Alliance Teams at various IBM Research and Development Facilities

9422-29, Session 7

Implementation of assist features in EUV lithography

Fan Jiang, Mentor Graphics Corp. (United States); Martin Burkhardt, IBM Thomas J. Watson Research Ctr. (United States); James Word, Mentor Graphics Corp. (United States)

The introduction of EUV lithography will happen at a critical feature pitch which corresponds to a k1 factor of roughly 0.45. While this number seems not very aggressive compared to recent ArF lithography nodes, the number is sufficiently low that the introduction of assist features has to be considered. While the small NA makes the k1 factor larger, the depth of focus still needs to be scaled down with wavelength. However the exposure tool's focus control is not greatly improved over the ArF tools, so other solutions to improve the depth of focus, e.g. SRAF, are needed. On the other hand, sub-resolution assist features (SRAFs) require very small mask dimensions, which make masks more costly to write and inspect. Another disadvantage of assist features is the fact that they may cause pattern-dependent best focus shift caused by thick mask effects. Those effects can be predicted, but the shift of best focus and the associated tilt of Bossung curves make the process more difficult to control.

We investigate the impact of assist features on printing in EUV lithography and evaluate advantages and disadvantages. By using image quality parameters such as best focus (BF), image log slope (NILS), depth of focus (DOF), and mask error enhancement factor (MEEF) separately with and without assist features, we will answer the question if we can gain a net benefit for 1D and 2D patterns by adding assist features. Assist features will only be introduced if any net improvement in process variation (PV) outweighs the additional expense of assist patterning on the mask.

In this paper, we investigate the difference in printing behavior of symmetric and asymmetric assist feature placement and whether model based assist feature placement can be introduced for EUV lithography. We also investigate the impact of flare on optimum assist size and placement.

9422-30, Session 7

Optical proximity effects in 4nm EUV lithography: a rigorous study using a non-conforming mesh PSTD method

Michael S. Yeung, Fastlitho Inc. (United States); Eytan Barouch, Boston Univ. (United States)

We have recently demonstrated by rigorous simulation[1] that EUV lithography can be used for the printing of circuits with 4-nm feature size. However, optical proximity effects are very complicated in this regime of feature size, due to the oblique incidence of the EUV illumination and the use of a multilayered mirror. For example, whereas 4-nm lines and spaces can be printed with ease, an isolated space suffers from very poor aerial-image quality. As a result, optical proximity correction (OPC) must be used to reduce the CD difference between isolated and dense features. In the case of general 2D patterns, even though we have demonstrated that they can also be printed using suitable exposure technique, extensive OPC must be used to compensate for line-end shortening and corner rounding. Thus, it is desirable to use rigorous simulation to study optical proximity effects in EUV lithography for 4-nm feature size in greater detail.

In order to simulate EUV masks containing complicated OPC features efficiently, we have developed a pseudo-spectral time-domain (PSTD) formulation using a novel type of mesh structure known as non-conforming mesh. In this type of mesh structure, the corners of each computational cell do not need to coincide with those of its neighbors. Instead, neighboring cells are required to share only boundary segments, but not corners. This freedom of placement of the cell corners allows a rectangular computational mesh to be generated easily even for a 2D mask pattern containing very complicated OPC features, as illustrated in Fig. 1. This enables the fast and accurate simulation of complicated OPC masks in EUV lithography.

In this paper, we will first present the new non-conforming mesh PSTD formulation. We will then apply it to a rigorous study of optical proximity effects in EUV lithography for 4-nm feature size. First, we will show how to reduce the CD difference between isolated and dense features using suitable multilayer tuning. This will enable the printing of a finite grating structure, consisting of a finite number of 4-nm lines and spaces, with very little optical proximity effect at the two ends of the structure, as illustrated in Fig. 2. Then we will show how to use various exposure and OPC techniques to enable the printing of some realistic 2D mask patterns taken from actual circuits with 4-nm feature size, as illustrated in Fig. 3 for both a memory and a SRAM circuit.

Through rigorous simulation of optical proximity effects in 4-nm EUV lithography for complicated 2D mask patterns using the very fast and accurate PSTD method, we hope that the 4-nm node may be reached much sooner than anticipated.

[1] M. Yeung and E. Barouch, "The feasibility of EUV lithography for printing circuits with 4 nm feature size", to be presented at SPIE Photomask Technology 2014 on September 18, 2014.

9422-31, Session 7

Directed self-assembly on resist-limited guiding patterns for hole grapho-epitaxy: Can DSA help lower EUV's source power requirements?

Juan Andres Torres, Fan Jiang, Yuansheng Ma, Joerg Mellman, Mentor Graphics Corp. (United States); Kafai Lai, Ananthan Raghunathan, Yongan Xu, Chi-Chun Liu, IBM Corp. (United States)

While it might sound counter intuitive to combine EUV and DSA since EUV has the potential to achieve resolutions commensurable to the period of traditional PS/PMMA diblock copolymer systems. It the ability of DSA to heal and rectify guiding patterns structures that make this combination attractive as a way to lower the EUV source power requirements for full volume production.

The tradeoff between line edge roughness (LER), Resolution and sensitivity is widely accepted as one of the challenges in resist development. It has been observed that more sensitive materials at a fixed resolution level will give rise to worse LER. Because of the lack of sufficient energy delivered to the resist, it is desirable to have materials which are more sensitive so that the EUV source power requirements could be lowered.

However, most attempts to simultaneously improve resolution, lower LER and increase sensitivity have not been successful. In addition, some studies have suggested that DSA needs to have a perfect guiding pattern in order to

assemble within acceptable error placement budgets. However as this study suggests, the above is true when the diblock copolymer has extremely low polydispersity and no homopolymer has been added. Under such scenario indeed the shape of the guiding pattern is a primary factor in the error placement of the cylinders after assembly.

We have performed a systematic study regarding the diblock composition to keep the size of the cylinder relatively constant despite the size of the guiding pattern. In the same manner under which different guiding patterns shapes have been found to provide acceptable cylindrical assembly using 193nm immersion exposure systems, this study assumes that LER is a random phenomena which conformably follows the shape of the guiding pattern.

While the edges of the guiding pattern will have fluctuations related to the LER of the EUV resist, as long as the centroid of the guiding pattern remains constant, the rectification characteristics of DSA permits adequate hole formation.

In this paper we include the level of LER a guiding pattern can have given a pre-determined diblock copolymer / homopolymer mixture. As the amount of homopolymer increases, the size and placement of the assembled diblock becomes less sensitive to the guiding pattern edge roughness. But the addition of homopolymer is only effective up to a point, as a homopolymer-majority mixture is not able to exhibit proper assembly behavior.

One of the concerns about homo-polymer rich mixtures is the effect it has in the formation of assembly defects. Such effect has not been fully characterized but this study serves as the basis for testing optimal combinations of materials and lithography settings for a EUV system with the end goal to enable hole printing at lower EUV source power requirements.

9422-20, Session PSTue

Novel resist approaches to enable EUV lithography in high-volume manufacturing

Mark Neisser, Kevin D. Cummings, Sean Valente, Cecilia A. Montgomery, Yu-Jen Fan, Ken Matthews, Jun Sung Chun, SEMATECH Inc. (United States)

EUV lithography is needed by the semiconductor industry for both its resolution and for the process simplification it provides compared to multiple patterning. However it needs many innovations to make it a success. One major area where innovation is needed is resist performance. Resists are commercially available for EUV use, but don't provide the required performance at a fast enough photo speed. SEMATECH has a coherent resist program to research and characterize new EUV resist technology. The program involves sponsoring research to develop novel materials, characterizing novel materials, developing methods for characterizing EUV resist and developing an understanding of the mechanisms of novel resist chemistries and how those mechanisms will affect resist performance. Results of various resist characterization methods will be described for both novel systems containing metals and conventional chemically amplified systems. Characterization methods include X-ray measurement of film density, AFM characterization of resist development, determination of resist development rates and determination of chemistry change as a function of exposure dose. These measurements will be discussed in relation to the different compositions and chemical mechanisms of the resist materials tested.

9422-69, Session PSTue

Evaluation of surfactant rinse material and process for EUV lithography

Kazuma Yamamoto, Toshiro Itani, EUVL Infrastructure Development Ctr., Inc. (Japan)

Extreme ultraviolet lithography (EUVL) is a candidate for the sub-10 nm node device manufacturing and beyond. However, resist pattern collapse is one concern for high volume manufacturing. To improve resist pattern collapse, resist, under-layer, and surfactant rinse materials are continuously being developed to improve resist pattern collapse [1]. Among these, surfactant rinse materials are known to be effective. Here, pattern collapse is inhibited through the reduction of capillary force at the drying process following rinse. We have continuously reported on improvement in this surfactant rinse technology.

In this study, we focused on a fundamental evaluation of the surfactant rinse materials and processes. As basis of comparison, a fixed resist material (EIDEC standard resist 1 or ESR1) was utilized for patterning exposures at the 0.3NA EUV small field exposure tool (SFET). The lithographic performance of ESR1 at the new surfactant rinse material and process was compared to those processed with de-ionized water (DIW) rinse and our standard rinse process (EIDEC standard rinse process 1 or ESPr1), which also utilizes a surfactant rinse material. As previously reported, ESPr1 shows better resolution limit compared to those of DIW rinse. However, at ESPr1 resist bridging at narrow pitches were observed. To understand this bridging phenomenon, experiments using high speed atomic force microscopy (HS-AFM) which allows in situ resist pattern analysis during rinse process was conducted. Moreover, as such bridging phenomenon is assumed to be the effect of resist pattern swelling during rinse, investigations on the effect of surfactant rinse process time on resist pattern profile was also performed.

From these experiments, it was found that the surfactant rinse material caused the resist pattern to deform during the rinse process which may have resulted in such bridging. Based on these fundamental studies, a new surfactant rinse process (Rinse A) was evaluated. The lithographic performance of ESR1 with rinse A resulted in better resolution limit compared to the ESPr1, and DIW. This improvement in resolution is mainly due to the reduction of the bridging phenomenon. It is noteworthy, that line width roughness (LWR) and sensitivity of the ESR1 did not change when using the ESPr1 and the rinse A, compared to DIW rinse.

During the conference, a detailed discussion of these results will be discussed.

9422-70, Session PSTue

Measurement of the phase defect size using scanning prove microscope and at-wavelength inspection tool

Tsuyoshi Amano, Hidehiro Watanabe, EUVL Infrastructure Development Ctr., Inc. (Japan); Tsukasa Abe, Dai Nippon Printing Co., Ltd. (Japan)

The influence of phase defects embedded in Extreme ultraviolet (EUV) mask blanks on wafer printing has always been a center of attention because the phase defects as small as 1.0 nm in height or depth are most likely to be printed on wafer at half-pitch 16 nm lines-and-spaces pattern [1]. To detect printable phase defect on the EUV mask blanks, several inspection techniques that employ EUV light or deep ultraviolet light have been developed [2, 3]. Among these techniques, an at wavelength dark-field inspection technique is a prime candidate for the EUV mask blank inspection method for 16 nm technology node [4].

In this study, to investigate the influence of the phase defect volume on the defect detection signals of the at-wavelength dark-field inspection tool, we prepared programmed phase defect EUV mask blanks. The defect type was pit and the lateral sizes were from 14 to 100 nm-wide. The defect sizes were measured after coating the multilayer using scanning prove microscope (SPM) with two types of measurement tips. One is a widely used tip made by silicone with its shape is cone-type. The other is a tip made by carbon nanofiber with its shape is cylinder of 10 nm radius (typical). The experimental results showed that the difference between the measurement repeatability of the phase defect volume using silicone type and carbon nanofiber type were not significant. The measurement accuracy of the phase defects was enough to evaluate the defect inspection yield and defect detection intensity using at-wavelength dark-field inspection tool. However, variation of the defect-to-defect was significant. This result indicates that measuring volume of all phase defects are essential to evaluate the defect detection yield using phase defect inspector and wafer printability.

After measuring the defect volume using SPM, defect detection signal intensity was examined using the dark-field inspection tool. The imaging optics of the inspector utilized in this study consists of a concave and a convex mirror so-called a Schwarzschild optics. The inner and outer numerical aperture (NA) of the Schwarzschild optics is 0.1 and 0.27, respectively. The pixel size of the CCD camera at the EUV blank plane was 462 nm (26X, inspection mode) and 10 nm (1200X, review mode). As a result, even though the defect signal intensity itself had variation, the defect volume can be estimated from the defect signal intensity.

This work was supported by NEDO.

References

[1] T. Terasawa et al., "Phase defect printability and actinic dark-field mask blank inspection capability analyses", Proc. SPIE 7969, 79690V-1 (2011).

[2] T. Terasawa et al., "Actinic phase defect detection and printability analysis for patterned EUVL mask", Proc. SPIE 7636, 763602-1 (2010).

[3] A. Ma et al., "Improvement of EUVL mask blank inspection capability at Intel", Proc. SPIE 7379, 73790I (2009).

[4] A. Tchikoulaeva, "EUV actinic blank inspection: from prototype to production", Proc. SPIE 8679, 86790I (2013).

9422-71, Session PSTue

Verification of an effect of phase defect characteristics on scattered light images

Noriaki Takagi, EUVL Infrastructure Development Ctr., Inc. (Japan)

Extreme Ultraviolet lithography is one of the most promising candidates among the next generation lithography options for printing critical layers of 16 nm half-pitch ULSI devices; and this challenge is possibly extendable to devices with 11 nm half-pitch.

On the other hand, one of the key challenges of EUVL is to make defect-free mask blanks. Therefore we have developed an actinic dark-field inspection tool to detect multilayer phase defect.

It is well understood that DSI(defect signal intensity which is obtained by summing scattered light intensity caused by phase defect) is influenced by phase defect's volume. However, DSI may be influenced by not only defect volume but also other phase defect characteristics. A relationship between DSI and phase defect characteristics has been studied with simulation and experiment, and it was confirmed that DSI was affected by phase defect shape such as aspect ratio of defect height to width. But it is difficult to confirm how defect characteristics influence a scattered light images caused by phase defect in actinic dark-field inspection. In this study, scattered light images will be captured with high magnification optics which is equipped to HVM ABI tool and the effect of phase defect characteristics on the image will be studied. Figure.1 shows cross section of the programmed pit phase defect measured with AFM, and intensity distribution of scattered light caused by programmed pit phase defect. Example1 defect has sharp-like shape compared to Example2 defect. According to this comparison, intensity distribution seems to be affected by phase defect shape.

Additionally, a relationship between focus position in ABI inspection and phase defect characteristics is studied with simulation and experiment. Defect size such as defect height and width are varied, and effect of defect characteristics on focus position is calculated in this simulation. After the simulation, experiment will be done to confirm whether the simulated result fit to experimental result or not.

9422-72, Session PSTue

Low-LER tin carboxylate photoresists using EUV

Ryan Del Re, Miriam Sortland, James Pasarelli, SUNY College of Nanoscale Science and Engineering (United States); Mark Neisser, SEMATECH Inc. (United States); Daniel A. Freedman, State Univ. of New York at New Paltz (United States); Robert L. Brainard, SUNY College of Nanoscale Science and Engineering (United States)

Organic chemically amplified photoresists have dominated the microelectronics industry for two generations of manufacturing technologies (?= 248 nm and 193 nm).1,2 These systems have shown to be quite capable of achieving the necessary photolithographic performance to allow the industry to follow Moore's law. However, we are rapidly approaching a barrier in which the cost and complexity of achieving smaller feature sizes faces diminishing returns. Extreme ultraviolet (EUV, ?= 13.5 nm) is one promising next generation printing technique, but there exists many challenges that must be resolved before it can be implemented. One major challenge for successful EUV implementation is photoresist design.

EUV photons are much higher energy than 193 nm photons, so traditional photoresist design may be inadequate to continue resolving increasingly smaller patterns. As we decrease film thickness to compensate for smaller patterning without line collapse, organic films may be unable to absorb the photons efficiently which may lead to poor sensitivity and line edge roughness (LER). Etch resistance may also be inadequate in these thinner, organic films.3,4 We have previously reported on a new resist system, MORE (Molecular Organic Resists for EUV), that seeks to rectify the potential obstacles that face EUV resist design. By using elements that have a high EUV optical density, we propose that we can create a molecular film that is capable of absorbing more precious EUV photons which may result in higher resolution patterns with better sensitivity and LER.

Here, we present recent lithographic results of several MORE mononuclear tin compounds that have been spin coated into a thin film and exposed to EUV light. We have synthesized a series of tin compounds of the general type (Benzyl)2Sn(COOR)2 = (C6H5CH2)2Sn(OOCR)2 in an attempt to study the effects of increasing ligand bulk and decarboxylative activity on photosensitivity and lithographic performance. While we found that the sensitivity of these compounds is overall poor, one compound, (C6H5CH2)2Sn(OOC(CH3))2, Figure 1, obtained high resolution patterning (16 nm) with low LER (2.1 nm) and moderate resolution patterning (22 nm) with excellent LER (1.4 nm), Figure 2. We also see a linear trend when we compare molecular weight with Emax, Figure 3.

9422-73, Session PSTue

Systematic study of ligand structures of metal oxide EUV-nanoparticle photoresists

Jing Jiang, Ben Zhang, Li Li, Cornell Univ. (United States); Mark Neisser, SEMATECH Inc. (United States); Jun Sung Chun, SEMATECH Inc. (United States) and SUNY College of Nanoscale Science and Engineering (United States); Emmanuel P. Giannelis, Christopher K. Ober, Cornell Univ. (United States)

Metal oxide nanoparticles resist represent a new class of photoresist materials which have exceptional sensitivity for EUV photopatterning. Previous studies of HfO2 MAA have shown sub-20 nm HP patterns at an EUV dose of 4.2mJ/cm2. The patterning mechanism is not a chemically amplified process but instead the solubility switch involves ligand exchange. The binding affinity of ligands on the as prepared resists compared to the anion of the photoactive compound affects the sensitivity of the photoresist under EUV radiation.

Benzoic acid is a ligand with a higher ligand binding affinity compared to other carboxylic acids that have been studied. The EUV patterning results showed that while the sensitivity is lower than 17.5 mJ/cm2 yet the line width roughness is also is improved to 3-5nm. Therefore, to further understand the relationship between resist performance and the ligand binding affinities, we systematically studied analogs of benzoic acid. By adding electron withdrawing or electron donating groups to different positions in the ring, we are able to adjust the binding affinities. The ligands we studied include p-toluic acid, o-toluic acid and nitrobenzoic acid. The C NMR shift of alpha carbons were used to examine the binding affinity of ligands. The chemical, physical properties and the DUV lithographic

performance of these particles are similar to the previous particle compositions. The EUV patterning results were obtained from these ligands and the line edge roughness, resolution and sensitivity were evaluated using Summit software. The EUV study provided us the further understanding of structure and property relationship. These recent results will be summarized in this presentation.

9422-74, Session PSTue

Experimental validation of stochastic: modeling for negative-tone develop EUV resists

Itaru Kamohara, Synopsys GmbH (Germany); Weimin Gao, Synopsys, Inc. (Belgium); Ulrich Klostermann, Thomas Schmoeller, Wolfgang Demmerle, Synopsys GmbH (Germany); Kevin Lucas, Synopsys, Inc. (United States); Danilo De Simone, Eric Hendrickx, Geert Vandenberghe, IMEC (Belgium)

Line width roughness remains a critical factor to realize smaller feature sizes in EUV lithography. The use of bright field mask is expected to have a good performance. Applying negative-tone develop (NTD) resist, which is now being successfully deployed in 193 immersion lithography, to EUV is the candidate but not yet reported so far. In this paper, a new EUV NTD resist material was investigated by comparing experimental metrology data and simulated results. A physics based NTD resist model which also considers stochastic effects has been used for this EUV resist study. The stochastic modeling approach takes shot noise and secondary electron effects during exposure into account, as well as the interaction amongst the finite number of chemical molecules (inhibitor, PAG, quencher) during PEB. Experiments were performed at IMEC using ASML's NXE:3100 EUV exposure tool. The smallest feature size is 24 nm on wafer. The calibrated EUV NTD stochastic resist model reproduces well the measured TWR (trench width roughness) results, obtained by top-down SEM measurements, and cross section SEM data correspond well with simulated stochastic 3D resist profiles including resist height loss. Validation results showed good CD and TWR prediction for the entire process window, through pitch, for dense and isolated structures. The model accuracy is comparable that of continuous (conventional, without stochastic) resist models.

9422-75, Session PSTue

Study of EUVL patterned mask inspection tool for half-pitch (hp) 16nm-11nm node

Ryoichi Hirano, Susumu Iida, Tsuyoshi Amano, Hidehiro Watanabe, EUVL Infrastructure Development Ctr., Inc. (Japan); Masahiro Hatakeyama, Takeshi Murakami, Shoji Yoshikawa, Kenichi Suematsu, Kenji Terao, EBARA Corp. (Japan)

EUV Lithography is a promising technique for the post-2X nm generation lithography because of its excellent resolution. EUVL patterned mask defect detection is one of the major issues to realize device fabrication with EUV lithography. According to the ITRS2013 and defect printability simulations the sensitivity requirement for an EUVL patterned mask inspection system is to be better than 13 nm for hp 11 nm node devices. We have already designed a novel Projection Electron Microscope (PEM) optics that has been integrated into a new inspection system named EBEYE-V30 ("Model EBEYE" is an EBARA's model code) and which seems quite promising for hp 16 nm node EUVL patterned mask inspection. A programmed defect mask was used for demonstrating the performance of the system for the hp 16 nm node. The PEM system performs well for hp 16 nm EUVL patterned mask inspection. Figure 1 shows a defect detection sensitivity platform of the Model EBEYE-V30 inspection system. It has a high resolution and high-throughput electron optics that can enable 19-hours long inspection time with a throughput determined by a data processing rate of 0.6 GPPS (Giga Pixel Per Second), and by a pixel size of 16 nm.

In this paper, we describe the experimental results of the EUVL patterned mask inspection using the above- mentioned system. Here the defect detection is executed by employing the new inspection tool, which utilizes its die-to-die inspection setup. Defect images were obtained as difference images obtained by comparing PEM images with-defects to the PEM images without-defects. Programmed defects in hp 11 nm (44 nm on mask) are applied for defect detection sensitivity evaluation.

Moreover, we discuss the system extendibility to 11 nm node defect detection. The inspection throughput is also one of the important issues of the patterned mask inspection tool. The inspection time is determined by a combination of image sensor pixel size and data processing rate using our PEM system. To improve the inspection throughput for hp 11 nm node defect detection, greater than 1.5 GPPS data processing rate realize less than 7 hours of inspection time. Hence our target is to achieve an inspection time of less than 7 hours. For this purpose, the processing rate is enhanced from 0.6 GPPS to 1.5 GPPS or higher. Figure 2 shows a schematic diagram of a patterned mask inspection tool technology development items. High-speed image sensor, high-speed image processing circuit, and bright/stable electron source are necessary for hp 11 nm defect inspection. The aims of the development are to attain a higher throughput, and increase the defect detection sensitivity by a higher processing rate using a smaller pixel size.

This study is supported by New Energy and Industrial Technology Development Organization (NEDO) and Ministry of Economy, Trade and Industry (METI).

9422-76, Session PSTue

Dependence of defect size and shape on detectability for EUV patterned mask inspection

Susumu Iida, Ryoichi Hirano, Tsuyoshi Amano, Hidehiro Watanabe, EUVL Infrastructure Development Ctr., Inc. (Japan)

The electron beam technique is a candidate for 1X nm EUV mask inspection. Especially the projection electron microscope (PEM) technique has a potential to take the clearer images of small patterns than those by DUV and a potential to inspect masks with the higher throughput than that of SEM inspection system. We had already reported that > 16 nm sized defects were detected on hp 64 nm L/S patterned EUV mask by using PEM inspection system we developed. The detectability of intrusion defect was higher than that of extrusion one. This phenomenon was good agreement with simulated result. In this paper, dependence of defect size and shape on detectability for EUV was investigated using PEM simulator we developed. Figure 1 shows schematic illustration of a top view of EUV mask with various types of defects, and the difference image between simulated PEM image with defects and that without defects. The defect signal intensities for the intrusion defects are much higher than those for extrusion defects. Especially, 16 nm sized pinhole defect was detected with strong intensity (60 sigma) whereas the same sized pin-dot defect was not detected (< 10 sigma). Furthermore, the pinhole defect is more sensitive than the intrusion defect. These phenomena can be explained by the secondary electron yields (SEYs) of EUV mask materials, and the defect size and shape as show in Fig. 2(a). In the case of electron beam (EB) inspection system, because the SEY of absorber is higher than that of ML, bright and dark areas in the EB image correspond to the absorber and ML parts. As an aspect ratio of the defect becomes higher, the SE signal from the ML becomes lower. Hence, when the pinhole defect becomes smaller, the contrast becomes higher. On the other hand, in the case of DUV inspection system, the contrast is inverted because the DUV is reflected by the ML and absorbed by the absorber layer as shown in Fig. 2(b). Therefore, the intrusion and pinhole defect size becomes smaller their defects signal intensities become smaller. We also investigate the detectability difference of various types of defects between SEM and PEM type inspection system.

9422-77, Session PSTue

Performance of actinic EUV mask review using scanning lensless imaging system

Sangsul Lee, Yasin Ekinci, Paul Scherrer Institut (Switzerland)

Actinic EUV mask imaging is an essential method to understand effect of blank, defects, pattern bias and optical proximity corrections owing to the 13.5 nm wavelength reflective properties on off-axis illumination. Mask inspection and imaging tools have been successfully developed using EUV imaging optics. Nevertheless, the traditional actinic inspection systems using imaging optics have several limitations such as optics aberrations, tight alignment tolerances, limited depth-of-focus, low transmission efficiency of the optical components, and high cost of high-resolution EUV optics. On the other hand, coherent scanning lensless imaging technique can be an alternative or complementary method to remedy the limitations of imaging optics for high-resolution characterization on EUV mask.

The Reflective EUV mask scanning lensless imaging tool (RESCAN) is an at wavelength reflective mask microscope designed for computational aerial image measurement and defect review. RESCAN has been installed and operated at the XIL-II beamline of Swiss Light Source (SLS). This computational lensless imaging system is very sensitive to detect phase contrast image because coherent phase retrieval algorithm called ptychography can deliver enhanced resolution and sensitivity. In this technique, diffracted signal from the mask is measured while the mask or the beam is scanned across a coherent illumination. Redundant scattering information from the sample is collected by overlapping scans in neighboring positions.

RESCAN is designed for 20 nm node resolution and we show the imaging results of this tool through reconstructed aerial images of resolution test patterns on a multilayer mask using 0.4 NA and 6° of angle of incidence off-axis illumination. In addition, from the methodological point of view we discuss the imaging effects of different parameters, such as coherence, illumination spot, fill factor, and overlapping ratio, on resolution and sensitivity. Currently the minor upgrade of RESCAN is scheduled for 4th quarter of 2014 to identify the resolution limit of scanning lensless imaging method on transmission system. We discuss the potential imaging performance capabilities of a novel actinic EUV mask inspection technique, based on the transmission coherent scanning lensless imaging of the RESCAN at the SLS.

We believe that our prototype imaging system is a remarkable approach to overcome the limitation of optics for high-resolution and high-throughput reviewing of EUV masks. The RESCAN can contribute to alternative imaging solution on phase defect identification and smallest pattern review, and the alliance with the stand-alone EUV source will generate a significant synergy effect.

9422-78, Session PSTue

Positive-tone resists made from complexes of platinum and palladium

Miriam Sortland, Ryan Del Re, James Passarelli, SUNY College of Nanoscale Science and Engineering (United States); Mark Neisser, SEMATECH Inc. (United States); Daniel A. Freedman, State Univ. of New York at New Paltz (United States); Robert L. Brainard, SUNY College of Nanoscale Science and Engineering (United States)

Extreme Ultraviolet (EUV) light (13.5 nm) is thought to be the next candidate for high volume microelectronic printing technology. As resolution is directly proportional to wavelength, EUV might enable the industry to meet the requirements of many nodes starting at 7 nm.. As EUV resists achieve better resolution, they must be coated thinner to prevent line collapse.1 Consequently, the thinner films must increase in optical density to absorb more EUV photons for better sensitivity and better LER.2 We are proposing a new resist platform consisting of high optical density metal oxide organometallic compounds. Here we will present a subset of this platform utilizing Platinum and Palladium compounds as EUV photoresists. These are the first positive-tone photoresists to come from of this project.

Platinum and Palladium exhibits high optical density which allow more absorption of EUV photons. This gives them the potential to be very sensitive resists and allow thinner films. The synthetic history of Platinum and Palladium is very rich, which provides us with a vast area of compounds to investigate for the use of photoresist. In addition, Platinum and Palladium have a well-known catalytic property and we are hoping to utilize this attribute to make sensitive resists without any use of acid. We have synthesized compounds of Platinum and Palladium with known photoactive ligands and coated these resists in polar solvents. Upon exposure, the chemical response in the photoactive ligand changes the solubility of the resist, making the exposed areas soluble in non-polar solvents. Positive tone contrast curves and imaging have been demonstrated (Figure 1, 2). We have been able to show resolution down to 35 nm and modulation down to 22 nm at a sizing dose of 156 mJ/cm2. We intend to improve resolution and sensitivity of these compounds by chemically altering the composition of the compounds. We will fully disclose the structures of the compounds during the conference.

9422-79, Session PSTue

Experimental test of an argon cusp plasma for tin LPP power scaling

Malcolm W. McGeoch, PLEX LLC (United States)

A new approach to power handling in the tin LPP source has been described theoretically and is now tested experimentally. This involves an argon cusp plasma that ionizes and dilutes tin atoms, then carries them in a guide magnetic field to a large area beam dump. The argon plasma has high enthalpy per atom, so can remove 25kW of waste heat. It also provides a barrier to argon flow that reduces vacuum pumping requirements toward the exit of the EUV source. Assuming 4% conversion efficiency from laser power to in-band 13.5nm radiation, the projected sustained source power is 200W at the intermediate focus.

9422-80, Session PSTue

Phase and amplitude defect distinction with an actinic dark-field microscope

Lukas Bahrenberg, Stefan Herbert, Aleksey Maryasov, Jenny Tempeler, Serhiy Danylyuk, RWTH Aachen (Germany); Rainer Lebert, Bruker ASC GmbH (Germany); Peter Loosen, Larissa Juschkin, RWTH Aachen (Germany)

One remaining challenge for HVM introduction of EUV lithography is the realization of an actinic mask blank inspection tool, which fulfills the requirements of the International Technology Roadmap for Semiconductors. The authors present defect investigations with an actinic (13.5 nm) Schwarzschild objective based dark-field microscope for mask blank inspection. Several updates of the deployed hardware and underlying concepts are discussed in detail.

This includes a novel approach to experimentally distinguish between deformations of the multilayer structure (phase defects) and inhomogeneities on top of the multilayer structure (amplitude defects) with a single inspection procedure. Investigations of the characteristic scattering behavior of phase defects and amplitude defects respectively are carried out.

Programmed structures underneath and on top of a multilayer structure were fabricated in order to obtain phase defects and amplitude defects with defined dimensions.

The defect size sensitivity of actinic inspection is determined. For this, precise light flux analysis is performed with the help of an in-vacuum EUV camera positioned in the sample plane. Obtained information and developed

models are used to calculate interdependencies of different parameters of the tool and to determine critical factors, limiting its performance.

Furthermore, several modular upgrade options are presented, that can increase performance of the inspection tool and enable additional features, extending its usability.

9422-81, Session PSTue

Optimizing performance of multilayer mirror optics for EUV and BEUV lithography

Tatyana Sizyuk, Purdue Univ. (United States)

The performance of extreme ultraviolet lithography (EUVL) devices currently being developed as well as of future lithography tools, which probably will be based on the BEUV sources, critically depend on the efficiency of light collection and transmission to the wafers. Design of multilayer mirrors (MLM) for EUVL is continuously being improved to increase mirrors lifetime and decrease performance degradation. Various mitigating and protective methods are being developed including ionic and atomic debris mitigation by magnetic fields and buffer gas and protection of MLM by the capping layer. Innovative design of MLM optics for future lithography is now being developed and effect of environment specific for the EUV and BEUV sources should be predicted and considered in details.

Simulation tools were enhanced and performance of MLM surfaces subjected to energetic ions in EUV and BEUV sources was compared. The HEIGHTS package was used for the simulation of plasma evolution and ions distribution in LPP systems in dependence on laser beam parameters and target material, density and geometry. The ITMC-DYN package was used to predict mirrors damage by ions with various energies. The ITMC-DYN Monte Carlo package for simulation of ions/target interactions with dynamic changing of target composition was further upgraded to analyze the effect of energetic ions on mirror collection system. Heating of mirror surfaces by radiation from plasma can enhance diffusion processes and this can result in intermixing layers that will further affect and degrade MLM reflectivity. Thermal diffusion processes in multiple-layer structure were analyzed and the dependence of MLM materials mixing on temperature and integrated effect of debris and thermal processes on mirror surface degradation were studied. Several possible mirror system designs being considered for EUV and BEUV lithography with different reflective and capping layers were simulated.

9422-82, Session PSTue

Alternative irradiation scheme for EUV source for inspection applications

Duane Hudgins, Nadia Gambino, Bob Rollinger, Reza S. Abhari, ETH Zürich (Switzerland); Fariba Abreau, Adlyte AG (Switzerland)

Extreme Ultraviolet Lithography (EUVL) is one of the most promising lithography technologies that will allow the surpassing of the critical resolution limits of current ArF lithography techniques for the generation of 10 nm semiconductor chip node size and beyond. The generation of light in the EUV range through a Laser Produced Plasma (LPP) is one of the leading technologies for the development of high volume manufacturing (HVM) lithography light sources. Through the irradiation of tin droplets by high-irradiance laser pulses, plasmas that are highly emissive at around 13.5 nm can be produced.

At the Applied Laser Plasma Science (ALPS) laboratory of LEC-ETH Zürich, a droplet-based laser-produced plasma (LPP) X-ray source with application in EUV metrology has been developed. The main source ALPS II is a prototype source equipped with a large capacity droplet dispenser and a high power (kW), high repetition rate Nd:YAG laser.

To optimize the overall source performances it is fundamental to improve current debris mitigation techniques in order to limit the amount of produced plasma debris (high energy ions, low energy particles and small droplet fragments). The distribution and composition of plasma debris in the source is also dependent on the early stage droplet-laser interaction and the subsequent ablation process. Recent work at the ALPS laboratory has been focused on the understanding of the plasma debris dynamics. In particular, additional methods for coupling the debris to the existing droplet debris mitigation techniques, based on various laser pulsing configurations are explored. These alternative irradiation schemes show potential for spatially shaping the debris composition and for increasing the coupling between the fuel and main pulse laser energy.

In this work, these alternative droplet irradiation schemes will be discussed. The fuel droplet and subsequent debris breakup has been imaged for different laser irradiances ranging from 1-100 GW/cm2. The laser irradiance is tuned through a series of adjustable polarization optics. The droplet imaging setup is realized with a shadowgraph technique utilizing a 1μs pulsed white light LED strobe with a 1μs timing resolution. This technique permits the study of the droplet velocity and the debris dynamics versus the laser irradiance. For the different laser irradiances, the debris velocity and trajectory are measured on the parallel plane to the laser axis. The results have an important relevance for the shaping of liquid droplet targets. The experimental results and their implications for EUVL applications will be also outlined in this work.

9422-83, Session PSTue

Improving process and system for EUV coat-develop track

Masahiko Harumoto, Dainippon Screen Manufacturing Co., Ltd. (Japan); Harold Stokes, Yan Thouroude, Dainippon Screen Deutschland GmbH (Germany); Tadashi Miyagi, Koji Kaneyama, Charles Pieczulewski, Masaya Asai, Dainippon Screen Manufacturing Co., Ltd. (Japan)

EUV lithography (EUVL) is well known to be a strong candidate for next generation, single exposure sub-30nm half-pitch lithography.[1] Furthermore, high-NA EUV exposure tool released two years ago gave strong impression by finer pattern results. On the other hand, it seems that the coat develop track process remains very similar and in many aspects returns to KrF or ArF dry process fundamentals, but in practice 26-32nm pitch patterning coat develop track process also has challenges with EUV resist.

As access to EUV lithography exposures became more readily available over the last five (5) years, several challenges and accomplishments in the track process had been reported, such as the improvement of ultra-thin film coating, CD uniformity, defectivity, line width roughness (LWR) and so on.[2-6] The coat-develop track process has evolved along with novel materials and metrology capability improvements.

Line width roughness (LWR) and defect control are demonstrated utilizing SOKUDO DUO coat develop track system with ASML NXE:3100 exposures in IMEC (Leuven, Belgium) clean room environment. Additionally, we will show the latest lithographic results obtained by novel processing approaches in EUV coat develop track system.

9422-84, Session PSTue

Effects of low-molecular weight resist components on dissolution behavior of chemically-amplified resists for extreme-ultraviolet lithography studied by quartz crystal microbalance

Mitsuyasu Masaki, Hiroki Yamamoto, Takahiro Kozawa, The Institute of Scientific and Industrial Research (Japan)

Conference 9422:
Extreme Ultraviolet (EUV) Lithography VI

Extreme ultraviolet (EUV) is regarded as the most promising exposure source for next-generation lithographic technology. For the realization of EUV lithography, EUV resist materials need to be improved from the viewpoint of the trade-off relationships between resolution, line width roughness (LWR), and sensitivity. In order to overcome this trade-off problem, it is essential to understand basic chemistry of resist matrices in resist processes. In particular, the dissolution process of EUV lithography is a key process for improving the trade-off relationship. Also, the high dissolution contrast between exposed and unexposed parts is required for ultrafine patterning. However, the details in dissolution process have not been clarified. Therefore, it is important to understand the dissolution behavior of resist film into alkaline developer. In this study, the dissolution behavior of the poly(4-hydroxystyrene) (PHS) film, which is a model polymer for chemically amplified EUV resists, with photoacid generators (PAGs) was investigated by varying the exposure dose and the acid generator concentration, using quartz crystal microbalance (QCM) in order to understand the effect of each resist component on the dissolution behavior. Also, we have studied the dissolution behavior of chemically amplified resist composed of partially protected PHS with and without acid generators.

In the experiment, PHS and PHS partially-protected with t-butoxycarbonyl group (tBOC-PHS) were used as a polymer for chemically amplified resists. Triphenylsulfonium-triflate (TPS-tf) and Triphenylsulfonium-nonaflate (TPS-nf) were used as an acid generator (PAG). The resist solutions were prepared by dissolving PHS or tBOC-PHS with acid generator in propylene glycol monomethyl ether acetate (PGMEA) for QCM measurement. The resist solutions were spin-coated onto QCM substrate to form thin film. They were exposed to EUV radiation. After exposure, they were baked in the temperature range of 90 oC for 60 s. The development behavior of PHS and tBOC-PHS films with and without acid generators was investigated by the QCM-based development analyzer (RDA-Qz3). Resist film thickness was measured with a surface profiler (ET200 (Kosaka Laboratory Ltd.)) and spectroscopic ellipsometry (UVISEL (Horiba)).

The relationship between resist thickness and development time were obtained by fitting the relationship between development time and resonance frequency in QCM experiments. In PHS films, it was found that the dissolution speed in these resist film became slower with the increase in TPS-tf concentration. Also, it was observed that the dissolution speed in PHS film with TPS-nf was faster than that of PHS film with TPS-tf in the presence of the same concentration of acid generators for both cases before and after EUV exposure. The solubility in the developer depends on the remaining PAG concentration and the structure of acid generators. In tBOC-PHS films, the swelling of resist film containing TPS-tf with different concentration was observed before and after EUV exposure. Also, the sensitivity of tBOC-PHS with acid generators became higher with increase of PAG concentration because of the increase in the acid generation efficiency. However, the dissolution speed was slower with increase of TPS-tf concentration. It is important for the EUV resist design to take into account the concentration of undecomposed PAG.

9422-85, Session PSTue

Evaluation of optical properties of EUV resist underlayer

Jung Sik Kim, Seongchul Hong, Jae Uk Lee, Seung Min Lee, Hanyang Univ. (Korea, Republic of); Jung Hwan Kim, Hyun Min Song, Hanyang Univ (Korea, Republic of); Jinho Ahn, Hanyang Univ. (Korea, Republic of)

Since the use of the resist underlayer (UL) has a beneficial effect of improving exposure latitude, the development of UL is in progress for extreme ultraviolet lithography (EUVL) as well. Since the aspect ratio of patterns becomes higher for a smaller feature size, a high performance EUV UL will be in demand.

In this study, we evaluated the optical properties of EUV UL by using the lithography simulation tool PROLITH X5 (KLA-Tencor), which can perform stochastic resist patterning simulation. We quantified the stochastic imaging characteristics of 14 nm half-pitch (hp) line and space (L/S) pattern and 18 nm hp contact hole (C/H) pattern by varying the refractive index and extinction coefficient of the UL in 0.5NA condition with the conventional binary intensity mask.

There was a significant change in imaging performance by varying the refractive index of EUV UL. As the difference of refractive index between UL and photoresist was increased, the reflectivity became higher at the interface between UL and photoresist. Since the total amount of absorbed light in photoresist became larger, feature size became smaller for L/S pattern and larger for C/H pattern than the target CD, and the stochastic imaging properties such as CD uniformity and line edge roughness were improved. However, there was a negligible effect in imaging performance by changing the extinction coefficient of UL.

9422-86, Session PSTue

New approach to improve LER of EUV resist pattern by chemical and thermal treatment

Tatsuro Nagahara, Kazuma Yamamoto, Yuriko Matsuura, AZ Electronic Materials (Japan) K.K. (Japan)

LER improvement of EUV resist by ERC:

ERC (Edge Roughness Controller) is a new process and material that improves EUV resist roughness. ERC is applied in development process of photoresist like rinsing material and the function is activated by thermal treatment.

9422-87, Session PSTue

Damage simulation of EUV-multilayered mask under-focused ion-beam irradiation

Kaoru Ohya, Univ. of Tokushima (Japan)

Focused ion beam (FIB) has become one of important tools for micro- and nanostructuring of substrates such as milling, deposition and imaging. The EUV lithography mask repair using FIB technology has exhibited excellent performance. However, the surface is still damaged on the nanometer scale by implanted Ga atoms and the interlayer mixing at the Mo/Si interfaces. In addition, due to non-uniform irradiation of the mask surface the multilayer is shrunken and deformed. It is important to investigate each kind of the damages quantitatively. In this report, we discuss the mask damages by FIBs of different ion species using a dynamic Monte Carlo simulation code, EDDY.

EDDY simulates the slowing down of an ion in the mask and the formation of recoil cascades leading to sputtering in the binary collision approximation. Three dimensional material changes in the mask arise from the deposition of implanted ions and the collisional mixing of implanted atoms and different material atoms. During implantation of the ion, EDDY is combined with an analysis of the Fickian equation that evaluates material changes due to the diffusion in the mask materials. In this simulation, The EUV mask consists of buffer layer (10-nm-thick CrN), capping layer (11-nm-thick Si), 40 pairs of 3-nm-thick Mo and 4-nm-thick Si film stack. It was irradiated with 30-keV H, Ne, He, and Ga ion beams up to a dose of 1016 ions/cm2, assuming the profile of Gaussian type with standard deviations of 1 nm, 3 nm, and 10 nm. The principle of the material changes is based on the assumption that each pseudo-projectile represents a differential dose of the ions and the surface layer is divided into many slabs of constant thickness. After ion bombardment, implantation, sputtering and atomic relocation cause removal or deposition of constituent atoms in different slabs. Local depletions or excess densities in each slab are allowed to relax by adjusting interval thickness. The incremental surface recession, or thickness increase, is calculated from the difference in integrated slab thickness before and after bombardment.

The most important result is that sputtering by a 30 keV Ga ion beam produced a deep hole in the mask surface, the interior of which looks exactly as the beam profile, and due to lateral relocation of the material atoms, the vicinity of the hole stood up above the surrounding. However,

due to much smaller energy transferred to the material atoms, such morphology changes were obtained much less for light ions, such as He and H. For irradiation with Ga and Ne ion beams, strong material mixing in the Mo/Si multilayers was obtained over their penetration depth in the mask. The Ga atomic density implanted in each layer is less than 1 % of the substrate material density. The material mixing with He and H ion beams was obtained only at the boundary between the layers, even for the highest dose.

9422-88, Session PSTue

Collector optic cleaning by in-situ hydrogen plasma

Daniel Elg, Shailendra N. Srivastava, David N. Ruzic, Univ. of Illinois at Urbana-Champaign (United States)

Extreme ultraviolet (EUV) lithography sources produce EUV photons by means of a hot, dense, highly-ionized Sn plasma. This plasma expels high-energy Sn ions and neutrals, which deposit on the collector optic used to focus the EUV light. This Sn deposition lowers the reflectivity of the collector optic, necessitating downtime for collector cleaning and replacement. A method is being developed to clean the collector with an in-situ hydrogen plasma, which provides hydrogen radicals that etch the Sn by forming gaseous SnH4. This method has the potential to significantly reduce collector-related source downtime. EUV reflectivity restoration and Sn cleaning have been demonstrated on multilayer mirror samples attached to an Sn-coated 300mm-diameter steel dummy collector driven at 300W RF power with 500sccm H2 and a pressure of 260mTorr. Use of the in-situ cleaning method is also being studied at industrially-applicable high pressure (1.3 Torr). Plasma creation across the dummy collector surface has been demonstrated at 1.3 Torr with 1000sccm H2 flow, and etch rates have been measured. Additionally, etching has been demonstrated at higher flow rates up to 3200sccm. A catalytic probe has been used to measure radical density at various pressures and flows. The results lend further credence to the hypothesis that Sn removal is limited not by radical creation but by the removal of SnH4 from the plasma. Additionally, further progress has been made in an attempt to model the physical processes behind Sn removal.

9422-90, Session PSTue

Simulation study of the impact of post exposure bake parameters on EUV resist LER and CDU

Suchit Bhattarai, Andrew R. Neureuther, Univ. of California, Berkeley (United States); Patrick P. Naulleau, Lawrence Berkeley National Lab. (United States)

Line edge roughness (LER) in chemically amplified positive tone EUV resists results predominantly from stochastic nature of processes that govern the translation of the aerial image into a chemical image, starting from photon absorption and followed by subsequent chemical processes such as acid generation, acid/base diffusion, acid/base annihilation, acid-catalyzed polymer deprotection, and reactions that govern the resist develop process. Understanding the role played by all of these chemistry parameters in determining the final LER can provide useful insights into the best strategies for tuning specific parameters to minimize resist LER. In this paper, we use a stochastic resist simulator to study the dependence of LER on the post exposure bake (PEB) reaction/diffusion parameters, e.g. acid/base annihilation rate, polymer deprotection rate, and acid/base diffusivity.

Preliminary simulation results are illustrated with a 50 nm half-pitch line/space aerial image with annular illumination and NA of 0.33. Assuming reasonable resist parameters, e.g. deprotection rate of 5 nm3/s, acid diffusion range of 10 nm and base diffusion range of 5 nm over a 90 s PEB time, LER at the end of PEB is found to decrease with increasing acid/base annihilation rate. This is explained by the fact that larger annihilation rate results in larger contrast in the acid image, which leads to a larger deprotection gradient at the line edge (defined at the position where 50% deprotection is reached). Increasing the acid/base annihilation rate from 5 nm3/s to 15 nm3/s causes the deprotection gradient to increase by 2x from 0.07/nm to 0.14/nm.

With a fixed acid/base annihilation rate, a larger deprotection rate results in larger LER. For acid/base annihilation rates larger than 10 nm3/s, degradation in the deprotection gradient with increasing deprotection rate closely explains the larger LER. For lower annihilation rates however, LER degradation with larger deprotection rate results from a lower incident photon count due to improved resist sensitivity associated with larger reactivity between acids and the polymer protected sites. With an acid/base annihilation rate of 10 nm3/s, 2x increase in the deprotection rate from 5 nm3/s to 10 nm3/s results in a 33% increase in LER, whereas with a larger annihilation rate, the sensitivity of LER to changes in deprotection rate decreases. We will also report on study of the sensitivity of LER on acid/base diffusivity, as well as the study of CD uniformity as a function of PEB parameters.

This research was supported by collaboration with the IMPACT+ program. This work was performed in part at Lawrence Berkeley National Laboratory which is operated under the auspices of the Director, Office of Science, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231.

9422-91, Session PSTue

Quickly identifying and resolving particle issues in photolithographic scanners

Allyn Jackson, CyberOptics Corp. (United States)

Stringent manufacturing requirements and the need to maximize both yields and tool uptimes in photolithographic scanner environments requires best-in-class practices for a contamination-free scanner process environment. Quickly identifying when and where airborne particles originate and the source of the contamination is challenging with traditional surface scan reticles, in-situ or hand-held methods. In addition, with these methods lacking real-time time-feedback, often “unexpected’ particle sources go undetected or take a long time to finally identify.

There are significant advantages of using the ReticleSense™ Particle Sensor in Photolithographic Scanners (APSR-Q) for quick particle qualification in Photo Lithography reticle environments. With all the necessary alignment and fiducial marks, APSR-Q can be loaded directly into a scanner just like a reticle and travel the entire reticle path to detect in real-time when and where particles are occurring in scanners. APSR-Q technology saves the time consuming task of partitioning with multiple surface scan reticles which require the high-value scanner to be brought off-line for lengthy particle source troubleshooting.

Specific, quantified results using the APSR-Q in terms of cost & time savings, reduction in manpower requirements and throughput will be highlighted.

9422-92, Session PSTue

LPP light source for actinic HVM mask inspection applications: progress in collected EUV brightness, stability, and cleanliness

Bob Rollinger, Nadia Gambino, Duane Hudgins, Alexander Sanders, Markus Brandstätter, Reza S. Abhari, ETH Zürich (Switzerland); Fariba Abreau, Adlyte Ltd. (Switzerland)

The next generation semiconductor devices with node sizes below 10 nm will be manufactured using extreme ultraviolet lithography (EUVL). EUV photons are generated from a Laser-Produced Plasma (LPP). The irradiation of tin droplets by a high power (kW) laser generates a plasma, which is highly emissive around 13.5 nm. This type of photon generation is today the base technology for high-volume manufacturing (HVM) lithography

light sources.. In addition to the application of EUV light sources in the scanner, sources with lower power levels, but high brightness and stability are required for actinic inspection applications. Examples are the Aerial Image Measurement System (AIMSTM) tool, as well as mask blank or pattern inspection tools. EUV lithography is only production ready, if these tools are available with HVM specifications.

At the Laboratory for Energy Conversion of the Swiss Federal Institute of Technology (ETH Zurich) prototype EUV sources for actinic inspection have been designed, built and tested over the last 8 years. The sources are based on micrometer-sized tin droplets that are irradiated by a high power (1.6 kW) Nd:YAG laser. Recent achievements on the latest prototype source ALPS II include a EUV emission pulse-to-pulse stability of 3% (?). This high pulse stability for a LPP source is a major criterion for the readiness of the source for HVM applications. Recently EUV collection optics and an intermediate focus (IF) module have been added to the source. Both modules are protected with the help of a gas-based debris mitigation system. The latest source performance results related to EUV emission and cleanliness after IF will be presented. The EUV output will be characterized in terms of power and beam characteristics at the IF. We also provide an update on source performance for our newly implemented droplet irradiation scheme. Details about the extension of the droplet generator operating time to 24/7, as well as the life-time management of the EUV collection optics will be also discussed in this presentation. Adlyte is in the process of commercializing the technology. An overall source roadmap will be presented.

9422-93, Session PSTue

Study of Dill's B parameter measurement of EUV resist

Atsushi Sekiguchi, Litho Tech Japan Co., Ltd. (Japan)

We did the research of the measurement of the simulation parameter of the EUV resist so far.

The development parameters[1]

The PEB parameters[2]

Dill's C parameters[3]

The quencher parameters[4]

It inputted these parameters to the lithography simulator and it did the simulation of the EUV resist.

As a result, it did the material of the EUV resist and the optimization of the process.

In this report, it developed the measuring method of the Dill's B parameter for EUV resist.

Dill's B parameter is related to the absorption of the resin of the resist and PAG.

It is an important parameter to evaluate the sensitivity of the resist.

The thin film of SiN into the EUV light. Therefore, it applies a resist to the thin film of SiN (200nm) and it measures transmissivity in the EUV light.

However, manufacturing for the thin SiN film substrate is difficult.

Also, it is difficult to coat a resist to good uniformly on the Si thin film

We report because we realized it and measured the Dill's B parameter of the EUV resist with different kind (Figuer-1).

Reference

[1] A. Sekiguchi: "Study of the simulation parameter for EUVL", Proc. of SPIE, Vol.7273(2009)

[2] A. Sekiguchi, and Y. Kono: "Study of De-protection reaction Analysis System for EUV Lithography", Proc. of SPIE, Vol.6923(2008)

[3] A. Sekiguchi, Y. Matsumoto, and J. J. Biafore: "Analysis of the generating action of the acid from PAG using acid sensitive dyes for EUV resist", Proc. of SPIE, Vol.8682(2013)

[4] A.Sekiguchi, and Y. Matsumoto:"Study of acid diffusion behaves from PAG by using top coat method" Proc. of SPIE, Vol.9051(2014)

9422-94, Session PSTue

Modeling of bispectral primary source for the EUV lithography

Alexsandr Grishkanich, National Research Univ. of Information Technologies, Mechanics and Optics (Russian Federation); Alexsandr Zhevlakov, National Research Univ. of Information Technologies, Mechanics and Optics (Russian Federation) and S.I. Vavilov State Optical Institute (Russian Federation); Sergey Kascheev, National Research Univ. of Information Technologies, Mechanics and Optics (Russian Federation); Ruben P. Seisyan, Ioffe Physical-Technical Institute (Russian Federation); Valentin Elizarov, Victor Bespalov, National Research Univ ITMO (Russian Federation)

The creation of high performance industrial lithography facilities with the technological standard of 10-20 nm is connected with realization of the resist irradiation modes with pulse repetition rate of 100 kHz. One of such mode perspective schemes is based on the primary laser source when it's radiation is converted to EUV region under the focusing it on the target and plasma forming. The greatest efficiency of EUV radiation generation is achieved under the two-pulse, bispectral target irradiation using a hybrid primary source containing a solid-state and ??2 lasers. Here, the solid state laser emits a pulse of relatively low power for the previous converter target heating and the plasma initiation. The main powerful ??2 laser pulse comes with a time delay. The advantages of such methods consist in the possibility of much lower power consumption and conserving at the same time the high efficiency of the laser radiation into the EUV.

The possibility of power consumption reducing in the channel of primary laser forming the main powerful pulse for the converter plasma irradiation is modeled on the example of using the nonlinear inorganic resists. The effect of a giant image contrast transfer in such resists under the silica plate increased irradiation intensity allows receiving a high resolution of the IC topology elements. The optical scheme of the converter irradiation two-pulse bispectral laser source is based on the master oscillator solid state laser, SRS conversion cascades and the ??2 amplifier.

The solid state laser in such primary source emitting low power pulse for the previous plasma heating serves at the same time as a pump source for the StRS converters series. The second Stokes component radiation coming from the last StRS converter with the wavelength of 10.6 ?m is injected into the ??2 amplifier input. The StRS converters in this case do not require of a power supply; their pumping is realized by the low power laser radiation and the first Stokes component converted from the wavelength of 1.06 ?m. Several rotational mirrors are set for the variation of the time delay between the previous pulse and the main pulse in the last StRS cell containing hydrogen.

9422-95, Session PSTue

Studying nanoparticle-surface interactions using low-pressure impactor and optimized scanning electron microscope imaging

Yashdeep Khopkar, Gregory Denbeaux, Univ. at Albany (United States)

Defectivity remains an issue in EUV mask blanks. Particles smaller than 50 nm can cause printable defects on the mask, thereby reducing the overall process yield. These particles can land on the surface during mask fabrication, storage or general usage. There is very little information available in literature to predict the interaction between a particle and a surface in the size regime of interest in vacuum. Optical particle counters and Laser Doppler Anemometry were previously used to study interactions between a particle and surface but they are limited by the smallest particle

size that can be detected. This limit is determined by the wavelength of light and detector used in the counter but is generally greater than 100 nm. We present a new method to study interactions between a nanoparticle and a surface, more specifically between 50 nm silicon dioxide particles and ruthenium coated surface using a low-pressure impactor. The surface is analyzed using scanning electron microscope (SEM) mapping process to find the fraction of particles captured by a surface at a particular particle impact velocity. This velocity can be tuned to help estimate the critical velocity at which the particles are completely captured on the surface. These results can be useful to design surfaces in vacuum systems that enhance capture of stray particles and help mitigate defectivity.

9422-96, Session PSTue

Experimental and simulation studies of printability of buried native EUV mask defects using a novel level-set multilayer growth model

Mihir Upadhyaya, SUNY College of Nanoscale Science and Engineering (United States); Vibhu Jindal, SEMATECH Inc. (United States); Adarsh Basavalingappa, Henry C. Herbol, SUNY College of Nanoscale Science and Engineering (United States); Il-Yong Jang, Jenah Harris-Jones, SEMATECH Inc. (United States); Kenneth A. Goldberg, Iacopo Mochi, Lawrence Berkeley National Lab. (United States); Sajan Marokkey, Synopsys, Inc. (United States); Wolfgang Demmerle, Synopsys GmbH (Germany); Gregory Denbeaux, SUNY College of Nanoscale Science and Engineering (United States)

Availability of defect-free masks is considered to be a critical issue for enabling extreme ultraviolet lithography (EUVL) as the next generation technology. Since completely defect-free masks will be hard to achieve, it is essential to have a good understanding of the printability of EUV mask defects. In this work, two native mask blank defects were characterized using atomic force microscopy (AFM) and cross-section transmission electron microscopy (TEM), and the defect printability of the characterized native mask defects was evaluated using simulations implementing the Finite-difference-time-domain (FDTD) and the Waveguide algorithms. The simulation results were compared with the through-focus aerial images obtained at the SEMATECH Actinic Inspection Tool (AIT) at Lawrence Berkeley National Lab (LBNL) for the characterized defects. There was good agreement between the through-focus simulation results and the AIT results. To model the Mo/Si multilayer growth over the native defects, which served as the input for the defect printability simulations, a level-set technique was used to predict the evolution of the multilayer disruption over the defect. Unlike other models that assume a constant flux of atoms (of materials to be deposited) coming from a single direction, this model took into account the direction and incident fluxes of the materials to be deposited, as well as the rotation of the mask substrate, to accurately simulate the actual deposition conditions existing inside the ion beam deposition tool. The modeled multilayer growth was compared with the cross-section TEM images through the given defects, and a good agreement was observed between them, thus giving us confidence in our growth model. Further, we developed an approximate, but robust method for investigating defect printability of arbitrarily-shaped native defects given the AFM defect profile on top of multilayer stack. Given the full-width-half-maximum (FWHM) and height of the defect, as obtained from top layer AFM, we were able to infer the bottom defect profile in terms of FWHM and height, through study of multiple native EUV mask defects. Native, gaussian and rectangular substrate defect profiles (having similar FWHM and heights) were compared for their printability performances, in terms of aerial image intensities, and reasonable comparison was obtained between them. Therefore, irrespective of the substrate defect shape, but having similar FWHM and height, we obtained comparable aerial image intensities. Thus, given an arbitrary defect profile on top of multilayer stack, we can reasonably determine its printability performance through simulations.

9422-97, Session PSTue

Calibration of system errors in lateral shearing interferometer for EUV-wavefront metrology

Jie Li, Feng Tang, Xiangzhao Wang, Fengzhao Dai, Feibin Wu, Shanghai Institute of Optics and Fine Mechanics (China)

New systematic error calibration method in lateral shearing interferometer is proposed for extreme ultraviolet (EUV) lithography. This method is used to remove the most significant errors: geometric optical path difference (OPD) and detector tilt error [1]. The difference fronts of 0th and ±1th order diffracted waves are used to reconstruct wavefront (Fig.1). The Zernike coefficients of reconstructed wavefront are used to calculate the distance of diffracted light converging point (d). The difference front of 0th and -1th order diffracted waves is mirrored and added to the difference front of 0th and +1th order diffracted waves (Fig.1). The sum is used to calculate detector tilt angle. The geometric OPD and detector-tilt induced systematic errors are removed based on the calculated d and detector tilt angle. Simulations and experiments (Fig.2) show that the root-mean-square (RMS) value of residual systematic error is smaller than 0.1nm. The proposed method can be used to measure accurately the aberration of EUV optics with large numerical aperture (NA 0.5) in lateral shearing interferometer.

9422-98, Session PSTue

Key components technology update of 100W HVM EUV source

Taku Yamazaki, Hakaru Mizoguchi, Hiroaki Nakarai, Tamotsu Abe, Yasufumi Kawasuji, Takeshi Okamoto, Hiroshi Tanaka, Yukio Watanabe, Tsukasa Hori, Takeshi Kodama, Yutaka Shiraishi, Shinji Okazaki, Takashi Saitou, Gigaphoton Inc. (Japan)

This paper introduces key components technology update of 100W HVM LPP-EUV (laser produced plasma extreme ultraviolet) source which enable sub-10nm critical layer patterning. This light source system is composed of several key components and each has its innovating, key and original technology. They are perfectly controlled and work harmoniously to produce stable plasma and provide high power EUV light in long term to the photolithography equipment. This paper describes the latest results obtained from our proto systems and test stand which support one 100 watt HVM LPP-EUV light source. Key components performance with experimental data and measurements are reported, such as high power short pulse CO2 drive laser, unique pre-pulse laser technology, very small droplet generation, magnetic debris mitigation, laser-droplet shooting control and etc.

9422-99, Session PSTue

13nm EUV free electron lasers for next generation photolithography: the critical importance of RF stability

Simon Keens, Bodo Fritsche, Carmen Hiltbrunner, Marcel Frei, Ampegon AG (Switzerland)

Moore's Law has, since 1965, correctly predicted progress in the field of microelectronics, with technological developments allowing for the doubling of transistor density approximately every two years. Recently, however, transistor density is approaching the physical limits of current technologies, partially due to diffraction phenomena limiting design resolution. As a result, the semiconductor industry is investigating use of extreme ultraviolet (EUV) light, with wavelengths of 13 nm, to reduce the size limit imposed by using longer wavelengths.

One source of EUV light uses a Free Electron Laser (FEL) system. This provides an extremely high intensity beam and the ability to tune the system to a specific wavelength. The output wavelength of an FEL is directly related to the input power of the electrons passing through the laser cavity from an electron gun/accelerator system. In reality, this power comes from electrons with is a finite distribution of energies around a mean value, with deviation caused by various factors, such as accelerator geometry, gun work function and, significantly, the amplifying RF power source stability and quality. The deviation of electron energies results in a distribution of photon energies and, since E = hf (Planck-Einstein relation), also of frequencies and wavelengths. Thus, in order to reduce the minimum size of features (apertures) in photolithography masks without causing diffraction effects, the distribution of photon energies must be minimised; this may be achieved by limiting distribution of electron energies. It follows that an RF power-source with high stability and RF quality, providing low dispersion of wavelengths offers better performance over less reliable RF sources which may result in undesirable diffraction effects if the same minimum aperture size, and thus maximum transistor density, is to be achieved.

Therefore, an important factor to achieve a high quality FEL for photolithography applications is the careful development of the amplifying RF system, designed with fully integrated, optimized and perfectly matched sub-systems. Consideration must be given to the amplification chain, from the digital low-level RF system up to the high power RF amplifier, incorporating low noise and high accuracy DC power supplies for solid state amplifiers, or high voltage modulators for klystron amplifiers. Understanding each individual sub-system is key to optimizing the EUV output of the FEL light source. Ampegon is constantly working to improve our RF systems, and therefore designs sub-systems specifically for individual applications, and develops critical sub-systems in-house. For lower RF power levels, highly modular and reliable solid state amplifiers up to 100kW CW RF power are available and offer improved performance. For power levels in the range of several 100kW up to megawatts, highly accurate and stable high voltage power supplies and modulators with a stability range of <20ppm have been developed. Our paper explains how such demanding goals can be fulfilled with solid state amplifier technology as well as with klystron amplifier technology, to meet the emerging EUV photolithography requirements of the semiconductor industry.

9422-32, Session 8

Best focus shift for thick masks

Martin Burkhardt, IBM Thomas J. Watson Research Ctr. (United States)

The best focus shift due to thick mask effects is well known, both in ArF, and more importantly in EUV, where the shorter wavelength is small compared to both mask openings and absorber height [krautschik2001,yan2002b]. The best focus shift is clearly visible when scattering bars are added to isolated non-dense features [burkhardt14]. This pattern dependent focus variation can be predicted in fast image calculations and used for optical proximity correction (OPC).

Even though this focus shift can be predicted and patterns can be corrected and even shifted for pattern placement, we would like to understand the mechanism that causes this focus shift. This can help us understand if, in addition to best focus shift, the image quality is further deteriorated due to the thick mask effects. For this, we investigate the complex values of the diffraction coefficients as suggested by Krautschik [krautschik2001]. The position of the diffraction orders is shown schematically on the left in Fig. 1, with three points of the right lower quasar element highlighted by color red, cyan, and green. The various diffraction orders then pick up a phase term according to the defocus value, as indicated by the approximate parabola on the right in Fig. 1. This defocus term then interacts and rotates the complex valued diffraction orders, as shown in Fig. 2, where we have set the phase of the 0th order to 0 for reference. In this diagram, we assume that the diffraction coefficients are constant for the three selected points in the illuminator pole indicate by red, cyan, and green. Highest contrast, and best focus, is typically reached when the image forming diffracted orders that interfere in the wafer plane have a complex angle of 0 or 180 degrees to each other. The defocus term rotates the diffraction coefficients in the complex plane, and depending on the location in the pupil and the magnitude of defocus we get a best focus that is different from a reference structure, such as an un-assisted trench.

We will present a visual and intuitive explanation for a qualitative evaluation of the best focus effects caused by the thick mask. krautschik2001:

C. G. Krautschik, M. Ito, I. Nishiyama, and K.~Otaki, "Impact of the EUV mask phase response on the asymmetry of Bossung curves as predicted by rigorous EUV mask simulations," Proc. SPIE 4343, pp. 392-401, 2001.

yan2002b: P.-Y. Yan, ``Understanding {B}ossung curve asymmetry and focus shift effect in EUV lithography," Proc. SPIE 4562, pp. 279-287, 2002.

burkhardt14: M. Burkhardt, G. McIntyre, R. Schlief, and L. Sun, ``Clear sub-resolution assist features for EUV," Extreme Ultraviolet (EUV) Lithography V 9048, pp. 904838-904838-7, SPIE, 2014.

9422-33, Session 8

Mitigation of image contrast loss due to mask-side non-telecentricity in an EUVL scanner

Shinn-Sheng Yu, Chih-Tsung Shih, Yen-Cheng Lu, Jack J. H. Chen, Anthony Yen, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

Due to the use of reflective optics in EUVL, the chief ray angle of incidence at the object (mask) side (CRAO) cannot be zero. This mask-side non-telecentricity reduces aerial image contrast, if off-axis illumination (OAI) is used. Generally, the incident beams are paired so that the two beams in each pair are symmetric with respect to the chief ray to avoid pattern shift when defocus. When OAI is optimized, the 0th and +1st or -1st diffraction orders resulting from each incident beam are also symmetric with respect to the chief ray. However, due to the non-zero CRAO, neither the two incident beams nor the two diffraction orders corresponding to each incident beam are symmetric with respect to the normal of the mask. There are two implications. First, since the reflectivity of the multilayer mirror depends sensitively on the angle of incidence, the intensities of the aerial images formed by the two incident beams are different. Second, for each incident beam, the corresponding two diffraction orders travel different absorber thickness, undergoing different amplitude attenuation and phase accumulation, thus generating an aerial image with I_Min≠0 (contrast loss) and I_Min laterally shifted in position. Since the positional shifts of I_Min of the aerial images formed by the two incident beams are different, their superposition leads to further contrast loss. The minimum achievable k_1 is at present limited to about 0.39, much higher than that achieved in optical lithography. Several methods can be employed to solve this problem. One of them is to fine tune the period of the multilayer mirror to reduce the imbalance in strength of the aerial images formed by the two incident beams. In this paper, we will propose a new mask structure to reduce the phase difference between different diffraction orders.

9422-34, Session 8

EUV telecentricity and shadowing errors in Monte Carlo simulations

Deniz Civay, Sudharshan Raghunathan, Vikrant Chauhan, Tuhin Guha Neogi, Lesley Smith, Jason Stephens, GLOBALFOUNDRIES Inc. (United States)

Monte Carlo simulations are used in the semiconductor industry to evaluate variability limits in design rule generation, commonly for interaction between different layers. The variability of the geometry analyzed is determined mainly by the lithography, process and OPC used. Monte Carlo methods for design rule evaluation can provide the requisite level of accuracy, and are suitable for two or more layer interactions because the variations on one can be assumed to be independent of variations on the other(s). The variability parameters and budget utilized in optical Monte

Carlo simulations is well-established. With the upcoming implementation of EUV lithography the variability budget will be impacted. EUV has an off-axis illumination angle that complicates the lithography process by causing telecentricity and shadowing errors. Telecentricity errors manifest as a printed feature being shifted relative to the design. The amount the feature is shifted is a function of the pattern density and design. Shadowing is caused by the 3D nature of the mask combined with EUV reflective mask technology. A shadow occurs at feature edges, where the source does not fully illuminate. Telecentricity and shadowing errors, although small at the 10nm node, will increase in relative size compared to the features printed beyond the 7nm node. Telecentricity and shadowing errors are complex in nature and can't be compensated for with a flat bias. These errors unique to EUV are incorporated into Monte Carlo simulations and evaluated against the standard cell design layers. The effect of these variability parameters is evaluated on critical 7nm node layout clips.

9422-35, Session 9

Analysis of EUV resist outgassing depended on the dosage

Eishi Shiobara, Isamu Takagi, Yukiko Kikuchi, Takeshi Sasami, Toru Fujimori, Shinya Minegishi, Soichi Inoue, EUVL Infrastructure Development Ctr., Inc. (Japan); Takeo Watanabe, Tetsuo Harada, Hiroo Kinoshita, Univ. of Hyogo (Japan)

The suppression of outgassing from the EUV resist is one of the most significant challenges to be addressed for realizing EUVL since the outgassing might be the main contributor to the contamination of the mirror optics in scanners which result in the reflectivity loss. The pragmatic outgas qualification utilizing the witness sample (WS) is becoming the general method to clarify pass/fail for commercially available resists. In this method, two kinds of the contaminations are evaluated. One is the cleanable contamination mainly consisted of hydrocarbon which can be removed by the hydrogen radical cleaning. Another is the non-cleanable contamination which remains on WS after the hydrogen radical cleaning. Also, there are two irradiation sources; the EUV light and electron beam (EB), for both the resist exposure and contamination deposition. The EB source system is preferable due to its high throughput. However, outgas qualification results between outgas test sites; especially cleanable contamination thickness, still have a large deviation. NIST has already reported that the wafer temperature during resist exposure was one of the root causes of the deviation [1]. The contamination thickness corrected by the temperature can reduce the deviation between outgas test sites well. However the temperature difference is not enough to explain the deviation. It is thought another causes still remain.

EUVL Infrastructure Development Center (EIDEC) was focused on the resist outgassing to realize high volume manufacturing by EUVL and has two outgassing evaluation systems. One is the outgas evaluation system by EUV light from the synchrotron radiation of NEWSUBARU in Japan and another is the EB-based evaluation system. In our previous study, the comparisons between EB-based outgas tester and that of EUV-based for both cleanable and non-cleanable contamination were evaluated using model resists. In our first results, the linear correlation of cleanable contamination between the EB-based and EUV-based evaluation system was obtained. In those experiments, we confirmed the proportional relationship between contamination thickness and exposure dose. However recently we found that there are some resists showing not proportional characteristics of contamination thickness to exposure dose. We will investigate details of the phenomenon and analyze its causes. The results will be presented and discussed.

This work is supported by New Energy and Industrial Technology Development Organization (NEDO).

9422-36, Session 9

First results of outgas resist family test and correlation between outgas specifications and EUV resist development

Yu-Jen Fan, SEMATECH Inc. (United States); Ken Maruyama, Ramakrishnan Ayothi, Takehiko Naruoka, JSR Micro, Inc. (United States); Tonmoy Chakraborty, Dominic Ashworth, SEMATECH Inc. (United States); Jun Sung Chun, SEMATECH/CNSE (United States); Cecilia A. Montgomery, Shih-Hui Jen, Mark Neisser, Kevin D. Cummings, SEMATECH Inc. (United States)

EUV resist development is still challenged by Resolution / Line-edge-roughness / Sensitivity trade-off and limited by the ASML NXE platform outgassing specification. The resist outgas cleanable contamination specification has been relaxed recently by ASML. In this paper, we discuss recent outgas testing results in relation to resist performance, and we describe the first results from outgas resist family testing using EUV resists that have shown proven imaging performance to improve the efficiency of outgas testing. In addition, dependency of film thickness and post exposure bake (PEB) temperature have been studied to further reduce the number of overall testing and meet outgassing requirements for high volume manufacturing (HVM).

The concept of family resist testing assumes that more photo acid generator (PAG), more protecting units, and more quencher will always lead to a higher contamination growth (CG), but we have found that this is not always the case. Witness sample based resist outgas testing results demonstrate multiple resist family tests where there is higher CG with lower PAG loading, even with the zero-PAG sample for research purpose only. That is, for these resist systems, adding more PAG suppresses resist outgassing, contrary to the assumptions guiding the resist family outgas test protocol. Based on current experimental results and fundamental study, the suggested boundary conditions would be: low-PAG, high protecting units, and high quencher for qualifying the outgas resist family test.

The performance of state of the art resists is described, including newer higher outgassing materials, negative tone development materials, nanoparticle materials, and metal based resists, are compared to previously demonstrated performance of chemically amplified resists and see if the relaxation of outgassing specification has helped the recent EUV resist development.

9422-37, Session 9

Collaborative work on reducing the inter-site gap of outgassing qualification

Soichi Inoue, Eishi Shiobara, Takeshi Sasami, Isamu Takagi, Yukiko Kikuchi, Toru Fujimori, Shinya Minegishi, EUVL Infrastructure Development Ctr., Inc. (Japan); Robert F. Berg, Thomas B. Lucatorto, Shannon B. Hill, Charles Tarrio, National Institute of Standards and Technology (United States); Ivan Pollentier, IMEC (Belgium); Yu-Jen Fan, Dominic Ashworth, SEMATECH Inc. (United States)

EUV resist outgassing qualification is one of the most significant challenges to be addressed for realizing EUV lithography. An effective qualification method is important as resist outgassing, which can be a main contributor to the contamination of the mirror optics in scanners, may result in reflectivity loss. The pragmatic outgassing qualification method utilizing a witness sample has become a defacto standard in clarifying a pass/fail for commercially available resists. The four institutions have played the role of test sites for multiple resist suppliers. Recently, they carried out the round-robin (RR) testing to compare the results among these test sites. It turned out there still remain non-trivial deviations of the contamination growth (CG) among test sites. This occurred even as each test site had

already been normalized to the EUV-only (on resist and witness sample) test site [1][2]. The relaxation of CG criteria has temporarily allowed such variations to be acceptable. However, the deviation is expected to remain a serious issue because resist suppliers will try to aim for optimization of their resists near this new specification, if it will mean better resist performance. A collaborative and intensive investigation among these sites on the root cause / reduction of such deviation is the obvious and straightforward approach in resolving the issue.

This paper reports on the all-out effort to reduce this inter-site gap in results obtained under the RR scheme. All test sites described above collaborated to find out the cause of such gap. NIST indicated the wafer temperature during exposure would impact on the amount of CG [3]. Moreover, post-RR discussions among these groups concluded that the difference in the degree of satisfaction for outgas-limited condition would be another primary root cause for such gap as well. For the former, EIDEC provided the wafer-shaped thermometer with wireless transmitting capability to measure the wafer temperature directly inter-site. For the latter, EIDEC provided the multiple model resists to clarify the difference in degree of satisfaction for outgas-limited condition. During the conference, preliminary data for the post RR discussion will be presented.

The team acknowledges ASML for the pro-active stance and technological cooperation in this collaborative work. This work is partially supported by New Energy and Industrial Technology Development Organization (NEDO).

Reference

[1] K. Petrillo et al., Presented at Oct 2013 IEUVI Resist TWG Meeting in Toyama (2013)

[2] J. Sohn et al., Presented at Feb 2014 IEUVI Resist TWG Meeting in San Jose (2014)

[3] H. Shannon et al., presented at SPIE Advanced Lithography 2014 (2014)

9422-38, Session 9

Polarization resolved measurements with the new EUV ellipsometer of PTB

Victor Soltwisch, Frank Scholze, Andreas Fischer, Christian Laubis, Christian Stadelhoff, Physikalisch-Technische Bundesanstalt (Germany); Albrecht Ullrich, Advanced Mask Technology Ctr. GmbH Co. KG (Germany)

After having developed metrology with synchrotron radiation at the storage rings BESSY I and BESSY II for more than 25 years [1], particularly also for the characterization of EUV optical components and detectors, PTB extended its capabilities for EUV metrology with respect to polarization resolved measurements, particularly in the spectral region around 13.5 nm.

With the development of larger numerical aperture optics for EUV and advanced illumination concepts for lithographic imaging, the polarization performance of the optical elements becomes ever more important. At PTB, we use monochromatized bending magnet radiation for the characterization of the optical elements because of the superior temporal stability and rapid tuneability of the wavelength. Thus the polarization of the radiation is almost linear, depending on the vertical beamline acceptance angle, and cannot be manipulated.

Therefore, we decided to equip the soft X-ray beamline which delivers particularly well collimated and highly linearly polarized radiation with a sample manipulator which allows freely setting the orientation of the plane of deflection. Thus we are able to characterize samples in any orientation with respect to the linear polarized direction. We additionally can add a linear polarization analyzer working with a Brewster reflector to analyze the state of polarization of the reflected beam.

We present first results on the polarization properties of EUV multilayer mirrors close to the Brewster angle where polarization selectivity up to several hundred is predicted from model calculations. We also present polarization resolved measurements of the EUV diffraction of absorber line patterns at EUV photomasks.

[1] B.Beckhoff, et al.; Phys. Status Solidi B 246, 1415-1434 (2009)

9422-39, Session 10

Measuring aberrations using EUV mask roughness

Rene A. Claus, Univ. of California, Berkeley (United States); Antoine J. Wojdyla, Markus P. Benk, Kenneth A. Goldberg, Lawrence Berkeley National Lab. (United States); Andrew R. Neureuther, Univ. of California, Berkeley (United States); Patrick P. Naulleau, Lawrence Berkeley National Lab. (United States); Laura Waller, Univ. of California, Berkeley (United States)

The behavior of roughness induced speckle through-focus shows noticeable signatures of the aberrations (see figure). We have a model that predicts the PSD of mask roughness induced speckle as a function of focus and aberrations [1] and are using this model to find the aberrations that best explain the measured speckle. Using SHARP [2], we take the average PSD of many measurements over a relatively small area of the camera and fit the model to that data to extract the aberrations that best explain the speckle assuming that the mask roughness is isotropic (which is confirmed by rotating the mask). This technique is able to measure the field varying wavefront aberrations without the need for a special sample mask and without sensitivity to stage drift. Such a method would enable any arbitrary mask to be used for in-situ monitoring of the inspection tool wavefront potentially improving the accuracy of defect dispositioning and printability estimation.

[1] R. A. Claus, A. R. Neureuther, P. P. Naulleau, “Mathematical model for calculating speckle contrast through focus,” SPIE Advanced Lithography 8679, (2013). doi: 10.1117/12.2012535

[2] K. A. Goldberg, I. Mochi, M. Benk, A. P. Allezy, et al. “Commissioning an EUV mask microscope for lithography generations reaching 8 nm,” SPIE Advanced Lithography 8679, (2013).

9422-40, Session 10

A method of image-based aberration metrology for EUVL tools

Zac Levinson, Rochester Institute of Technology (United States); Sudharshanan Raghunathan, Erik A. Verduijn, Obert R. Wood II, Pawitter J. Mangat, GLOBALFOUNDRIES Inc. (United States); Kenneth A. Goldberg, Markus P. Benk, Antoine J. Wojdyla, Lawrence Berkeley National Lab. (United States); Vicky Philipsen, Eric Hendrickx, IMEC (Belgium); Bruce W. Smith, Rochester Institute of Technology (United States)

For several lithography generations, pupil plane characterization has played a critical role in image process optimization. This continues into EUV lithography (EUVL) with an additional importance placed on the understanding of the influences and variations to aberration behavior during system operation. Optical interferometric methods have been shown to have sub-nanometer accuracy and are the de facto standard of aberration metrology. Such methods can be challenging to implement during tool use, especially where EUV wavelengths introduce additional constraints. In-situ EUVL aberration metrology is essential because imaging is inherently more sensitive to thermally-induced system drift than DUV lithography. We will present an approach to image-based EUV aberration metrology using binary mask targets, as seen in Figure 1, and iterative model-based solutions to extract an aberrated pupil function. The approach is enabled through previously developed modeling, fitting, and extraction algorithms. In this paper, we examine the flexibility and criticality of the method using two experimental case studies. The first is the characterization an ASML NXE:3100 exposure system using SEM image analysis for inverse solutions of pupil plane behavior. The second study is with the SEMATECH High-NA Actinic Reticle review Project (SHARP) at Lawrence Berkeley National

Laboratory, using the analysis of EUV mask microscope images formed on a CCD sensor. The expected sources of aberrations are different for each due to the differences in image formation in these tools. Despite these differences, we seek to extract the aberrated pupil function of the imaging system using a single algorithm. We will present improvements on previous results of primary aberration sensitivity below 0.04 wave, and show the importance of system use aberration monitoring. Higher aberration measurement accuracy is expected from SHARP due to the continuous grayscale images it produces.

9422-41, Session 10

Correlation of actinic blank inspection and experimental phase defect printability on NXE3x00 EUV scanner

Rik Jonckheere, IMEC (Belgium); Hidehiro Watanabe, EUVL Infrastructure Development Ctr., Inc. (Japan); Dieter Van den Heuvel, IMEC (Belgium); Osamu Suga, Noriaki Takagi, EUVL Infrastructure Development Ctr., Inc. (Japan)

Apart from printing particles added by handling, the major challenge of extreme ultraviolet (EUV) mask defectivity is the severe printability of defects of the multi-layer (ML) mirror on the mask, i.e., the so-called ML-defects, sometimes referred to as phase defects. Just nanometer high or deep local distortion of this ML mirror have very high probability to print, because they cause a local phase shift (scaling to one fourth of the wavelength). Dedicated blank inspection tools are available, of which the most established ones use visible or deep-UV light. EIDEC and its predecessor SELETE/MIRAI have been focusing on the development of actinic blank inspection (ABI), in which EUV light is used to find the ML-defects on the blank and reported on the progress and performance, mainly based on programmed defects.

An important step in deciding on the criterion to use for considering ABI-detected ML defects on a blank unacceptable, is to determine how these affect the obtained pattern on the printed wafer. EIDEC and imec have jointly correlated blank defect detection capability of the latest ABI tool in development at EIDEC to wafers printed on imec's NXE3100. The focus has been on native defects, not programmed defects. A mask, made on a blank inspected on ABI to best effort, was exposed on NXE3100. Printing ML-defects were identified by wafer inspection, with subsequent repeater analysis. Forward correlation of ABI detections to the printed wafer was also undertaken.

This paper will discuss the obtained results from the perspective of how to use ABI to assess which kind of native ML defects need to be avoided during blank fabrication. These would cause printing defects and yield limitations for EUV lithography if they are not overcome during the blank fabrication process, unless only other solutions such as compensation repair or pattern shift will be used to render residual blank defects non-printable. Also exposures on NXE3300 are planned to be included.

9422-42, Session 10

Phase measurements of EUV mask defects

Rene A. Claus, Univ. of California, Berkeley (United States); Antoine J. Wojdyla, Markus P. Benk, Kenneth A. Goldberg, Lawrence Berkeley National Lab. (United States); Andrew R. Neureuther, Univ. of California, Berkeley (United States); Patrick P. Naulleau, Lawrence Berkeley National Lab. (United States); Laura Waller, Univ. of California, Berkeley (United States)

Multilayer defects are one of the key problems for EUV. Particles, pits, or bumps on the substrate or in the multilayer will propagate through the stack and result in a phase shift. AFM is typically used to measure the height and width of these bumps and they are then modeled to determine their likely phase. Knowing the phase of these defects is critical to determining printability, performing repairs and covering the defect by pattern shift.

We are using SHARP, an actinic EUV microscope [1] at Lawrence Berkeley National Lab, to measure the through-focus behavior of native and programmed defects on an un-patterned mask blank. We then apply the Transport of Intensity Equation [2] to extract the phase and amplitude from these images. By comparing the shape of the phase bump to the AFM measurement we will be able to show how accurate AFM is at predicting the imaging effect of the defect.

[1] K. A. Goldberg, I. Mochi, M. Benk, A. P. Allezy, et al. "Commissioning an EUV mask microscope for lithography generations reaching 8 nm," SPIE Advanced Lithography 8679, (2013).

[2] M. R. Teague, "Deterministic phase retrieval: a green's function solution," J. Opt. Soc. Am. 73, pp. 1434-1441, Nov 1983.

9422-43, Session 10

Application of transport of intensity equation in EUV multilayer defect analysis

Dongbo Xu, Peter Evanschitzky, Andreas Erdmann, Fraunhofer-Institut für Integrierte Systeme und Bauelementetechnologie IISB (Germany)

The fabrication of EUV masks cannot avoid small multilayer defects. Several methods and various types of equipment are presently under development for defect detection and characterization. One of the key challenges is the extraction of relevant defect parameters from measured optical, EUV, SEM or AFM images and to use them to characterize the printing behavior of the defect and to derive appropriate repair parameters. In this paper, a new method for characterization of multilayer defects based on measured EUV projection images at different focus positions is proposed.

Figure 1 shows a mask with a typical multilayer defect and the corresponding aerial image in the nominal focus plane. The defect causes an intensity loss in the defect area. In general, multilayer defects are mixed amplitude and phase objects with an asymmetric through-focus printing behavior. In order to retrieve the phase characteristics of the defect, the Transport of Intensity Equation (TIE) is applied to several simulated aerial images at different focus positions. Besides being simple, the TIE method achieves a phase accuracy equivalent to that of interferometric methods, but it is much less sensitive to the coherence of the illumination. However, recovering phase (and amplitude) from a series of defocused images is a nonlinear problem because the aerial image is bilinear with phase and amplitude. A higher order TIE is used to consider this nonlinearity. This higher order TIE applies polynomial fitting on an equidistant grid of intensity values at different focus positions. Afterwards, it extracts the first order derivative and employs the standard TIE equation to extract the phase values at the specified grid. In the paper, we focus on the effect of defect parameters (defect top height, defect top width and defect bottom size) on the phase and intensity of the reflected light. The impact of optical system parameters such as illumination shape and NA on the extracted phase is investigated. The extracted phase is fitted by analytical functions, e.g. a simple Gaussian. A characteristic amplitude and width of the phase deformation is calculated. In addition to the previously used intensity loss caused by the defect, the Gaussian parameters of the extracted phase provide important parameters, which determine the printing behavior of the defect. The described parameters are analyzed for different types of defects and defect parameters. The relationship between these optical parameters and geometrical multilayer defect parameters is investigated. The combination of the extracted phase and intensity characteristics provides a promising method for the reconstruction of geometrical multilayer defect parameters. Finally, the method is used to retrieve the phase of a multilayer defect in the vicinity of an absorber pattern. All simulations are done with the lithography and imaging simulator Dr.LiTHO.

Conference 9422:
Extreme Ultraviolet (EUV) Lithography VI

9422-44, Session 11

Actinic Review of EUV masks: Status and recent results of the AIMS EUV system *(Invited Paper)*

Dirk Hellweg, Markus R. Weiss, Carl Zeiss SMT GmbH (Germany); Sascha Perlitz, Jan Hendrik Peters, Anthony D. Garetto, Carl Zeiss SMS GmbH (Germany); Vibhu Jindal, SEMATECH Inc. (United States)

The EUV mask infrastructure is of key importance for the successful introduction of EUV lithography into volume production. In particular, for the production of defect free masks, actinic review of potential defect sites is required. With such a review it can be decided if a defect prints, i.e. if it needs to be repaired or compensated. It also serves as verification for the repair or compensation with the Merit™ electron beam repair tool, thereby providing a closed loop mask repair solution. To realize such an actinic review tool, Carl Zeiss and the SEMATECH EUVL Mask Infrastructure consortium started a development program for an EUV aerial image metrology system, the AIMS™ EUV, with realization of a prototype tool. After first tests early 2014 the prototype was updated to meet production needs. The delivery of the first customer tool is planned for the first half of 2015. The AIMS™ EUV concept and its feasibility haves been discussed in previous years at SPIE Advanced Lithography conferences. In this paper, we discuss the current status of the prototype integration and show recent results.

9422-45, Session 11

New ways of looking at masks with the SHARP EUV microscope

Kenneth A. Goldberg, Markus P. Benk, Antoine J. Wojdyla, Patrick P. Naulleau, Weilun L. Chao, David G. Johnson, Alexander P. Donoghue, Ryan H. Miyakawa, Yow-Gwo Wang, James B. Macdougall, Lawrence Berkeley National Lab. (United States)

Extended capabilities in source definition, additional imaging modes, and data analysis methods have enhanced the mask-imaging and process-investigation capabilities available to users of the SHARP EUV mask microscope.

SHARP (The SEMATECH High Numerical Aperture Actinic Reticle Review Project) is a synchrotron-based extreme ultraviolet (EUV) microscope dedicated to photomask research and described in several previous papers [1, 2, 3, 4]. Operational since mid-2013, SHARP is designed to emulate the illumination and imaging conditions of a wide-variety of current and future EUV projection lithography scanners. SHARP's lossless Fourier-synthesis illuminator can be programmed to adjust the illumination partial coherence at the touch of a button, producing arbitrary angular source spectra, including disk, annular, Quasar, dipole, cross-pole, and others. SHARP now contains three objective-lens arrays with nearly 200, electron-beam fabricated, high-magnification Fresnel zone plate lenses. The conventional, mask-side numerical aperture (NA) values vary from 0.025 up to 0.15625 (equivalent to 0.1 to 0.625 4xNA). Specific lenses with 0.25 and 0.33 4xNA values are matched to the Alpha Demo Tool and NXE 3100/3300 tools from ASML.

SHARP is routinely used to investigate mask architecture, materials and pattern properties; defects and repair strategies; surface and pattern roughness; and more. Up until this time, the focus of SHARP's work was solely to reproduce the conditions of wafer printing tools—that no longer needs to be the case. Ongoing development of SHARP has concentrated on three areas: lenses, source configurations, and data analysis, all designed to extract additional quantitative information from mask imaging.

The fact that SHARP's lenses are defined as holographic elements, and are fabricated according to mathematical formulas, enables us to customize the imaging properties of new lenses to include such properties as differential interference contrast, Zernike phase contrast, stereoscopic imaging, and other capabilities (see Figures 1 and 2).

Lithographic developments in the area of source-mask optimization (SMO) have inspired us to introduce arbitrary, pixelated source angular spectra to SHARP, emulating faceted illumination in EUVL scanners and enabling the study of image formation under illumination conditions obtained from source-mask optimization (SMO).

Finally, the extraction of quantitative phase information from EUV mask imaging is a key element in improving our understanding of defects and repair efforts. We have several ongoing efforts in phase imaging, including both computational and direct evaluation of the complex electric field amplitude reflected from the mask surface point by point.

This work is funded by SEMATECH, and performed by University of California Lawrence Berkeley National Laboratory under the auspices of the U.S. Department of Energy, Contract No. DE-AC02-05CH11231.

9422-46, Session 11

SEMATECH produces defect-free EUV mask blanks: defect yield and immediate challenges

Alin O. Antohe, Dave Balachandran, SEMATECH Inc. (United States); Long He, Intel Corp. (United States); Patrick A. Kearney, Anil Karumuri, Frank Goodwin, Kevin D. Cummings, SEMATECH Inc. (United States); Onoue Takahiro, Hoya Japan (Japan); Alan Hayes, Veeco Instruments Inc. (United States)

Availability of defect-free reflective mask has been one of the most critical challenges to extreme ultraviolet lithography (EUVL). To mitigate the risk, significant progress has been made on defect detection, pattern shifting, and defect repair. Clearly, such mitigation strategies are based on the assumption that defect counts and sizes from incoming mask blanks must be below practical levels depending on mask specifics. The leading industry consensus for early mask product development is that there should be no defects greater than 80 nm in the quality area, 132 mm x 132 mm. In addition less than 10 defects smaller than 80 nm may be mitigable. SEMATECH has been focused on EUV mask blank defect reduction using Veeco NexusTM IBD platform, the industry standard for mask blank production, and assessing if IBD technology can be evolved to a manufacturing solution.

SEMATECH has recently announced a breakthrough reduction of defects in the mask blank deposition process resulting in the production of two defect-free EUV mask blanks at 54 nm inspection sensitivity (SiO2 equivalent). The paper will discuss the dramatic reduction of baseline EUV mask blank defects, review the current deposition process run and compare results with previous process runs. Likely causes of remaining defects will be discussed based on analyses as characterized by their compositions and whether defects are embedded in the multilayer stack or no-embedded.

9422-47, Session 11

Demonstration of enhanced defect sensitivity at focus for EUV mask inspection using SHARP EUV microscope

Yow-Gwo Wang, Lawrence Berkeley National Lab. (United States) and Univ. of California, Berkeley (United States); Ryan Miyakawa, Weilun L. Chao, Markus P. Benk, Antoine J. Wojdyla, Alex P. Donoghue, David G. Johnson, Kenneth Goldberg, Lawrence Berkeley National Lab. (United States); Andrew R. Neureuther, Lawrence Berkeley National Lab. (United States) and Univ. of California, Berkeley (United States); Ted Liang, Intel Corp. (United States); Patrick P. Naulleau, Lawrence Berkeley National

Lab. (United States)

In EUV mask fabrication process flow, ML blank inspection is an important step to qualify the blanks before absorber deposition. Two methods are generally utilized to detect signal from a ML defect: scattering in a dark field (DF) or imaging in a bright field (BF). ML phase defect in general exhibits lower signal when imaged in-focus under a conventional BF microscope. Signals are higher in defocus, but the blank will need to be scanned multiple times in an inspection tool. The Zernike phase contrast (ZPC) method can achieve in-focus sensitivity to phase defects. This can significantly improve the efficiency of EUV mask inspection process. Moreover, additional pupil plane appodization can further improve defect signal-to-noise due to mitigation of speckle noise from the surface roughness on the EUV mask.

To implement the Zernike phase shift method, we use specially designed zoneplates that have recently been fabricated and installed into SEMATECH Berkeley mask inspection microscope SHARP. For our experiment, the Fresnel zoneplates is fabricated by electron-beam lithography with a diameter about 100 um, and the 4xNA is at 0.33. To encode the phase shift and apodization features on the zoneplate, we modify the position of specific zones to match the illumination condition and control the angular duty cycle to manage the transmission of light.

As previously reported, we have investigated ZPC method mostly by comprehensive simulations with limited experimental data. In this paper, we present extensive experimental results using a programmed defect test mask and directly compare the Zernike phase contrast method to the conventional bright and dark-field inspection methods and. The test mask contains well-characterized ML phase defects of a wide range of sizes. We present results for isolated ML phase defects with height ranging from about -1nm to +2nm that were grew from substrate defects ranging from 40 nm to 60 nm. Moreover, we show results for proximity defects ranging from 40 nm on the substrate to 75 nm. The detection results are correlated against AFM characterization of the multilayer bump heights for each of the substrate defects. The experimental data clearly show that ZPC method increases phase defect signal strength and improves the signal to noise ratio relative to multilayer roughness.

9422-48, Session 11

Toward defect guard-banding of EUV exposures by full chip optical wafer inspection of EUV mask defect adders

Scott D. Halle, Luciana Meli, Robert Delancey, IBM Corp. (United States); Kaushik Vemareddy, KLA-Tencor California (United States); Gary Crispo, KLA-Tencor New York (United States); Ravi K. Bonam, Daniel Corliss, IBM Corp. (United States)

The risk of EUV mask defect adders resulting in chip repeating defects on wafers continues to be a key challenge for wide adoption of EUV into production fabs. To ensure that EUV exposed wafers are “free” of EUV Mask Adder Printable Defects (MAPS), there is a need for full wafer/chip inspection at production worthy inspection times. While eBeam die to data inspection techniques1 have demonstrated sensitivity to detectable MAPS, rapid optical defect inspection methods with sufficient detection sensitivity would be strongly desired. The detection sensitivity of an optical defect inspection tool configured as a Die To “golden-wafer” Virtual Die scheme (D2VD), has been used to examine 0.33NA EUV exposed programmed defect wafers. Investigation of both opaque and pin-dot type defects over a range of defect sizes, as shown in Figure 1 below, has yielded wafer defect detect sensitivities down to 10nm. The efficacy of this D2VD scheme to suppress both nuisance and random process defect as function of the optical tool detection threshold is shown to be a powerful methodology. Sensitivity of detection to tool parameters such as: chip sampling requirements by defect size and type, detection thresholds, repeater search range, and filtering and illumination modes have been explored. The challenges of full chip EUV MAPS are also addressed.

This work was performed by the Research and Development Alliance Teams at various IBM Research and Development Facilities.

1 S. Halle et al., “E-beam defect inspection of EUV reticles and wafers” SPIE 2013 and R. Bonam et al.,” E-beam inspection of EUV programmed defect wafers for printability analysis” ASMC 2014.

9422-49, Session 11

Application of differential phase contrast imaging to EUV mask inspection: a numerical study

Xibin Zhou, Dominic Ashworth, Kevin D. Cummings, SEMATECH Inc. (United States)

Since photoresists are primarily sensitive to light intensity, actinic EUV mask inspection tools such as AIMS or SHARP measure the intensity distribution of light at image formation planes. However, in situations such as studying the phase jumps associated with absorber edges, inspecting phase defects formed by embedded particles under Si/Mo multilayers, or developing phase shifting EUV masks for resolution enhancements, direct phase measurements could benefit our understanding of the masks under investigation.

To date, all proposed or demonstrated methods for actinic phase characterizations of EUV mask require either sophisticated optics, such as specially designed zone plates (Zernike phase contrast microscopy) [1] and EUV beam splitters (interference microscopy) [2], or numerical phase reconstructions from multiple images of a through-focus series [3].

Asymmetric illumination based on differential phase contrast imaging had long been known as an effective method to enhance contrasts for unstained transparent biological samples, even before Zernike invented the phase contrast mechanism bearing his name. Here we demonstrate numerically that it could be used for phase characterization of EUV mask, providing enhanced contrasts, extended depth-of-focus, and quantitative phase measurements.

In Fig. 1(a) and 2(a), through-focus aerial images of a square phase defect (100 nm in width and 0.2 nm in height, all in wafer dimensions with 4x demagnification) were simulated with Kirchhoff thin mask model in PROLITH. The differences between aerial images shown in Fig. 1(a) and Fig. 2(a) are due to different illumination settings used – full and asymmetric half annular illuminations respectively as shown in Fig. 1(b) and 2(b). The contrasts extracted from these images for both illumination settings are plotted in Fig. 3. In the case of annular illumination, the contrast is minimized at the best focus, increases towards defocus locations and peaks around 200 nm of defocus. When asymmetric half-annular illumination is used, the contrast is improved across focus including at the focal plane. As shown in Fig. 2 (c), the phase gradients at the top and bottom edges of the phase defect are clearly visible in the aerial image at focus. It is then possible to obtain the resolution-limited phase profile of the defect by a simple integration.

The scheme described above can be easily tested and integrated in both full field (AIMS or SHARP) and scanning mask inspection tools using segmented photodetectors. In addition to defect inspection, it also provides opportunities for quantitative studies of phase shifting EUV masks and phase jumps at absorber edges of regular EUV masks.

[1] Wang, Y.-G., Miyakawa, R., Neureuther, A., Naulleau, P., “Zernike Phase Contrast Microscope for EUV mask inspection” Proc. SPIE 9048, 904810 (2014).

[2] Kazuhiro Hamamoto, Yuzuru Tanaka, Takahiro Yoshizumi, Yasuyuki Fukushima, Hideaki Shiotani, Noriyuki Sakaya, Morio Hosoya, Tsutomu Shoki, Takeo Watanabe and Hiroo Kinoshita “Phase Defect Observation Using a EUV Microscope” Proc. SPIE 6151, 615119 (2006).

[3] Mochi, I., Goldberg K.A., Xie, R., Yan, P., Yamazoe, K., “Quantitative evaluation of mask phase defects from through-focus EUV aerial images”, Proc. SPIE 7969, 79691X (2011)

Conference 9422:
Extreme Ultraviolet (EUV) Lithography VI

9422-50, Session 12

EUV lithography scanner for sub-8nm resolution *(Invited Paper)*

Jan B. P. van Schoot, Koen van Ingen Schenau, ASML Netherlands B.V. (Netherlands); Sascha Migura, Carl Zeiss SMT GmbH (Germany)

EUV lithography for resolution below 8 nm half pitch requires the numerical aperture (NA) of the projection lens to be significantly larger than the current state-of-the-art 0.33NA. In order to be economically viable, a throughput above 100 wafers per hour is needed.

As a result of the increased NA, the incidence angles of the light rays at the reticle increase significantly. Consequently the shadowing deteriorates the aerial image contrast to unacceptably low values.

The only solution to reduce the angular range at the reticle is to increase the magnification. Simulations show that we have to double the magnification to 8x in order to overcome the shadowing effects. Assuming the mask infrastructure will not change the form factor, this will inevitably lead to a field size that is a quarter of the field size of current 0.33NA step-and-scan systems. This will reduce the throughput of the high-NA scanner to a value significantly below 100 wafers per hour, unless additional measures are taken.

In this paper we will present the introduction of an anamorphic step and scan system, with which we can print fields that are half the size of the current full field. By increasing the transmission of the optics and by increasing the acceleration of the wafer- and reticle stage we can enable a throughput in excess of 150 wafers per hour, making this an economically viable lithography solution. We will show the simulated imaging behavior of such an anamorphic system, and will elaborate on the impact of this system on the rest of the lithographic ecosystem.

9422-51, Session 12

EUV lithography optics for sub-9nm resolution

Bernhard Kneer, Sascha Migura, Jens Timo Neumann, Winfried Kaiser, Carl Zeiss SMT GmbH (Germany); Jan B. P. van Schoot, ASML Netherlands B.V. (Netherlands)

EUV lithography for resolution below 9 nm requires the numerical aperture (NA) of the projection optics to be significantly larger than 0.45. For such high-NA, the current EUV projection optics configuration featuring 4x magnification, full field size and a 6'' reticle is not feasible anymore: The increased chief ray angle together with the higher NA at reticle lead to increased shadowing effects and hence unacceptable contrast loss and mask efficiency.

The only solution to reduce the angles at the reticle and hence the shadowing effects is to increase the magnification. For recovering contrast loss and mask efficiency, a magnification larger than ~6x is needed. Consequently, a trade-off between two extreme options emerges. The first option is to retain the 26 x 33 mm^2 full field (FF) at wafer. This would require a mask size >6'', that is currently not supported by the industry. The second option is to keep the 6'' mask size. This would lead to a smaller imaging field size, e.g. 13 x 16.5 mm^2 quarter field with 8x magnification, and, hence, to productivity loss and split fields.

In order to find the best solution in this trade-off, a direction dependent, so called anamorphic magnification of 4x / 8x enabling a half field (HF) of 26 x 16.5 mm^2 using a 6'' mask is a solution for optimized productivity and resolution.

We have performed detailed investigation of the imaging behavior of anamorphic optical systems. Generally, we have found very good imaging behavior of these designs. We will show that the image contrast for the horizontal lines is as good as for a 8x magnification, i.e. as good as it is with NA 0.33.

Finally, we will discuss the optical solutions for anamorphic high-NA lithography concerning the impact to the design as well as to the needed technology.

9422-52, Session 12

Imaging performance of EUV lithography optics configuration for sub-9nm resolution

Jens Timo Neumann, Matthias Rösch, Paul Gräupner, Sascha Migura, Bernhard Kneer, Winfried Kaiser, Carl Zeiss SMT GmbH (Germany); Koen van Ingen Schenau, ASML Netherlands B.V. (Netherlands)

EUV lithography for resolution below 9 nm requires the numerical aperture (NA) of the projection optics to be significantly larger than 0.45. For such high-NA, the current EUV projection optics configuration featuring 4x magnification, full field size, and a 6'' reticle is not feasible anymore: the increased chief ray angle at reticle leads to shadowing and hence unacceptable contrast loss.

Design solutions are available, and are presented at this conference, introducing a new optical configuration which restores simultaneously superior imaging performance and productivity. This new configuration employs anamorphic imaging, i.e., it utilizes different reduction ratios: in the folding direction of the optical column, the reduction ratio is increased to, e.g., 8X in order to allow for a small chief ray angle at reticle and hence control mask induced effects; in the orthogonal direction, where mask induced effects play a far less important role, a reduction ratio of 4X can be maintained. This paper provides a thorough evaluation of the imaging capabilities of such new optical configurations. We investigate the imaging properties of the new configurations by means of rigorous simulations of relevant and illustrative use cases, taking into account mask induced effects as well as characteristics of the optics. We compare the simulated imaging behavior to that of other, more traditional optics configurations, and show that the productivity gain of our new configurations is indeed obtained at excellent imaging performance.

9422-53, Session 12

EUV resolution enhancement techniques (RET) for k1s below 0.4

Stephen D. Hsu, Rafael C. Howell, Jianjun Jia, Hua-Yu Liu, Keith Gronlund, ASML Brion (United States); Steve Hansen, ASML US, Inc. (United States); Jörg Zimmermann, Carl Zeiss SMT GmbH (Germany)

Due to the exponential growth of mobile wireless devices, low-power logic chips continue to drive device scaling. To enable sub-10 nm device scaling at an affordable cost, there is a strong need for single exposure advanced lithography. Extreme ultraviolet lithography (EUVL) is one of the more promising candidates to support the design rules for sub-10 nm. The aggressive mobile device design rules continue to push the critical dimension (CD) and pitch and put very stringent demand on the lithography performance such as pattern placement control, image contrast, critical dimension uniformity (CDU), and line width roughness (LWR).

In this paper we report the latest advances in resolution enhancement techniques to address low k1 EUV challenges, specifically: optimization of pattern placement control, enhancement of through focus contrast, and reduction of photon stochastic impacts. We have developed an innovative source-mask optimization (SMO) [1] [2] to significantly reduce edge placement errors (EPE). Aggressive design rules using the state-of-the-art NA of 0.33 of the NXE:3300B and its successor tools can have imaging k1s below 0.4 which may stretch current process capabilities for single exposure high volume manufacturing (HVM). Burkhardt et al. reported in a previous study that inserting sub-resolution assist feature (SRAF) at semi-isolated

features introduces strong Bossung tilt and best focus shift and a general solution for random pitches is not apparent [3]. Kang observed the same issues and proposed to introduce spherical aberrations to correct these effects while having a global impact on the full-chip [4]. In this work we introduce a new methodology to apply SRAFs to improve contrast, reduce best focus shift, and improve process window. Initial results show a 37% process window improvement (Figure 1) for an aggressive low k1metal design. Finally, a significant EUV challenge is the line-edge-roughness (LER) and local CD uniformity (LCDU). Source power, photoresist, mask bias, and feature size all impact the stochastic effects that can result in large LER for low-k1 patterning. We incorporated both a new analytic and an empirical LER model in the SMO NXE platform to study how pupil, mask, and target co-optimization can reduce LCDU, and assessed the trade-offs to global CDU and scanner throughput (Figure 2).

We believe that these advanced EUV RET techniques can support imaging k1s below 0.4 and extend single exposure for with a NA of 0.33, as is used in the NXE:3300B and its successor tools.

9422-54, Session 12

Novel interferometric strategies for characterizing high-NA EUV optics

Ryan H. Miyakawa, Patrick P. Naulleau, Lawrence Berkeley National Lab. (United States)

As exposure tools move toward higher numerical apertures, characterizing and removing optical aberrations remains a key part of achieving resolution targets. Common-path approaches such as lateral shearing interferometry (LSI) have had success at moderate numerical apertures (NA ~ 0.3) [1]; however, these techniques run into several obstacles when applied at higher NA (NA > 0.4). Chief among these obstacles are systematic aberrations due to high incident angles on the diffraction grating, and non-planar Talbot surfaces that create regions of poor fringe contrast across the pupil. In this paper, we present two strategies for extending LSI to high numerical apertures. These strategies will be employed in the installation and alignment of the 0.5-NA SEMATECH Berkeley Microfield Exposure Tool (MET5).

The lateral shearing interferometer works by interfering laterally separated or "sheared" copies of a test wavefront. The resulting interference contains information about the wavefront derivative in the direction of the shear. Performing the measurement twice — in the x- and y-directions — gives derivatives in orthogonal directions which can be used to reconstruct the test wavefront. Fig. 1 illustrates two of the primary obstacles in performing LSI on high-NA optics. Fig. 1a shows that even with perfect grating alignment, a perfect optic will give lambda/10 rms waves of aberration at the edge of the pupil; grating tilts of 0.5 degrees will quadruple this error. Fig. 1b illustrates that at 0.5-NA, Talbot surfaces can no longer be approximated as planes, and thus there are no CCD positions that can measure high fringe contrast across the whole pupil simultaneously.

In this paper, we present two approaches that address these obstacles. The first method involves axial stitching of multiple planes through-z, and the second is the wavefront reconstruction via 2nd-harmonic analysis. In the axial stitching approach, multiple fringe patterns are collected while the diffraction grating is scanned in z. Each image will have a different region of high fringe contrast, corresponding to cross-sections of the image in Fig. 1b. These images are then stitched so that regions of high fringe contrast properly cover every part of the pupil.

The 2nd-harmonic analysis involves examining the interference between the +1 and -1 diffracted orders rather than the conventional 0/+1 interference. This "double-frequency" interference has the unique property that the zero-OPD fringe is stationary in Z. Although this mode of analysis is slightly more susceptible to noise, it is resistant to many of the systematic errors that plague the conventional mode of analysis.

9422-55, Session 12

Advanced coatings for next-generation lithography

Philipp Naujok, Sergiy Yulin, Norbert Kaiser, Andreas Tünnermann, Fraunhofer-Institut für Angewandte Optik und Feinmechanik (Germany)

The development of Mo/Si multilayer coatings with high reflective optical performance up to 70 % for EUVL application is close to saturation. Beyond EUV lithography (BEUV) at 6.X nm wavelength has a potential to extend EUVL beyond the 11 nm node [1]. The development of high-reflective coatings designed at the wavelength of 6.X nm is currently under intensive research in different labs [2, 3]. It is known that B - based multilayer mirrors provide the highest possible calculated peak reflectivity up to 80% near the boron-K absorption edge (at a wavelength of about 6.5 nm). Currently the highest reported experimental reflectivity of 57.3% @ 6.65 nm was achieved with LaN/B4C multilayer mirrors [2]. It is obvious that the insufficient reflectivity of the optics will be lowering the optical throughput of industrial lithography systems and thereby fundamentally obstructs a road for the possible application of this technology. To implement the B-based mirrors and to enable their industrial use, an experimental reflectivity of > 70% has to be achieved in near future.

The authors will present promising approaches to enhance the optical performance of B-based multilayer coatings due to the mitigation of common interface imperfections of multilayer structures. It will be proved that transition from conventional La/B4C to promising LaN/B4C [1] multilayer coatings leads to considerable improvement of reflective properties due to more perfect interfaces in the LaN/B4C multilayer stack. Maximum peak reflectivities of 58.1% and 66.2% at the wavelength of 6.65 nm have been experimentally achieved with LaN/B4C multilayer mirrors deposited with an industrial sputtering system and designed at the near-normal and grazing incidences, respectively. It should also be noted that the maximum experimental reflectivity of the conventional La/B4C mirrors was only 41.0%.

In addition, temporal and thermal stability of the studied mirrors in the temperature range of 100 - 500°C was investigated and will be discussed. Finally, different modern approaches including the introduction of ultrathin diffussion barriers into multilayer design [3] to reach the targeted reflectivity of 70% will be analyzed.

[1] Banine V. et al.: Next generation of EUV lithography: Challenges and opportunities: International Workshop on Extreme Ultraviolet Sources, Dublin, 2010.

[2] Makhotkin I.A. et al.: "Short period La/B and LaN/B multilayer mirrors for ~ 6.8 nm wavelength," Opt. Express 21(24), 1610–1619 (2013).

[3] Chkhalo N.I. et al.: "High performance La/B4C multilayer mirrors with barrier layers for the next generation lithography," Appl. Phys. Lett. 102(1), 011602 (2013).

9422-56, Session 13

The Patterning Center of Excellence (CoE): an evolving lithographic enablement model

M. Warren Montgomery, Jun Sung Chun, SUNY College of Nanoscale Science and Engineering (United States); Michael Liehr, Univ. at Albany (United States); Michael D. Tittnich, Albany NanoTech (United States)

As EUV lithography moves towards high volume manufacturing (HVM), a key need for the lithography materials makers is access to EUV photons and imaging.

The Resist Materials Development Center (RMDC) provided a solution path to materials companies by allowing the Resist and Materials companies to work together, in a consortium fashion, in order to address

the need for EUV photons. Thousands of wafers have been processed by the RMDC (leveraging the CNSE MET, CNSE Alpha Demo Tool and the Lawrence Berkeley MET) allowing many of the questions associated with EUV materials development to be answered. In this regard the activities associated with the RMDC are continuing.

As the major Integrated Device Manufacturers (IDMs) have purchased EUV scanners, Materials companies must provide scanner based test data. The RMDC has to evolve the RMDC into "The Patterning Center of Excellence (CoE)". The new CoE leverages the capability of the CNSE based Advanced Patterning with EUV capability of the RMDC to create and integrated lithography model which will allow materials companies to advance materials development in ways not previously possible. In this talk we will provide a status update of the center's progress and will show performance results for a number of model resists which has been evaluated in the center. Specifically, resolution and CD uniformity will be discussed for a number from various suppliers.

9422-57, Session 13

EUV mask cleans comparison of frontside and dual-sided concurrent cleaning

Lin L. Cheong, Louis M. Kindt, IBM Corp. (United States); Christina Turley, IBM (United States); Dusty Leonard, John M. Boyle, Applied Materials, Inc. (United States); Christopher F. Robinson, IBM Corp. (United States); Jed Rankin, IBM (United States); Daniel Corliss, IBM Corp. (United States)

This paper compares a frontside-only with a concurrent front and backside cleaning of EUV masks. A base recipe, capable of single sided cleaning, was modified to achieve concurrent front and backside cleaning of EUV masks. An EUV mask was cleaned using the base recipe 120x times with no detrimental impact in 13.5nm reflectivity. Surface roughness of the mask had negligible change and demonstrated no obvious signs of pitting. Cleaning cycles were separated by at least 8 hours to reproduce the use of the mask in normal conditions. After 125x cleans, XPS and STEM data from the mask confirm the presence of Ru layer remaining. This study will discuss the comparative performance of single frontside and concurrent front and backside cleans performance.

IBM's health of line EUV monitor masks were used as test vehicles for concurrent cleaning process evaluations. It was expected that different material surfaces would have different affinities for particle adhesion and accumulation. These EUV monitor masks contain regions of Ru-capped multilayer, TaBN absorber and CrN (on backside) that can be inspected by unpatterned optical inspection equipment. Masks with accumulated particles are sent for cleaning and subsequently inspected post cleaning. All masks were able to achieve cleanliness specifications for both the front and backside of the mask, in less than or equal to two cleaning cycles.

9422-58, Session 13

No more of Moore's Law: the high cost for dimensional scaling

Arindam Mallik, Julien Ryckaert, Abdelkarim Mercha, Diederik Verkest, Kurt G. Ronse, Aaron Thean, IMEC (Belgium)

Moore's Law (Moore's Observation) has been driving the progress in semiconductor technology for the past 50 years. The semiconductor industry is at a juncture where significant increase in manufacturing cost is foreseen to sustain the past trend of dimensional scaling. At N10 and N7 technology nodes, the industry is struggling to find a cost-effective technology solution. On the other hand, from a technology point of view, the relative slow ramp-up of alternative lithography technologies like EUVL and DSA pushes the industry to adopt a severely multi-patterning-based solution. Both of these technological transformations have a big impact on die yield and eventually die cost. This paper is aimed to analyze the impact on manufacturing cost to keep the Moore's law alive. Furthermore, we analyzed the impact of EUVL introduction on tackling the high cost of manufacturing.

The primary contribution of this paper are as follows:

1. We have evaluated the cost impact of 1D vs 2D BEOL designs for both N10 and N7 technology node. Traditionally, the Mx layers are laid out in a bi-directional manner to have a compact standard cell layout. The critical pitch needed for targeted dimensional scaling in N10 and N7 requires severe multi-patterning that impacts cost and yield. Another choice which entails a paradigm change in circuit design is to force a single orientation to the Mx layers. This allows the pitch to scale further down to 40nm keeping a double patterning technology. In this way SADP/SAQP technology can be used for Mx and reduces the variability due to overlay. However this patterning choice has strong implication on the design of standard cells that now need to be drawn with a unidirectional M1. It induces additional penalty due to the introduction of additional Mx layer to meet the routing density constraint. We evaluated and compared the cost of 2D vs 1D design in both N10 and N7 technology node. The results shown in the paper establishes the fact that by adopting to bi-directional EUVL patterning at N7, the die cost can be cut down by 20%.

2. A comprehensive analytical yield model is developed to capture the impact of multiple patterning and complex process steps in die level cost for N10 and N7. As shown in Figure 1(a), number of lithography masks seem to be increasing exponentially due to multi-patterned solutions for N10 and N7 node. We have formulated a model to analyze the impact of multi-patterning on the die yield. The developed model takes into account on the complexity of lithography mask, number of deposition, etch steps attached to each masks to evaluate the impact of every lithography mask on the over-all die yield. As shown in Figure 1(a), EUVL-based solutions for N7 helps us to reduce the number of masks significantly and subsequently improving the yield of a same-sized die by 5% (EUV_BLK) to 10% (EUV_Mx).

3. The development of alternative lithography technologies like EUVL naturally demands an answer to the cost impact to introduce such techniques at a die level. We have proposed two alternatives for EUVL introduction, estimated the impact on wafer cost. Furthermore, we have shown how introduction of EUV lithography can help to improve the yield of a die. Subsequently, the die cost can be reduced. Initial experiments reveal that the cost of a state-of-the-art die can be reduced by 38% by adopting an EUVL solution of acceptable throughput of 75 WPH as shown in Figure 1(b).

[1] Arindam Mallik, Julien Ryckaert, et al., "The economic impact of EUV lithography on critical process modules", SPIE Advanced Lithography, February 2014

9422-59, Session 13

Multi-stack extreme-ultraviolet pellicle with out-of-band reduction

Sung-Gyu Lee, Guk-Jin Kim, In-Seon Kim, Jinho Ahn, Jin-goo Park, Hye-Keun Oh, Hanyang Univ. (Korea, Republic of)

The EUV (Extreme-Ultraviolet) lithography is one of the best candidates among the next generation lithography technologies. In order to protect the mask from detects which cause the image deformation, the EUV pellicle was suggested and it should be very thin due to high absorption of EUV light. The mesh supported EUV pellicle was considered since a very thin EUV pellicle might have a problem of structural stability, however, it can lead to the image deformation caused by mesh structure. To overcome this problem, people investigated the multi-stack pellicle stacked by several thin films. The multi-stack pellicle has been fabricated by ASML using a poly-silicon and a silicon nitride.

We try to optimize the structure of multi-stack pellicle that shows and low OoB (out-of-band) transmission as well as high EUV transmission since the OoB radiation emitted by EUV source would make the image deformation

if it reaches to the wafer. We investigated various materials and their combinations.

The multi-stack pellicle is consist of core layer (placed at the center) and capping layers (placed at the top and bottom). We used poly-silicon as a core layer. The initial chosen thicknesses are 48 nm core layer, 3.8 nm top capping layer and 5 nm bottom capping layer, respectively, as used by ASML. The OoB radiation emitted by EUV source was checked at 193, 248, 365 and 436 nm.

Figure 1 and 2 shows the result of EUV transmission and OoB transmission, respectively. As can be seen in the figures, other materials with less OoB transmission would make better performance compared to known silicon nitride used by ASML.

9422-60, Session 14

Performance overview and outlook of EUV lithography systems

Alberto Pirati, Rudy Peeters, Daniel A. Smith, Sjoerd Lok, Arthur W. E. Minnaert, Martijn van Noordenburg, Jörg Mallmann, ASML Netherlands B.V. (Netherlands); Noreen Harned, ASML (United States); Judon Stoeldraijer, Christian Wagner, ASML Netherlands B.V. (Netherlands); David C. Brandt, ASML (United States); Nigel R. Farrar, ASML (United States); Daniel J. Brown, ASML (United States); Herman Boom, Hans Meiling, Ron Kool, ASML Netherlands B.V. (Netherlands)

Multiple NXE:3300B systems are operational at customer sites. NXE:3300B is ASML's third generation of EUV systems and the first one delivered with MOPA + Pre-pulse EUV source technology. Deployment of Pre-Pulse technology enabled to demonstrate productivity capability several times higher than that of NXE:3300B predecessor, the NXE:3100. Additional improvements in CO2 drive laser performance, EUV source Conversion Efficiency and optical transmission are being deployed to further increase productivity performance.

Overlay and Imaging performance in line with the requirements of 10nm logic devices have been demonstrated; Matched Machine overlay to ArF immersion below 4.0nm and full wafer CDU performance of less than 1.5nm are regularly achieved.

Using customized freeform pupils, process window and CDU improvement have been proven for the 10 and 7 nm nodes, while mask defectivity has been reduced by 10x in a year and the first full scale prototype pellicles have been manufactured.

In parallel, the first NXE:3350B, ASML's fourth generation EUV system, is being qualified.

This paper will present an overview of the current EUV performance and of the on-going developments in productivity, imaging, overlay and mask defectivity reduction.

9422-61, Session 14

Overlay and edge placement control strategies for the 7nm node using EUV and ArF lithography

Jan Mulkens, Daan Slotboom, Henry Megens, Michael Hanna, Richard J. F. van Haren, ASML Netherlands B.V. (Netherlands)

The development of the 7-nm logic nodes has started and EUV lithography is considered as major candidate for printing the critical layers. In the industry there are two design approaches debated: the random 2D layout design versus the regularized 1D design layout. Latter enables ArF/EUV complementary lithography in which the use of EUV lithography steps can be minimized, whereas the 2D design layout enables the smallest chip cell size by moving all critical layer steps to EUV. Next to cost per layer considerations, the achievable overlay and edge placement error (EPE) accuracy is also part of the equation. EPE refers to the relative displacement of the edges of two features from their target positions and especially when using complementary lithography method overlay comes into the equation of EPE. For this we developed an analytical method to calculate EPE including systematic and pseudo-random effects at a range of spatial frequencies.

In this paper we will compare the two patterning option methods for 10-nm and 7-nm logic devices, by constructing and evaluating the overlay and edge placement error (EPE) strategies and resulting error budgets. For the 1D design approach we discuss the patterning control spacer pitch division resulting in complex multi-layer alignment and EPE optimization strategies. Solutions include overlay and CD metrology based on angle resolved scatterometry, scanner actuator control to enable high order overlay corrections and computational lithography optimization to minimize imaging induced pattern placement errors of devices and metrology targets. We will use 10-nm node experimental data and extrapolate the error budgets towards the 7-nm technology node. The experimental data will be based on NXE:3300B and NXT:1970Ci exposure systems. The results will be compared to the 2D design alternative which is more straightforward using single expose patterning and EUV for all critical layers.

9422-62, Session 14

Development of a high-numerical aperture EUV lithography tool: the SEMATECH Berkeley MET5 Platform

Patrick P. Naulleau, Arnaud P. Allezy, Christopher Neil Anderson, Carl W. Cork, Paul E. Denham, Michael R. Dickinson, Geoff Gains, Eric M. Gullikson, Ryan H. Miyakawa, Senajith B. Rekawa, Will Thur, Daniel J. Zehm, Lawrence Berkeley National Lab. (United States); Regina Soufli, Lawrence Livermore National Lab. (United States); Matt Bjork, Mark Bremer, Luc Girard, Robert Kestner, John Kincade, Louis A. Marchetti, Zygo Corporation (United States); Russell Hudyma, Hyperion Development LLC (United States); Dominic Ashworth, Kevin D. Cummings, SEMATECH Inc. (United States)

Microfield exposure tools (METs) have played a crucial role in the development of EUV resists over the past decade. The current generation of METs with a numerical aperture (NA) of 0.3, are approaching the end of their useful lifetime due to strong progress in EUV resists over the years. In order to support future resist developments into the sub-16-nm regime, SEMATECH is executing a 0.5 NA MET development program. This program includes the development of a brand new exposure tool platform at Berkeley as well as a new cleanroom facility with a wafer track installed at the Advanced Light Source (ALS) synchrotron. The new tool and facility are being constructed at a separate location on the ALS floor, allowing the current MET to remain operational throughout the new tool integration process. As with the current MET, the new MET5 will harness the unique high brightness capabilities of the ALS to enable a lossless full programmable coherence illuminator. The lithography tool will also include integrated wavefront metrology capabilities using an in-situ EUV interferometer.

In this presentation, we provide a detailed overview of the new synchrotron beamline, tool platform and facility and an update on the status of the various components and the integration process. Figure 1 shows a photograph of the platform being assembled in the new cleanroom

9422-63, Session 14

Evaluation of EUV resist performance using interference lithography

Elizabeth Buitrago, Paul Scherrer Institut (Switzerland); Oktay Yildirim, ASML Netherlands B.V. (Netherlands); Michaela Vockenhuber, Paul Scherrer Institut (Switzerland); Coen Verspaget, Naoko Tsugama, Rik Hoefnagels, Gijsbert Rispens, ASML Netherlands B.V. (Netherlands); Yasin Ekinci, Paul Scherrer Institut (Switzerland)

Extreme ultraviolet lithography (EUVL) stands out as the most promising option for future technology nodes in the semiconductor industry.1 For its successful introduction into the extremely competitive and stringent high-volume manufacturing phase, EUV resist performance remains a challenge. Particularly, there is a trade-off relationship among the resolution (half-pitch, HP), sensitivity (dose), and line-edge roughness (LER) that can be achieved with EUV resists which ultimately hampers their performance and extendibility towards future nodes. Here, we report the performance of highly promising EUV resists that are evaluated by EUV interference lithography (EUV-IL) in the Swiss Light Source (SLS) synchrotron facility at the Paul Scherrer Institut (PSI).2 With EUV-IL, a mask with diffraction gratings is illuminated by a spatially coherent beam in the extreme ultraviolet (13.5nm) energy range. First order diffracted beams overlap at a distance from the mask where the interference pattern is created (periodic aerial image). The masks used here consist of HSQ (Hydrogen silsesquioxane) gratings fabricated on a 100-nm-thick nitride (Si3N4) membranes and a gold or nickel photonstop. EUV-IL, with a well-defined aerial image, is thus a simple yet powerful method to create high-resolution periodic nanostructures for the fast and accurate characterization of EUV lithography resists.3

In this study, several commercially relevant chemically-amplified resists (CARs) have been investigated with the aim to resolve patterns down to 11 nm HP. Though other non-CAR resists have been found to be able to achieve resolutions down to 7 nm, pattern collapse for aspect ratios above 1 for 11 nm HP and below have been found to be prevalent. Crucial parameters, such as critical dimension (CD) and line edge roughness have been evaluated as a function of dose, and the exposure latitudes (EL) were determined. Furthermore, we report on the performance of novel resists. For instance, polymeric resists incorporating heavy atoms increases the absorption of EUV light.4 Such resist platforms offer new pathways in order to increase the sensitivity of the EUV resists without compromising the resolution.

9422-64, Session 14

Method of accurately characterizing out-of-band light in an EUVL scanner

Shinn-Sheng Yu, Yen-Cheng Lu, Chih-Tsung Shih, Shang-Chieh Chien, Shu-Hao Chang, Hsiang-Yu Chou, Jui-Ching Wu, Tao-Ming Huang, Jack J. H. Chen, Anthony Yen, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

Unlike the excimer laser light source in optical lithography, the bandwidth of the current laser produced plasma source for EUV lithography (EUVL) is not as narrow as one would expect. Although the multilayer (ML) acts as an excellent spectral filter for EUV, it is not effective in the longer wavelength range such as DUV. Unfortunately, current mainstream EUV resists employ similar platforms as those used for DUV chemically amplified resists, and thus the impact of out-of-band (OOB) light can be prominent.

Previously, researchers at IMEC et al., by employing an EUV mask with aluminum absorber, estimated the amount of OOB light in an EUV scanner by comparing dose to clear of resist exposed using mask regions with and without the aluminum absorber (i.e., the ML region). The reason why aluminum absorber is chosen is that it doesn't reflect EUV light because its refractive index is close to 1. However, the OOB light reflected by the OOB test mask is not the same as that reflected by the production mask, which uses different absorber. Even if the relative reflectivity between the OOB test mask and production mask can be determined, it is not possible to calibrate back the total integrated resist response, e.g., a CD change, unless the resist response at each wavelength is measured.

To efficiently and accurately characterize the OOB light for a specific lithographic process on a specific scanner, we design a new test mask to reflect essentially the same OOB light as the production mask but hardly any EUV light. By utilizing the wide linear range of resist response, the contribution of OOB light can be accurately quantified. This provides valuable information for OPC modeling, resist development, and exposure tool improvement.

9422-65, Session 14

EUV mask particle adders during scanner exposure

Yoonsuk Hyun, SK Hynix, Inc. (Korea, Republic of)

As EUV reaches high volume manufacturing, scanner source power and reticle defectivity attract a lot of attention. EUV scanner source power and blank mask quality is improving steadily to satisfy semiconductor industry's needs. Even thought EUV pellicle is being actively investigated, it is very probable to expose EUV masks without EUV pellicle for some time. To secure clean EUV mask under pellicle-less lithography, EUV scanner cleanliness needs to meet the requirement of high volume manufacturing. In this paper, we will show the cleanliness of EUV scanners in view of mask particle adder during scanner exposure. From this we will find several tendencies of mask particle adders depending on environment of mask in scanner. Further we can categorize mask particle adders, which could show the possible causes of particle adders during scanner exposure.

9422-66, Session 14

Debris monitoring and minimization system for EUV sources

Arjen de Jong, Rene Jilisen, Mark A. van de Kerkhof, Arnold van Putten, ASML Netherlands B.V. (Netherlands)

In NXE laser-produced-plasma (LPP) light sources, extreme-ultra-violet (EUV) light is created by exciting tin with a laser. This tin is supplied in the form of small droplets that are hit by a pre-pulse and main pulse laser. The tin droplet is converted into plasma which emits the desired light wavelength. Under non-optimal conditions, tin debris fragments can be created that can contaminate the light source optics. The current presentation describes experiments with a novel metrology technique that can quantify debris in situ in the source. The results can be used to adjust and optimize the source settings to significantly reduce contamination and increase lifetime and availability.

A novel optical technique uses a pulsed double cavity laser at 532 nm with beam shaping optics that is fired at a synchronized time delay after the EUV burst. The light is converted to a thin light sheet that illuminates possible debris fragments in the direct region around the plasma. A dedicated double frame camera is positioned at an angle with respect to the light sheet and records the scattered 532nm photons. Images are processed using internally developed software tools.

Mie scattering theory is applied to convert the intensity of the incoming individual particles to a diameter estimation and the two frames are correlated with advanced particle tracking algorithms to capture the velocity and direction of each individual particle. Due to the fact that light intensity is used for particle sizing instead of resolving the edges of the particle itself, smaller individual particles down to a diameter of 100nm can be detected. The technique provides particle count, diameter, direction and velocity information.

This technique has successfully been applied on real NXE test sources. The methodology provides a significant improvement in debris quantification. On real sources it has proven to directly identify plasma conditions with

significant debris reduction. Furthermore, it has potential to correlate the plasma settings to lifetime estimations and thus can be used for both source optimization and design. We will present both the metrology and the achieved results.

9422-67, Session 14

Feasibility study on the impact of higher power EUV irradiation on key lithographic elements

Soichi Inoue, Shinji Mikami, Eishi Shiobara, Isamu Takagi, Hiroyuki Tanaka, EUVL Infrastructure Development Ctr., Inc. (Japan)

Gradual source enhancement is driving EUV lithography to move forward to the high volume manufacturing (HVM) phase in recent days. However, further challenges coming up during such phase should be addressed for realizing EUVL as an effective lithographic technology. The possible impact of pulsed EUV light with extremely higher power irradiation (from laser-produced plasma (LPP) source) on key lithographic elements such as resists, reticle and/or pellicle, etc. is one of the biggest concerns that need to be clarified as EUVL becomes an HVM technology.

As a general assumption resist outgassing/contamination amount and reticle/pellicle damage are proportional to the total dosage of the EUV light irradiation they receive. Previous studies have yielded very useful information, but the EUV source used were one or two orders low in power density (on the sample plane) compared to actual scanners1-4. Thus, at this time, no evidence has been reported if such results will hold true if ever higher-power pulsed EUV sources were applied.

EIDEC built a high power EUV irradiation tool (HPEUV) equipped with LPP source to investigate its possible effect on the aforementioned lithographic elements. This work reports on the feasibility study on the impact of higher power EUV irradiation on the key elements through the application of the HPEUV tool. The equipment consists of an LPP source with relay mirrors which facilitate the EUV irradiation on the sample plane. The LPP source has relatively lower power at intermediate focus (IF) compared to those utilized in presently available HVM EUV scanners. However, with fewer relay mirrors compared to these EUV scanners, sufficient EUV power density is emulated on the sample plane i.e. EUV power equivalent to what is expected in future HVM EUV scanners can be obtained. The basic design configuration and preliminary results of EUV irradiation tests performed will be presented during the conference.

This work is partially supported by Ministry of Economy, Trade, and Industry (METI) and New Energy and Industrial Technology Development Organization (NEDO).

References:

1. Bas Mertens et. al., “Optics contamination under pulsed EUV radiation,” 2nd International Symposium on Extreme Ultraviolet Lithography, 2003

2. Hans Meiling et. al., “First performance results of the ASML alpha demo tool,” Proc. of SPIE Vol. 6151, 615108-1, 2006

3. Shannon B. Hill et. al., “Limits to accelerated MLM lifetime testing; TiO2 in hydrocarbons and Ru in H2O,” IEUVI Optics contamination TWG, EUVL symposium, 2007

4. Takahiro Nakayama et. al., “Analysis of carbon deposition on multilayer mirrors by using two different beamlines,” Proc. of SPIE Vol. 7271, 72713P-1, 2009

Conference 9423: Alternative Lithographic Technologies VII

Monday - Thursday 23–26 February 2015

Part of Proceedings of SPIE Vol. 9423 Alternative Lithographic Technologies VII

9423-1, Session 1

Edge placement: foundation for Moore's Law extension *(Invited Paper)*

Yan A. Borodovsky, Intel Corp. (United States)

No Abstract Available

9423-2, Session 1

Imprint lithography for high-volume semiconductor manufacturing *(Keynote Presentation)*

Toshiaki Ikoma, Canon Inc. (Japan)

No Abstract Available

9423-3, Session 1

A direct comparison of directed self-assembly processes to an alternative lithographic process for patterning dense line-space arrays *(Invited Paper)*

Dan B. Millward, Micron Technology, Inc. (United States)

To accurately assess the prospects for block co-polymer directed self-assembly (BCP DSA) as a future manufacturing technique, its technical merits must be compared against the benchmarks set by current best known manufacturing methods using the same target pattern and the same wafer stack. Potential cost benefits alone are not a sufficient driver for change to BCP DSA patterning if other methods can demonstrably provide a higher quality pattern. This presentation will discuss the status of BCP DSA strategies for patterning line-space arrays relative to a proven manufacturing method, with defect density and line roughness as the figures of merit.

9423-4, Session 2

Implementation of templated DSA for via layer patterning at the 7nm node *(Invited Paper)*

Roel Gronheid, Jan Doise, Joost P. Bekaert, Boon Teik Chan, IMEC (Belgium); Germain L. Fenger, Mentor Graphics (Deutschland) GmbH (Belgium); Daisuke Fuchimoto, Hitachi High-Tech Science Corp. (Japan); Guanyang Lin, AZ Electronic Materials USA Corp. (United States); Mark H. Somervell, Tokyo Electron America, Inc. (United States); Julien Ryckaert, Geert Vandenberghe, IMEC (Belgium)

In recent years major advancements have been made in the directed self-assembly (DSA) of block copolymers (BCP). Insertion of DSA for IC fabrication is seriously considered for the 7nm node. At this node the DSA technology could alleviate costs for double patterning and limit the number of masks that would be required per layer. One of the most straightforward approaches for implementation would be for via patterning through templated DSA (grapho-epitaxy), since hole patterns are readily accessible through templated hole patterning of cylindrical phase BCP materials. A tentative process flow is given in the Figure below. Here the pre-pattern template is first patterned into a spin-on hardmask stack. After optimizing the surface properties of the template the desired hole patterns can be obtained.

For implementation of this approach to be implemented for 7nm node via patterning, not only the appropriate process flow needs to be available, but also appropriate metrology (including for pattern placement accuracy) and DSA-aware mask decomposition are required. In this paper the imec approach for 7nm node via patterning will be discussed.

9423-5, Session 2

DSA guiding pattern generation with immersion lithography

Yuansheng Ma, Mentor Graphics Corp. (United States)

Due to the natural healing effect of DSA, employing DSA for technology nodes 7nm and below has the potential to reduce one or two mask numbers by grouping the neighboring sub-resolution features and putting them on the same mask. Therefore, it may greatly reduce the manufacturing cost compared to traditional multiple patterning technoloy.

However, there are two fundamental challenges facing the enablement of DSA for technology node 7nm and below: the first is the phase transition which causes defects on wafer; the second is the DSA placement errors when there is no phase transition. The DSA placement error directly translates into the total overlay required for certain technology node. To reduce the defect density (or phase transition) with DSA, we have to ensure that the design is DSA-compliant.

For a DSA-compliant design, it is seen that the guiding pattern's shape for grapho-epitaxy DSA formation places significant role to overcome the above two constraints of DSA. There are two perspectives in terms of the guiding pattern shape control. One is related to whether the original desired guiding pattern is a practical optimal solution for the design target. To be a practical optimal guiding pattern, it means the mask is easy to achieve manufacturing pattern fidelity with traditional OPC methods. The other is about how well the process can control the imaging of the optimized guiding pattern. The better the guiding pattern is controlled, the less the random DSA placement errors, thus less burden on overlay control for a smaller node technology which is almost a bottleneck for shrinking.

Peanut-alike shape has been widely used as a type of guiding pattern to create DSA targets in pitches other than the di-block copolymer's natural pitch. The wish is that the design target can be achieved by increasing the modulation of peanut shape. However, it is difficult to achieve the desired modulation. The reasons are: First, the features which are grouped for DSA process are in sub-resolution region. If we use individual design target for OPC, then the process variation could be so large to a degree that it is impossible to control the DSA phases – causing more random defects or placement errors. Second, the desired width for modulation control needs to be so thin that it is hard to achieve with optical technology even if we use the post-synthesized feature for OPC. On the other hand, for an aggressive DSA-compliant design in natural pitch, it is often to see that peanut-alike guiding patterns are formed under certain process conditions; Figure 1 shows an example.

In this paper, we are going to present our study on the guiding pattern generation with IMEC's test cases for 7 nm. The source is expected to have been optimized based on a SMO study for DSA. The focus will be on the following perspectives: (1) How to group to generate the desired guiding pattern? (2) Given a desired peanut-alike guiding pattern shape, what OPC can do to help achieving it on wafer? What's the relationship between DSA feature placement error versus the tolerances with respect to a variety of OPC schemes such as conventional OPC, pxOPC and matrix OPC?

9423-6, Session 2

Customization and design of directed self-assembly using hybrid prepatterns

Joy Y. Cheng, Melia Tjio, Hoa Truong, IBM Research - Almaden (United States); Hsinyu Tsai, IBM Thomas J. Watson Research Ctr. (United States); Chi-Chun Liu, IBM Corp. (United States); Gurpreet Singh, Gregory S. Doerk, Charles T. Rettner, Markus Brink, Srinivasan Balakrishnan, IBM Research - Almaden (United States); Nelson M. Felix, IBM Corp. (United States) and IBM Research - Almaden (United States); Michael A. Guillorn, IBM Thomas J. Watson Research Ctr. (United States); Daniel P. Sanders, IBM Research - Almaden (United States)

The directed self-assembly (DSA) of block copolymers (BCPs) is a promising resolution enhancement technology to extend the patterning capability. Chemoepitaxy has been demonstrated to reliably generate dense grating and hexagonal arrays from a sparse chemical prepatterns. Many patterning applications demand complex customization of dense DSA patterns and recently the customizations of dense DSA arrays using a separate cut layer have been implemented in two different approaches: customization after DSA layer and customization before DSA layer. 'Cut-last' customization of 42nm pitch line-space DSA patterns after DSA with separate mask has been demonstrated (1). 'Cut first' schemes using buried customization levels under the DSA guiding layer have also been demonstrated. (2). However, as the pitch of DSA pattern become smaller, customization of DSA pattern becomes more challenging because of the tight overlay budget. To address this challenge, we introduced a self-aligned DSA customization process based on inorganic-organic hybrid prepatterns where the cut layer itself is the guiding layer for DSA (3).

The inorganic-organic hybrid prepattern provides a route to simultaneously direct and customize the self-assembly of block copolymers. The chemical contrast between organic and inorganic regions direct the global self-assembly of block copolymers, while the etch contrast between organic and inorganic regions offers self-aligned masks for customizing arrays of self-assembled block copolymer domains. This paper will cover process, performance, and design considerations of DSA on 193i-based hybrid prepatterns. Figure 1A and 1B show self-aligned single-line cut of 33 nm pitch line-space pattern and self-aligned two-line cut of 25 nm pitch line-space pattern based on 100 nm pitch hybrid prepattern defined by 193i lithography. This DSA customization scheme is evaluated over a range of basic constructs. Examples of construct evaluation are shown in Figure 1C. Combinations of the working constructs enable complex customization of dense line-space arrays. An example of two-dimensional customization of line-space arrays is shown in Figure 1D.

References:

1. C.-C. Liu, et. al. SPIE 9049, Alternative Lithographic Technologies VI, 904909 (2014).

2. S. Sayan, et. al. SPIE 9051, Advances in Patterning Materials and Processes XXXI, 90510M (2014).

3. G. Doerk, et. al. SPIE Proc. SPIE 8680, Alternative Lithographic Technologies V, 86800Y (2013)

9423-7, Session 2

Directed self-assembly on enhanced chemical patterns

Lei Wan, He Gao, Ricardo Ruiz, Thomas R. Albrecht, HGST (United States)

Directed self-assembly (DSA) on lithographically defined chemical patterns or topographic templates, termed as block copolymer lithography, is currently considered as a viable candidate for high density patterning with sub-lithographic resolution. Particularly, in microelectronics industry, DSA has become a distinct candidate to extend the 193 nm water immersion photolithography for sub-40-nm resolution. For the application of bit patterned media (BPM) in magnetic data storage industry, DSA on prepatterns defined by rotary e-beam lithography is the current approach for fabrication of nanoimprint templates. However, DSA is still not ready for microelectronics industrial fabrication in terms of defectivity and processing conditions. On the other hand, BPM application can tolerate much more defects, but demands more aggressive lithographic resolution. Besides the properties of block copolymer materials, successful DSA relies on precise control of the geometrical and chemical properties of the prepatterns. In this paper, we demonstrated a method to reduce defect density and relax processing conditions by manipulating the properties of chemical patterns.

Our final goal is to fabricate nanoimprint master templates containing rectangular bit cells with arbitrary bit-aspect-ratio, which can be realized by a double imprint process via the intersection of orthogonal line patterns imprinted from two independent submaster templates with circumferential lines or radial lines. The submaster templates are fabricated by directed self-assembly of lamellae-forming PS-b-PMMA on chemical patterns and subsequent pattern transfer. A state-of-art rotary e-beam tool is used to expose resist prepatterns with periodicities commensurate to the natural periods of lamellae-forming PS-b-PMMA block copolymers. DSA with density multiplication is carried out on chemical contrast patterns following the "LINE" flow.1 In this flow, a mat layer is first deposited on a substrate and then patterned by conventional lithography methods. A brush layer is selectively grafted in the interspatial area between the mat features to form chemical patterns. The geometrical and chemical properties of the chemical patterns need to be tightly controlled in order to obtain nearly perfect DSA. Here, the chemical patterns are alternating stripes of crosslinked polystyrene (XPS) and PS-r-PMMA-OH brush. One "ideal" chemical pattern should have a full pitch of 2, 3 or 4L0, contain continuous XPS stripes uniform width of 0.5 or 1.5L0, and be uniformly backfilled with PS-r-PMMA-OH brush with certain composition. DSA defects start to appear when the properties of chemical patterns deviate from the ideality. Defect-free DSA is still achievable while the deviation is within a range, referring as a processing window. For BCPs with sub-30-nm in full pitch, it becomes challenging to target the small processing window, which results in high defectivity and/or nondesired processing conditions. Therefore, a DSA process with a wider process window would solve these two main issues. Here, a unique process is carried out to enhance the chemical patterns, therefore nearly perfect DSA can be achieved with a much wider processing window.

1. C. C. Liu, E. Han, M. S. Onses, C. J. Thode, S. X. Ji, P. Gopalan and P. F. Nealey, Macromolecules 44 (7), 1876-1885 (2011).

9423-8, Session 2

Understanding of PS-b-PMMA directed self-assembly registration by phase segregation under laser-induced millisecond thermal annealing

Alan G. Jacobs, Cornell Univ. (United States); Byungki Jung, Intel Corp. (United States); Christopher K. Ober, Michael O. Thompson, Cornell Univ. (United States)

Directed self-assembly (DSA) of block copolymers has emerged as a likely candidate for bottom up lithography to enable patterning at dimensions below 20 nm. The PS-b-PMMA system has been extensively explored and has demonstrated the ability to register patterns to both chemical and physical features during thermal annealing at temperatures near 250 C in the minutes time frame. We have previously demonstrated the ability to extend polymer processing to substantially higher temperatures by limiting anneals to millisecond time frames by laser spike annealing (LSA). Utilizing LSA, we have also demonstrated remarkable improvements in DSA film defectivity by annealing near the order disorder transition (ODT) temperature (TODT). This effect is inherently different from a purely thermal anneal for longer times as performing a single LSA prior to a reference hot plate anneal improved defectivity greatly while LSA after the hot plate provided incremental improvements.

Defectivity improvements are hypothesized to be due to the development

of an initial seed alignment developed during LSA. Films annealed just below TODT exhibited the greatest improvement in defectivity going from 24% defective to <5% defective. At these temperatures, films experience greatly improved mobility while maintaining segregation allowing for preferential alignment to occur between the chemoepitaxy template and the block copolymer film. Understanding the process of order development and alignment to pre-patterned surfaces are of paramount importance to develop methods for reducing defectivity besides annealing longer.

To examine the segregation evolution in time and temperature, undirected PS-b-PMMA films were annealed using LSA and investigated by micro-beam grazing incidence small angle x-ray scattering (μGISAXS). By using a 20 ?m wide x-ray beam, structure was probed across ~1 mm wide LSA scans up to 700 C allowing for the precise characterization of film morphology at a wide range of temperatures while maintaining constant film parameters. Additionally, by utilizing multiple LSA scans at short dwells and comparing to a single long dwell scan, the effect of quench rate was decoupled from the time a peak temperature. The quench rate strongly modifies the amount of segregation occurring when the polymer more strongly phase segregates at lower temperature.

This data shows that full phase segregation occurs on millisecond timescales in this extended temperature regime and that even quenching from above the ODT at ~10^4 K/s allows some order to form showing the rapid progression of segregation relative to the large scale polymer motion required for defect annealing in DSA. This means that phase segregation is effectively decoupled from the standard hot plate anneal and the processing before the hot plate anneal can to a great extent determine the resulting film defectivity.

9423-9, Session 3

Device fabrication using nanoimprint lithography *(Invited Paper)*

Tatsuhiko Higashiki, Tetsuro Nakasugi, Takuya Kono, Sachiko Kobayashi, Toshiba Corp. (Japan)

No Abstract Available

9423-10, Session 3

Nanoimprint systems for high-volume semiconductor manufacturing

Kazunori Iwamoto, Canon Inc. (Japan)

Jet and Flash Imprint Lithography (J-FIL) has been in development for the past decade to meet the several requirements for semiconductor manufacturing. The technology is now ready for pilot production for semiconductor memory devices at 20nm and below, and offers very significant advantages over 193nm SAQP in terms of cost of ownership and design flexibility (lack of design rule restrictions).

This presentation will describe the progress Canon has made on overlay, throughput and defectivity and on the development of manufacturing ready lithography equipment for sub 20nm lithography.

9423-11, Session 3

Status of jet and flash imprint lithography process defects

S. V. Sreenivasan, Canon Nanotechnologies, Inc. (United States)

Nanoimprint lithography techniques are known to possess replication resolution below 5nm. A specific form of imprint lithography known as Jet and Flash ImprintTM Lithography (J-FILTM) has been developed for manufacturing advanced CMOS memory. A one step patterning at 15nm half-pitch can be achieved with J-FIL eliminating the need of complicated and expensive SAQP. In addition, patterns are not limited to repeating structures such as lines and spaces thereby leading to significant cost savings in patterning. J-FIL involves field-by-field inkjet deposition of a low viscosity resist fluid followed by imprinting with nano-scale precision overlay. A mask with a relief structure is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is separated from the substrate leaving a patterned resist on the substrate.

This presentation will discuss the status of process defectivity and mask life for J-FIL. The discussion will include printing partial fields at the edge of the wafers. Defect data including systematic defects associated with the liquid resist phase (prior to UV exposure) and solid resist phase (after UV curing and separation); and random defects caused by various types of particle and surface contaminants will be discussed. For the various defect types, root cause analysis and ongoing process improvements will be discussed. Also, since J-FIL is a patterning technique that lacks pellicles, mask life studies that look at added repeaters over multiple lots will be discussed. The use of mask replicas have been established and discussed in prior conferences. Data indicating the progress towards the addition of about 1 repeating defect adder per cm2 over 10 wafer lots will be presented.

9423-12, Session 3

HVM readiness of nanoimprint lithography templates: defects, CD, and overlay

Koji Ichimura, Kouji Yoshida, Saburo Harada, Takaharu Nagai, Masaaki Kurihara, Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan)

Nanoimprint lithography is gathering much attention as one of the most potential candidates for the next generation lithography for semiconductor. This technology needs almost no additional mask data preparation from design, simpler exposure system, and just single patterning process without any coat/develop truck, and has potential of cost effective patterning rather than very complex optical lithography and/or EUV lithography.

Replication of the EB written high quality master templates is proposed for the use of nanoimprint for the semiconductor lithography. Maintaining the quality of the master templates in replication process is very important. Nanoimprint technique is also used for the replication of the templates, and optimization of the nanoimprint process is very important as well as pattern transfer etching process after imprint.

Defect control is one of the concerns of template replication. Careful optimization of the nanoimprint process can reduce the defect density on the replicated templates. Critical dimension uniformity can be improved by improving the imprint uniformity. Overlay is of the interest for the next generation semiconductor lithography. Uncorrectable distortion of the nanoimprint template is needed to be as low as possible. Since the nanoimprint process is a kind of the physical contact process and may produce undesirable substrate distortion. Imprint process need to be carefully considered to reduce such distortions.

In this presentation, our recent improvement of the replicated template quality will be reported from the nanoimprint point of view.

9423-13, Session 4

Single-digit nanomanufacturing by electric-field scanning probe lithography on molecular resist *(Invited Paper)*

Marcus Kaestner, Yana Krivoshapkina, Matthias Budden, Steve Lenk, Tzvetan Ivanov, Technische Univ. Ilmenau (Germany); Christian Neuber, Hans-Werner Schmidt, Univ. Bayreuth (Germany); Ivo W. Rangelow, Technische Univ. Ilmenau (Germany)

The routine "on demand" fabrication of features smaller than 10 nm opens up new possibilities for realization of many novel nanoelectronic, NEMS, optical and bio-nanotechnology-based devices. Especially, a successful 'beyond CMOS' information-processing paradigm most likely will require novel lithographic technologies. Systems with such low dimensions exhibit peculiar characteristics: quantized excitations, single-atom electron spin qubit in silicon, and Coulomb blockade and single-electron tunneling [1, 2]. However, the lack of adequate manufacturing technologies, especially lithographic methods, inhibits the practical application of quantum effect devices such as room temperature single-electron and quantum-dot devices [2].

Based on the thermally actuated, piezoresistive cantilever technology we have developed a scanning probe lithography (SPL) platform (Fig. 1 & Fig. 2) able to image, inspect, align and pattern features down to single digit nano regime. [1-7] Herein, we have already demonstrated the application of electric field, current controlled SPL for fabrication of sub-5 nm features [2, 6], their combination with electron / EUV lithography [6] as well as their practical usage in pattern transfer by plasma etching [5].

In this paper we show the advancement of the electric field, current controlled SPL (EF-CC-SPL) towards the dynamic mode mask-less writing of positive as well as negative tone features, the optimization of exposure parameters for both modes, as well as the improvement of the set-up itself for ease of use lithographic application. For example, in Fig. 2 an array of 4 meander line features are written by direct, positive-tone mode SPL. AFM imaging for subsequent feature inspection was carried out directly after SPL processing (no step in between) using the same cantilever (5 nm tip radius of curvature). In positive tone SPL mode, the applied electric field triggers a local field emission of low energy electrons penetrating the resist, which leads in turn to a direct removal process below the nanoprobe. Within one meander line feature the pitch was modulated from (1) 75 nm hp; (2) 50 nm hp; (3) 25 nm hp, and backward, whereby each meander was patterned at different exposure dose. One can obtain that meander line (b) was under-exposed, line (d) is over-exposed, and features (a) and (c) are exposed with optimum dose.

In summary, a big process window, high reproducibility as well as versatility of the EF-CC-SPL process for patterning of diverse molecular resist materials can be obtained, offering promising novel routes towards patterning of single digit nano-features. Owing to highly promising merits of the SPL, like: (1) Capability of closed-loop lithography, including pre-imaging for overlay alignment and stitching, and post-imaging for feature inspection; (2) Capability of sub-5-nm lithographic resolution with sub-nm line edge roughness (LER); (3) High overlay alignment accuracy close to atomic level; (4) Ease-of-use and relatively low costs of ownership, SPL is a promising allround-tool for rapid nanoscale prototyping and high resolution nanoimprint lithography (NIL) template fabrication.

9423-14, Session 4

Optimization of near-field scanning optical lithography

Ben S. Routley, John L. Holdsworth, Andrew J. Fleming, The Univ. of Newcastle (Australia)

Near-field scanning optical lithography (NSOL) offers a pathway to integrated circuit (IC) prototyping with 30nm feature sizes. Although current optical techniques offer this resolution with much higher throughput they require a unique mask for each IC design. This mask is typically costly and many are required, ultimately making this approach less suitable for prototyping. As NSOL is a direct write technique no mask is required. Other direct write techniques include electron-beam lithography, x-ray lithography and ion-beam lithography. These techniques require a vacuum which increases the high capital cost. NSOL also has the advantage that it can be applied to already well established optical based manufacturing techniques that have been honed by vast amounts of research and development. Traditionally NSOL is considered a serial process and thus has a relatively low throughput. However NSOL can be performed in parallel with the use of an array of near-field probes.

In order to obtain optimal performance from NSOL multiple parameters need to be optimized. This optimization would be a heavy undertaking if done solely experimentally and thus a two dimensional computational model based on the finite-difference frequency-domain (FDFD) method was developed. FDFD solves Maxwell's equations for a grid of specified material constants producing a map of the electric field. By multiplying the modulus of this map squared with the corresponding imagery dielectric constant, a map that is proportional to the absorption at each grid point is produced. This map can then be sliced up to produce absorption profiles. These profiles can then be used to calculate the full width half maximum (FWHM). Although the FWHM is not equal to feature size produced, it is related, making it a useful metric for comparing arrangements. Typically the FWHM was calculated at the photoresist/anti-reflective coating interface as this will be the maximum. The parameters that were explored included the probe aperture size, photoresist thickness, the wavelength of the incident light and the anti-reflective coating thickness. These optimized parameters were then tested experimentally.

9423-15, Session 4

Progress on thermal scanning probe lithography

Felix Holzner, Philip Paul, Simon Bonanni, Stefan Weber, Martin Spieser, SwissLitho AG (Switzerland); Colin Rawlings, Heiko Wolf, Ute Drechsler, Urs Duerig, Armin W. Knoll, IBM Research – Zürich (Switzerland)

Thermal scanning probe lithography (tSPL) has recently entered the lithography market as the first true alternative to electron beam lithography (EBL). In 2014, the first dedicated lithography systems based on this technology have been installed at universities in Europe and America.

The tSPL technology is attractive due to the fact that no development and additional inspection steps are necessary to write nanostructures at 10nm and even below. Furthermore, the unique capabilities that go beyond the capabilities of EBL enable researchers to try out new designs for devices. The direct 3D writing capability using a closed-loop lithography scheme has enabled a vertical resolution below 2nm and hence allows the fabrication of accurate 3D shapes, e.g. for nanophotonic and nanooptical applications.

Since the proof-of-principle of tSPL in 2010 [1,2] the technology has undergone tremendous progress. In 2011, the patterning speed using a single heated tip could be strongly increased to outperform any other tip based lithography technique and match the speed of high resolution Gaussian-beam EBL [3]. In 2012, the in-situ high speed imaging capability in combination with the natural surface roughness as the perfect marker structure was used to demonstrate position determination for stitching with 1nm accuracy [4]. Pattern transfer with low line edge roughness and 27.5nm half-pitch was shown in 2013 [5] and recently pushed below 20nm half-pitch. In 2014, a novel scheme employing the in-situ imaging and the detection of buried structures under the resist was shown to be suitable for overlay with 3nm accuracy without using dedicated markers [6].

Today, tSPL is mainly suitable for rapid prototyping applications in basic research. Current development efforts are going also towards industrial applications. Accurate and stable full wafer scale mechanics and multi cantilever patterning are the main requirements and challenges for this transition towards the industrial usage of the technology. A prototype of a 12-inch tSPL system has been constructed and tested, demonstrating high resolution tSPL processing on large scale samples. Also a novel kind of thermal cantilevers with an integrated electrostatical actuation mechanism has been fabricated. These cantilevers can be operated independently of the substrate and further enable the usage of multiple independent cantilevers at high speed. First patterning results using this kind of cantilevers for tSPL will be presented and upcoming challenges will be discussed.

Acknowledgment: This work is supported by the "Seventh Framework Programme (FP7)" in the project "SNM: Single Nanometer Manufacturing for beyond CMOS devices".

[1] D. Pires, J. L. Hedrick, A. De Silva, J. Frommer, B. Gotsmann, H. Wolf, M. Despont, U. Duerig and A. W. Knoll, Science 328 (2010), 732.

[2] A. W. Knoll, D. Pires, O. Coulembier, P. Dubois, J. L. Hedrick, J. Frommer

and U. Duerig, Adv. Mater. 22 (2010), 3361-3365.

[3] P. Paul, A. Knoll, F. Holzner, M. Despont and U. Duerig, Nanotechnology 22 (2011), 275306.

[4] P. Paul, A. Knoll, F. Holzner and U. Duerig, Nanotechnology 23 (2012), 385307.

[5] L.L. Cheong, P. Paul, F. Holzner, M. Despont, D. J. Coady, J. L. Hedrick and U. Duerig (2013) Nano Letters, 13(9), 4485-4491.

[6] C. Rawlings, U. Duerig, J. Hedrick, D. Coady & A. Knoll, Advanced Intelligent Mechatronics (AIM), 2014 IEEE/ASME International Conference on (pp. 1670-1675). IEEE

9423-16, Session 4

Challenges and opportunities of scanning probe lithography for creation of guiding patterns used in directed self-assembly of block co-polymers

Francesc Perez-Murano, Laura Evangelio, Matteo Lorenzoni, Marta Fernandez-Regulez, Ctr. Nacional de Microelectrónica (Spain); Marcus Kaestner, Yana Krivoshapkina, Ivo W. Rangelow, Technische Univ. Ilmenau (Germany)

Directed self-assembly (DSA) of block co-polymers (BCPs) allows the creation of large area patterns at high resolution. Owing to the high-throughput capability and its simplicity in comparison to pure top-down techniques, DSA offers high potentials for industrial impact. Orientation and perfect periodicity of the DSA patterns are achieved by conveniently created guiding patterns, which direct the assembly of the BCPs. Deep UV lithography (DUVL) is usually the method of choice for defining the guiding patterns. However, due to the limited availability of DUVL in research environment, electron beam lithography is applied therefor. In both cases it is challenging to obtain guiding patterns with sufficient resolution, required for the future evolution of semiconductor manufacturing.

Instead, scanning probe based lithography (SPL) enables unique capabilities in terms of resolution and pattern placement. Recent advances include the achievement of patterning resolution below 5 nm by local anodic oxidation, three dimensional patterning by thermomechanical writing and the localized removal of calixarene-based molecular resist for high resolution patterning. All of them offers advantages compared to EBL or DUVL, not only in terms of resolution, but also in other aspects like the possibility for in-line inspection and the lack of proximity effects.

The application of SPL for creation of guiding patterns has been previously presented by Checco and coworkers . Here the terminal methyl groups of an OTS self-assembled monolayer are converted into carboxylic groups, which show a higher affinity to the PMMA block in cylindrical formed BCP. We have shown previously that guiding patterns can be created on PS-OH brush layers to align lamella forming PS/PMMA block co-polymers.

Herein, we present our advances in SPL applied to create chemical guiding patterns for DSA of BCPs. We demonstrate the creation of sub-10 nm patterns as well as the application of novel SPL methods based on current-controlled exposure of calixarene-based molecular resist. Interestingly, the chemical/physical nature of the guiding patterns created by SPL shows distinct features like unexpected affinity to the co-polymers blocks and the fact that they can consist of a combination of chemical and topographical change. In consequence, they reveal novel alignment approaches for BCPs enabling a smaller pitch and larger multiplication factors. The challenges for future applications of SPL in terms of throughput and reproducibility will be discussed, and examples of pattern formation by parallelization of the SPL process in order to increase the throughput and pattern extension will be shown

9423-17, Session 5

Pattern transfer into silicon using sub-10 nm masks made by Electron Beam Induced Deposition

Marijke Scotuzzi, Technische Univ. Delft (Netherlands); Martin Kamerbeek, Technische Univ. Delft (Netherlands) and MAPPER Lithography (Netherlands); Andy Goodyear, Oxford Instruments (United Kingdom); Mike Cooke, Oxford Instruments Plasma Technology (United Kingdom); Cornelis W. Hagen, Technische Univ. Delft (Netherlands)

To fabricate single-digit nanometer patterns is not trivial. Resist-based lithography is not ca-pable of routinely providing sub-10 nm structures. Two lithography techniques that do have the required spatial resolution are Scanning Probe Microscopy (SPM) and Electron Beam Induced Deposition (EBID). Both are serial writing techniques and therefore inherently slow. This problem can be alleviated by parallelization. The European project Single Nanometer Manufacturing for beyond CMOS devices (SNM) [1] aims at using these techniques to fabri-cate stamps for Nano-imprint Lithography (NIL), to develop NIL processes for the fabrica-tion of single-digit nanometer devices.

In Delft we focus on parallel EBID [2] for which we are developing a Multi-Beam Scanning Electron Microscope (MBSEM) with 196 beams [3,4], each of which has the same probe size and probe current as a single-beam SEM. NIL stamps, that have to be UV transparent, can be made either by direct deposition of transparent patterns on a conducting transparent substrate, or by deposition of masks (not necessarily transparent) for a subsequent pattern transfer into a transparent stamp material. To gain some insight in transferring nano-patterns into an under-lying substrate, we use EBID to fabricate patterns that serve as etch masks in a subsequent plasma etching process. A first test was aimed at selecting the best process out of three plasma etching processes, using HBr, Cl2 and Cl2+BCl3, respectively. They are a combination of Inductively Coupled Plasma and Reactive Ion Etching, providing separately control over the energy and the density of the ions. The EBID etch-masks consist of four arrays of dots, pat-terned on top of a Si wafer, using the MeCpPtMe3 precursor, at 30 kV. The dots have sizes varying from 19 nm to 42 nm at a pitch of 100 nm. The best result is achieved with the Cl2 based etch, as it preserves the width of the patterns, and the height of the patterns increased by a factor of 4 after etching. Figure 1 shows SEM images and AFM profiles of the mask and the transferred pattern as a result of the Cl2 etch. Figure 2 shows the AFM line profiles of the central line of the top left array of dots before (blue) and after (red) etching. The next step is to fabricate sub-10 nm patterns and transfer them into Si. Figure 3 shows a SEM image of the dot- and line-shaped EBID masks. The lateral size of the features was determined from the SEM images, and the height from AFM measurements. We will report the results of the dif-ferent etching processes performed on these EBID masks.

References

[1] We acknowledge support from the European Union under Grant Agreement No. 318804 (SNM).

[2] P.C. Post, A. Mohammadi-Gheidari, C.W. Hagen and P. Kruit, J. Vac. Sci. Technol. B29 (2011) 06F310.

[3] A. Mohammadi-Gheidari, C.W. Hagen and P. Kruit, J. Vac. Sci. Technol. B28 (2010) C6G5.

[4] A. Mohammadi-Gheidari and P. Kruit, Nuclear Instruments and Methods in Physics Re-search A 645 (2011) 60.

9423-18, Session 5

Sub-5nm patterning using helium ion-beam lithography and nanoimprint lithography

Yuhan Yao, He Liu, Yifei Wang, The Univ. of Southern

California (United States); Wen-Di Li, The Univ. of Hong Kong (Hong Kong, China); Ahmad N. Abbas, Gang Liu, The Univ. of Southern California (United States); R. Stanley Williams, Hewlett-Packard Labs. (United States); Chongwu Zhou, Wei Wu, The Univ. of Southern California (United States)

Helium ion beam lithography (HIBL) is a recently developed nanolithography technology. It uses a He ion beam to direct write patterns in the same fashion as electron beam lithography (EBL). Due to its advantages, such as smaller focusing spot and less proximity effects than electron beam, it can go beyond the resolution of EBL. We have demonstrated patterning of various nano-patterns using HIBL. For example, we achieved dense lines with half-pitch down to 4 nm. Moreover, we also achieved sub-5 nm patterning using nanoimprint lithography (NIL) with molds fabricated by HIBL. The combination of NIL and HIBL mitigates the two major drawbacks of HIBL: low throughput and the tendency to damage substrates. We also used HIBL as a direct milling tool to pattern metal and Graphene with dense lines down to 4 nm half-pitch. Our Raman spectra show that the HIBL patterned Graphene nanoribbons (GNRs) have lower line-edge roughness than reported GNRs patterned by EBL. At 5 nm half-pitch, the GNRs had a band gap of 88 meV. A gas sensor was also built using these GNRs.

9423-19, Session 5

Fabrication of functional electromechanical nanowire resonators by focused ion-beam (FIB) implantation

Jordi Llobet, Marc Sansa, Ctr. Nacional de Microelectrónica (Spain); Xavier Borrisé, Institut Català de Nanociència i Nanotecnologia (ICN2) (Spain); Francesc Pérez-Murano, Ctr. Nacional de Microelectrónica (Spain)

We present the fabrication of silicon nanowire (SiNW) mechanical resonators by a resistless process based on focused ion beam local gallium implantation, selective silicon etching and diffusive boron doping. The resulting suspended SiNWs present a good electrical conductivity which is employed to characterize their high frequency mechanical response by electrical methods.

The fabrication of suspended silicon nanowires by this method is simple, fast and reliable, and it does not require a critical surface preparation, since it proceeds correctly even in the presence of silicon native oxide [1]. The etching of the underlying Si is performed by wet silicon etching using TMAH (tetramethilammonium hydroxide) at 25% of concentration. We take advantage of the anisotropic etching rate of TMAH to obtain released or non-released nanowires according to their specific orientation. The last step consists on a post-annealing at high temperature in a boron environment, allowing the recovering of the crystalline structure and the improvement of the electrical conductivity of the silicon nanowire [2]. The final resistivity of the SiNWs is on the order of 10-4 Ω•m and 10nm diameter free suspended structures of more than 4μm length are achievable.

The devices consist on double clamped SiNWs with a side-gate nearby for electrostatic actuation. The length of the nanowire is 4.14 μm and the dimensions of the cross-sectional area are 40 nm (thickness) x 540 nm (width). The thickness of the SiNW is 40 nm that corresponds to the range of implanted gallium.

As the suspended SiNWs are conductive at the end of the fabrication process, the electrical read-out of their mechanical oscillation is enabled. We measure their frequency response by using a frequency modulation (FM) electrical down-mixing method [3,4]. The measurements are performed inside the vacuum chamber of the SEM/FIB system using three micromanipulators with electrical connection for low-resistance and low-noise electrical measurements. We have been able to identify the different resonant modes of the devices. The flexibility of the technique allows to experiment in different designs like coupled devices or asymmetric structures.

[1] J. Brugger, G. Beljakovic, M. Despont, N. F. De Rooij, P. Vettiger “Silicon micro /nanomechanical device fabrication based on focused ion beam surface modification and KOH etching” Microelectronic Engineering 35(1):401-4 (1997)

[2] J. Llobet, M. Sansa, M. Gerbolés, J. Arbiol, N. Mestres, X. Borrisé, F. Pérez-Murano. “Enabling electromechanical transduction in silicon nanowire mechanical resonators fabricated by focused ion beam implantation” Nanotechnology 25 135302 (2014)

[3] M. Sansa, M. Ferna?ndez-Regu?lez, A. San Paulo, and F. Pe?rez-Murano “Electrical transduction in nanomechanical resonators based on doubly clamped bottom-up silicon nanowires” Applied Physics Letters 101(24):243115 38 (2012)

[4] M. Sansa, M. Fernandez-Regulez, J. Llobet, A. San Paulo, F. Perez-Murano “High sensitivity linear piezoresistive transduction for nanomechanical beam resonators” Nature Communications 5:4313 (2014)

9423-20, Session 5

Towards nanostars patterning by three coplanar beam interferential lithography

Joyce Ibrahim, Anna Rumyantseva, Gilles Lerondel, Timothée Toury, Univ. de Technologie Troyes (France)

In the last 20 years, periodic nanostructures made of metals have attracted a lot of interest due to their optical properties. Metallic nanoparticles display a collective resonance of free confined electrons. They can be used to enhance the IR vibrational signal of absorbed molecules on the sample surface [1]. Nanostars had already shown an increase in the enhancement in extinction measurement in the visible [2]. Different approaches used for fabrication of patterned structures however we are limited by the size of the nanostructured area and the cost which prohibits patterning for large scale applications [3]. Interference lithography holds the promise for fabricating large-area, nanometer-scale, periodically patterned structures having different forms. Multiple beam interference lithography has been used to create different forms of photonic structures [4] and recently for fabricating plasmonic nanostructures [5].

In this work we demonstrate the fabrication of nanostars by a new top-down approach namely, three coplanar beam interferential lithography. In this technique the beam is split to three coherent beams thanks to a phase mask. The intensity of the beam at the center is half as compared to the intensity of the other two beams. In this manner, we can generate structures directly in the photoresist or we can transfer it to another type of material by lift off or by etching process. Various parameters such as time, angle and phases have been optimized in order to obtain nano-stars.

Figure 1 shows a scanning electron microscope (SEM) image of the gold nanostructures obtained by using interferential lithography technique in combination with lift-off process. Due to the lack of full phase control we obtain stars on a limited surface of about 50μm x 50μm. The distance between two adjacent arms of the same star is 2μm. For the same reason on the same substrate we have different shapes of structure and this effect more precisely is due to the change in phase or misalignment of one of the three beams. This phenomenon is called “moiré patterns”.

We conducted a parametric simulation study to obtain stars using this technique. We use a photoresist (S1813) with dose threshold; above certain energy the photoresist will be exposed. We obtain a map for exposed and unexposed area (fig.2). A comparison between final structures fig.2 a) and simulated once is shown in fig. 2 b) and c). For different phases we obtain different forms of structures as already demonstrated from non-planar three beams IL [6].

Multiple-exposure interferometric lithography using three coplanar beams is a technique for the production of complex structure such as three armed stars. The phase of the beam can be controlled to change the form of the structures. Those nanoparticles can be used in the field of detection SERS and SEIRA with final applications in chemo or biosensing.

References:

[1] J.Grand, P.M. Adam, A.S. Grimault, A. Vial, M de La Chapelle, J.L. Bijeon, S. Kostcheev, and P. Royer. Plasmonics, page 135, September 2006.

[2] M. de la Chapelle, N. Guillot, B. Fremaux, H. Shen, and T. Toury. Plasmonics, july 2012.

[3] G. Lerondel, S. Kostcheev, and J. Plain. Nanofabrication for plasmonics. Springer Series in optical Sciences, 2012.

[4] V.Berger, O. Gauthier-Lafaye, and E. Costard. J. Appl. Phys, April 1997.

[5] C. H. Liu, M. H. Hong, H. W. Cheung, F. Zhang, Z. Q. Huang, L. S. Tan, and T. S. A. Hor. OSA, July 2008.

[6] Cheng Lu, X. K. Hu, S. S. Dimov, and R. H. Lipson. OSA. page 7202, October 2007.

9423-21, Session 6

Defect mitigation and root cause studies in IMEC's 14nm half-pitch chemo-epitaxy DSA flow

Hari Pathangi, Boon Teik Chan, Hareen Bayana, Dieter Van Den Heuvel, Lieve Van Look, Paulina A. Rincon-Delgadillo, IMEC (Belgium); Guanyang Lin, Yi Cao, JiHoon Kim, AZ Electronic Materials USA Corp. (United States); Doni Parnell, Tokyo Electron Europe Ltd. (Netherlands); Kathleen Nafus, Tokyo Electron America, Inc. (United States); Ito Chikashi, Venkat R. Nagaswami, KLA-Tencor Corp. (United States); Lucia D'Urzo, Entegris GmbH (Germany); Roel Gronheid, IMEC (Belgium); Paul F. Nealey, The Univ. of Chicago (United States)

Directed self-assembly (DSA) of block co-polymers (BCPs) is a very simple and elegant pattern generation technique that has been studied both by industry and academia from a variety of perspectives during the last decade [1,2]. DSA has been up-held as a promising candidate for patterning in future device fabrication schemes, where conventional lithography seems to be pushed towards it's physical limitations. Achieving production-friendly defect densities in DSA flows has been identified as one of the major milestones for demonstrating the maturity of DSA [3,4].

In our previous work [4], we demonstrated defectivity levels after transferring 14 nm half-pitch DSA line/space patterns into the Si substrate in a fully integrated 300 mm wafer production environment. We reported a total defect density of 200 cm-2, which was mainly a result of an extended BCP anneal duration. In this manuscript, we report our recent optimization efforts in monitoring and reducing the total defect density of our chemo-epitaxy flow. Our current process, upon optimization, results in a final defect density of around 48 cm-2 after pattern transfer.

In addition to presenting a sheer reduction in our defect numbers, this manuscript will describe our efforts in understanding the possible root cause(s) of the most prevalent defect modes observed after pattern transfer. This is enabled by our cohesive efforts from different fronts including, understanding (i) the influence of chemical compositions of the DSA materials involved in the flow towards assembly defects, (ii) the influence of the various process parameters and their interactions on specific defect modes and the total defect density, at large and (iii) the limits and sensitivity of the defect inspection/review tools in identifying the rather non-conventional DSA defect modes [5].

References

[1] S.O. Kim et al., Nature (2003), Vol. 424, 411-414.

[2] C. Bencher et al., Proc. SPIE 7970 (2011), 79700F.

[3] P.A.R. Delgadillo et al., Proc. SPIE Vol. 8323 (2012), 83230D-1

[4] R. Gronheid et al., Proc. SPIE (2014), Vol. 9049, 904905-1.

[5] C. Ito et al., Proc. SPIE (2014), Vol. 9049, 90492D-1.

9423-57, Session PS1

Negative e-beam resists using for nano-imprint lithography and silicone mold fabrication

Shyi-Long Shy, National Nano Device Labs. (Taiwan); Anil Kumar T.V., Gene Sheu, Shao-Ming Yang, Asia Univ. (Taiwan); M. C. Chen, C. S. Hong, National Nano Device Labs. (Taiwan)

Nano-imprinting technology, as one of the most promising fabrication technologies, has been demonstrated to be a powerful tool for large-area replication up to wafer-level, with features down to nanometer scale. This study aims to develop capabilities in patterning nano structure using thermal nano-imprint lithography (NIL). 30nm Si molds are patterned by electron-beam lithography (EBL) using NEB22 A2 negative e-beam resist. The NEB22 A2 negative e-beam resist possess a variety of characteristics desirable for NIL, such as low viscosity, low bulk-volumetric shrinkage, high Young's modulus, high thermal stability, and excellent dry-etch resistance. The excellent oxygen-etch resistance of the barrier material enables a final transfer pattern that is about three times higher than that of the original NIL mold. Based on these imprint on negative photo resist approach is used for pattern transfer into silicon substrates. The result is a high-resolution pattern with feature sizes in the range of nanometer to several microns. Detail process of negative e-beam resist using for nano-imprint lithography and silicone mold fabrication will be presented in SPIE Advanced Lithography 2015.

9423-58, Session PS1

Advanced nano lithography via soft materials-derived and reversible nano-patterning methodology for molding of infrared nano lenses

Jae Hong Park, National Nanofab Ctr. (Korea, Republic of); Hyun Ik Jang, National Nanofab. Ctr. (Korea, Republic of); Jun Yong Park, Seok Woo Jeon, KAIST (Korea, Republic of); Woo Choong Kim, Hee Yeoun Kim, National Nanofab Ctr. (Korea, Republic of); Chi Won Ahn, KAIST (Korea, Republic of)

One of the two main processes of engineering nanostructures is the top down method, which is a direct engineering method for Si-type materials using photolithography or e-beam lithography. The other method is the bottom-up method, using nano-imprinting. However, these methods are very dependent on the equipment used, and have a high process cost. They are also relatively inefficient methods in terms of processing time and energy. Therefore, some researchers have studied the replication of nano-scale patterns via the soft lithographic concept, which is more efficient and requires a lower processing cost. In this study, accurate nanostructures with various aspect ratios are created on several types of materials. A silicon (Si) nanomold is preserved using the method described, and target nanostructures are replicated reversibly and unlimitedly to or from various hard and soft materials. The optimum method of transferring nanostructures on polymeric materials to metallic materials using electroplating technology was also described. Optimal replication and demolding processes for nanostructures with high aspect ratios, which proved the most difficult, were suggested by controlling the surface energy between the functional materials. Relevant numerical studies and analysis were also performed. Our results showed that it was possible to realize accurate nanostructures with high depth aspect ratios of up to 1:18 on lines with widths from 300–400 nm.

In addition, we were able to expand the applicability of the nano structured mold by adopting various backing materials, including a rounded substrate. The application scope was extended further by transferring the

nanostructures between different species of materials, including metallic materials as well as an identical species of material. In particular, the methodology suggested in this research provides the great possibility of creating nanostructures composed of various materials, such as soft polymer, hard polymer, and metal, as well as Si. Such nanostructures are required for a vast range of optical and display devices, photonic components, physical devices, energy devices including electrodes of secondary batteries, fuel cells, solar cells, and energy harvesters, biological devices including biochips, biomimetic or biosimilar structured devices, and mechanical devices including micro- or nano-scale sensors and actuators.

9423-59, Session PS2

Fabrication of silicon nanowire devices by oxidation scanning probe lithography

Yu Kyoung Ryu, Ricardo Garcia, Instituto de Ciencia de Materiales de Madrid (Spain) and Spanish National Research Council (Spain)

Silicon nanowires (SiNWs) are one of the key nanostructure systems to fabricate functional and sensitive devices such as label-free biosensors, suspended nanoelectromechanical resonators (NEMS), photovoltaic devices or lithium batteries. Currently, there are many methods available to synthesize (Bottom-up) or to produce (top-down) silicon nanowires with high surface-to-volume ratio and large integration. Scanning probe lithography (SPL) is one of the most promising alternative lithographic technologies that is being developed nowadays to pattern and fabricate nano devices due to its relatively low-cost and simple experimental set-up requirements, its positioning and shaping capabilities and its applicability to a wide range of materials (polymers, metallic or semiconducting surfaces, self-assembled monolayers or biological samples).

Specifically, oxidation scanning probe lithography (o-SPL) can be employed to obtain straight and curve silicon nanowire field effect transistors (SiNW FETs) starting from a silicon on insulator (SOI) substrate. O-SPL technique consists basically in the oxidation of a silicon surface when an atomic force microscope (AFM) tip is placed to it a few nanometers of distance and a pulse is applied between them. A water meniscus and the dissociation of the water molecules are produced by means of the strong electric field which is formed between the tip and the sample (1-30 V/nm). The water meniscus confines the reaction locally and acts as an electrochemical cell at the nanoscale. The fabrication steps include a photolithography one to define metallic location markers, o-SPL to fabricate the silicon oxide etch masks, another photolithography step to contact the oxide masks with the electrode contacts and finally, reactive ion etching to transfer the pattern of the silicon oxide mask to the top silicon layer of the SOI. After the etching step, a back-gated Schottky barrier SiNW FET is obtained, where the metal electrodes act as the source and drain, the silicon nanowire is the channel of the transistor, the buried oxide layer (BOX) is the dielectric layer and the bottom silicon layer acts as the back gate. These silicon nanowires have a trapezoidal shape inherited from the shape of the oxide mask produced by the o-SPL step and average electron mobility and subthreshold swing of, respectively, 200 cm2 V-1 s-1 and 500 mV/dec, values that are comparable with those from similar silicon nanowire transistors fabricated by other top-down and bottom-up methods found in the recent literature.

The combination of o-SPL with RIE using an ultra thin SOI is able to produce sub-12 nm thick silicon nanowires by using sub-1.1 nm thick silicon oxide masks. This resistless etching process yields silicon nanowires with very small cross sections (< 100 nm2) and with a silicon oxide mask: silicon nanowire widths ratio close to one. This last point means that in this process, the lateral resolution of the silicon nanowire is given by the lateral resolution achievable with the scanning probe lithography, since the anisotropic dry etching is able to replicate the width of the mask onto the silicon substrate. The o-SPL fabricated Schottky barrier SiNW FETs have been employed as free-label biosensors to detect molecular recognition processes.

9423-60, Session PS3

An instruction-based high-throughput lossless decompression algorithm for e-beam direct write system

Cheng-Chi Wu, Jensen Yang, Wen-Chuan Wang, Shy-Jay Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

About 13-Terabyte data for Massive e-beam direct write lithography (MEBDW) system, a potential solution for high-volume manufacturing (HVM) of 10-nm and beyond technology nodes in a 26 mm x 33 mm field of layout, is required. Therefore cost reduction on data storage and transmission through development of high compression rate of lossless data and high throughput real time decompression algorithms is necessary.

In this paper, an instruction-based hybrid decompression (IBHD) is proposed. It is an asymmetric scheme to hybrid simple compression methods. The decompression is achieved by instruction-based decoding. The input layout image is partitioned into different fragments, compressed and encoded into instructions. On the MEBDW system side, the encoded bit-stream is decoded by the IBHD decoder. The function of this decoder is to execute only a minimal number of simple instructions, thus the decoder can be implemented with low gate-count on ASIC. Simulation results show that a single IBHD decoder is capable of providing an output data rate as high as ~50Gbps in various masking layers.

9423-61, Session PS3

Fast and thick e-beam resists exposed with multi-beam tool at 5 keV for implants and mature nodes: experimental and simulated model study

Aurélien Fay, Nideye A. Thiam, CEA-LETI (France); Marie-Laure Cordini, STMicroelectronics (France); Isabelle Servin, Christophe Constancias, Ludovic Lattard, Laurent Pain, CEA-LETI (France)

Maskless lithography represents today an attractive solution to address sub-20 nm technology nodes to extend Moore's law. However, multi-beam lithography at low energy has also the capability to extend to mature CMOS technologies [130-45nm nodes] with high throughput and significant manufacturing costs reduction . To address this market needs, new e-beam resists must be compatible with standard CMOS process flow. It requires both "fast" resists for throughput gain and cost of ownership and "thick" resists matched with the current post-lithography processes such as etching and implant steps. The lithographic ability for multi-beam technology is not limited by critical dimensions (CD) targets because the layout designs are relaxed (140 nm minimum pitch for Gate for 45 nm node). The main challenge to overcome is to maintain correct resist profiles using thick resist films with high aspect ratio up to 3. For implants, resist thickness has to be sufficiently large to stop ion penetration, reaching for instance 400 nm for DUV resists in conventional optical lithography. Nevertheless, ion implementation simulations performed with the SRIM software show that the stopping power of 150 nm thick resist is widely sufficient to mask some layers such as Lightly Doped Drain (LDD) and Source/Drain (S/D).

In this paper, we will focus on the lithographic performances of "fast" & "thick" E-beam resists for multi-beam exposure at 5 keV. Images of lines and spaces (L/S), contact holes (CH) patterns and cut SRAM 65 nm show well resolved patterning with high sensitive positive CAR resist (dose ~15-20 μC/cm2) at film thickness of 130 nm exposed with a 5 keV MAPPER pre-alpha tool [Fig. 1]. The resist profile resulting from SEM cross-section shows an undercut profile for positive resist due to forward scattering and proximity effect [Fig. 2b] (resist footings for negative tone). From these assessments, we investigated post-lithography treatments to minimize this undercut. In addition, two different CAR resist platforms have been tested with different resist thicknesses and different CD pitch of 110, 140 and 180 nm. No issue

of pattern collapse has been observed for the CMOS design rules, 130-45 nm nodes. In parallel to this experimental work, we developed a theoretical model to simulate 3D patterning at 5 keV. We firstly performed Monte Carlo simulations with Casino to extract the electron beam Point Spread Function (PSF) as a function of the depth into the wafer stack [Fig. 2a]. The theoretical 3D developed patterns were calculated by using the INSCALE software. We find that the simulations are in good agreement with the SEM cross-section images [Fig. 2b], as well as with the experimental top view SEM images and confirm the absence of fully suspended resist regions. Thus we demonstrate the capability of the 5keV E-beam lithography on thick resist for implants and 130-45 nodes.

[1] G. de Boer, EIPBN conference (2013)

[2] J. F. Ziegler and J. P. Biersack and M. D. Ziegler (2008). SRIM - The Stopping and Range of Ions in Matter. SRIM Co. ISBN 0-9654207-1-X

[3] CASINO V2.42—A Fast and Easy-to-use Modeling Tool for Scanning Electron Microscopy and Microanalysis Users, SCANNING VOL. 29, 92–101 (2007)

9423-63, Session PS3

Nanoscale intracavity defects in photonic crystal microcavity filter for enhancing transmission

Aju S. Jugessur, The Univ. of Iowa (United States)

There have been numerous reports1-3 on one- (1-D) or two-dimensional (2-D) photonic crystal (PhC) microcavity filters over the last several years. The functionality of these devices can be tailored to suit any specific application such as optical filters2,4, sensors5,6 and optical memory7. In particular, 1-D PhC microcavity filters are promising candidates for a wide range of applications. Nevertheless, the coupling of light into these miniature devices still poses a technical challenge, especially, when light transits the waveguide region to the photonic crystal structures and vice versa. Large reflection, coupling and scattering losses are common at these transition zones. Appropriate features need to be added in those regions in order to provide a gradual modal conversion. In previous reports, by the same author, a mode-matching technique has been demonstrated in 1-D PhC microcavity filters4 outside the cavity region. In this work, nano-scale defects are designed and added within the cavity that demonstrates an enhancement in optical transmission. Unlike previous reports4, the added features do not have the same periodicity as the PhC holes in the mirror section. The size and period of the mode-matching holes have been designed and optimized to obtain a higher transmission at the selected second resonance peak. The computation spectrum of the 1D PhC filter without intra-cavity defects is shown in Figure 1. Figure 2 shows a schematic of the device design with the intra-cavity holes. Figure 3 shows the fabricated device using Electron Beam Lithography and Reactive ion etching, where a proximity correction tool has been used for the exposure of the structure. The addition of nano-scale defects such as holes within the cavity region results in an optical transmission enhancement by a factor of 2.5, as demonstrated in the experimental spectrum in Figure 4. The wavelength spectrum also shows various spurious transmission features that are believed to originate from other microcavities within the device structure. Cavities could be formed due to fabrication errors such as overlays at the taper sections or simply fabrication defects within the structure. The peak resonance linewidth is also broad, with a low Q-factor and the addition of the nano-scale defects within the cavity decreases the Q-factor further. This is believed to be due to a decrease in photon-lifetime within the cavity as the defects help with the transition of the scattering losses within the cavity to the periodic and waveguide regions at a much faster rate.

9423-65, Session PS4

Periodic structures with 50nm feature size using Talbot lithography and a table top EUV laser

Wei Li, Colorado State Univ. (United States); Hyun-su Kim, RWTH Aachen (Germany); Carmen S. Menoni, Colorado State Univ. (United States); Larissa Juschkin, RWTH Aachen (Germany); Theodore B. Norris, Univ. of Michigan (United States); Mario C. Marconi, Colorado State Univ. (United States)

We describe an extreme ultraviolet (EUV) lithography method utilizing a compact EUV laser and the Talbot effect. With an illumination wavelength of 46.9 nm we demonstrated 50nm dense lines using displacement Talbot lithography (DTL). This particular method allows for doubling the spacial frequency of the mask and simultaneously provides an effectively infinite depth of focus.

Fractional Talbot lithography with up to 5X spacial frequency multiplication was also demonstrated. Lines with a periodicity of 600 nm were obtained starting from a master with a period of 3μm.

Using the traditional Talbot lithography we also fabricated meta-surfaces with sub-50 nm patterns in Au, transferring the Talbot lithography print onto an Au-coated substrate using anisotropic ion etching.

All the experiments described herein have been performed in a table top system which is cost effective, capable of patterning large area in short exposures and very repetitive. The technique described in this work is well suited for a small scale, table-top lithography tool compatible with prototyping and small volume production of periodic nanostructures.

9423-66, Session PS4

High-resolution plasmonic lithography for practical application and fabrication of high-aspect-ratio nanoimprint masters

Jae W. Hahn, Howon Jung, Seok Kim, Jinhee Jang, Seonghyeon Oh, Dandan Han, Yonsei Univ. (Korea, Republic of)

We evaluate the ultimate resolution of plasmonic lithography using the ridge aperture. We introduce a theoretical model to analyzes this resolution predicts that the resolution of plasmonic lithography strongly depends on the ridge gap, achieving values under 1x nm with a ridge gap smaller than 10 nm. Using the circular contact probe, we record high-density line array patterns with a half pitch up to 22 nm, and obtain good agreement between the theoretical model and experiment. We propose a new scheme of overlay alignment for plasmonic lithography using a scanning contact probe. Using two resonances of a ridge aperture in a metal film, we introduce the aperture's multifunctional characteristics for patterning and alignment at different wavelengths. The uncertainty of the overlay alignment method is shown to be less than approximately 2 nm. We successfully demonstrate practical application of plasmonic lithography to fabricate high-resolution and high-aspect-ratio nanoimprint masters. Using properties of a non-propagating near-field, we apply plasmonic lithography to pattern a micron-scale fluidic channel in photoresist. We apply a deep reactive ion etching (DRIE) process to transfer an arbitrary fluidic channel into a silicon substrate and fabricate a high-aspect-ratio imprint master. Subsequently, we carry out the imprint process to replicate the fluidic channel with an aspect ratio of 7.2. The solution for amplifying shallow pattern depth by using the underlying layers and reactive ion etching (RIE) processes after lithography is verified by fabricating the 70 nm resolution line array patterns on silicon substrate. Using the multilayer structure, we fabricate high-resolution nanoimprint masters in a silicon substrate with an aspect ratio greater than 1.

9423-67, Session PS4

Electric-field assisted assembly of core-shell nanoparticle arrays for contact-hole patterning

Lan Lin, Xuexue Guo, Nathan Young, Theresa S. Mayer, The Pennsylvania State Univ. (United States)

A significant challenge for traditional lithography is aggressive scaling of contact hole features without loss in critical dimension uniformity or pattern placement accuracy. Several alternative nanoscale patterning processes are being actively investigated, including nanoimprint lithography, maskless direct-write electron beam lithography, and block-copolymer directed self-assembly. While each of these techniques can deliver ultra-high-resolution features, factors such as overlay error, low throughput, defects, and/or limited pattern complexity present barriers for large-scale manufacturing. The lack of a well-defined solution drives the need to explore new strategies.

Here, we present an electric-field assisted assembly approach that is being investigated to create dense arrays of contact hole patterns with complex 1D and 2D feature geometries. This hybrid top-down/bottom-up strategy uses a spatially varying dielectrophoretic (DEP) force created by lithographically defined guiding features to assemble dense arrays of core-shell nanoparticles within the features, thereby replicating features within the starting pattern. The process exploits solution-based synthesis protocols with tight size control to produce nanoparticles from core and shell materials that have high etch selectivity. For close-packed particle arrays, the half- and full-pitch of the contact hole array should be defined by the starting nanoparticle core and shell diameter rather than by the optics of the lithography system. We will discuss the field-assisted assembly mechanism as well as the DEP force on individual particles as they populate resist patterns composed of 1x1, 1x2, 1x3, and 1x4 contact hole arrays. Initial assembly results will be presented showing site-specific placement of sub-100 nm SiO2 nanoparticles within the lithographic guiding features.

9423-68, Session PS4

Photo-induced large-scale circular surface-relief diffraction gratings on azo-glass

James Leibold, Ribal Georges Sabat, Royal Military College of Canada (Canada)

Novel metallic light-interfering fixtures, called Circular Diffraction Grating Generators (CDG), were designed and fabricated using common machine shop equipment. They consisted of annular rings with the inner diameter shaped conically. They acted as three-dimensional laser beam splitters able to achieve an interference pattern of constant-pitch, concentric and sinusoidal light variations. Solid thin-films of Disperse Red 1 azo-functionalized glass-forming compound were subsequently placed behind the fixture and circular surface-relief diffraction gratings were inscribed due to the photochemical trans-cis isomerization process of the azobenzene chromophores. This was accomplished by exposure to a collimated laser beam with a wavelength of 532 nm and an irradiance of 604 mW/cm2 for 350 seconds. The fabricated circular diffraction gratings were stable and of high quality, with pitches ranging from approximately 600 to 1400 nm and depths up to 250 nm. They could also be produced on a large scale since their diameter is only limited by the size of the collimated laser beam and the CDG fixture opening. In this experiment, the resulting gratings had a diameter of 11.4 mm. The gratings' pitch was dependent on the CDG fixture geometry, while the depth, and to a certain extent, the diffraction efficiency could be varied depending on the inscribing laser irradiance and the amount of exposure time. For a certain CDG fixture dimensions, it was also demonstrated that annular diffraction grating rings could be produced. A theoretical model was developed to correlate the CDG fixture dimensions and the inscribing laser wavelength to the gratings' pitch and diameter. The grating pitches were measured using AFM and SEM imagery, as well as first-order diffraction angle measurements, and agreed very well with the theoretical predictions. These gratings had the main advantage over other nano-fabrication techniques of being produced in a simple single-step procedure with no post-processing or specialized equipment, as well as the ability for the gratings to be thermally erased and optically re-written. Possible applications for these new gratings may include optical sensors, enhancement of LEDs, improvements in solar cell efficiency, plasmonic lenses, circular grating distributed feedback dye laser and optical measuring techniques.

9423-69, Session PS4

Solid immersion optical lithography – tuning the prism/sample interface for improved ultra high-NA, high aspect ratio resist patterns over large exposure fields

Sam D. C. Lowrey, Richard J. Blaikie, Univ. of Otago (New Zealand)

Recent work with dielectric resonant reflector underlayers has shown that high aspect ratio imaging can be achieved for solid immersion interference lithography in the ultra-high numerical aperture (UHNA) regime where evanescent fields are responsible for the resultant field intensity in the resist medium [1].

The gap that is present between the prism/sample interface during imaging has proved to be a problem for good reproducibility and quality of UHNA regime, high aspect ratio, resist structures irrespective of whether or not an index matching liquid (IML) is utilised [1], [2].

Here we present simulation and preliminary experimental results for fine tuning of the prism/sample interface. These results show the requirements that an IML must meet for producing high aspect ratio resist structures in the UHNA regime with and without good gapping control. In addition, the results show the limits of our solid immersion Lloyd's mirror interference lithography (SILMIL) system in the absence and presence of an IML when imaging over relatively large exposure fields. Figure 1 shows attenuated total reflectance (ATR) versus numerical aperture curves for increasing prism/sample interface separation (LHS) and the corresponding resultant electric field intensity in the resist layer for these interface separations (RHS). The white curves in the RHS plots correspond to the iso-intensity contour of 1/e2 of the maximum intensity and are representative of the outline of the resultant resist structure. Figures 1(a), (b) and (c) show an air gap/prism interface index mismatch of 1.84, an IML/prism refractive index mismatch of 0.07 and an IML/prism refractive index mismatch of 0.0016, respectively and the effects of an increased gap separation over the range of 0-90 nm. In each case, a dielectric resonant underlayer has been utilized consisting of HfO stacked upon SiO2 and with a silicon substrate. These results highlight the additional care that is required when selecting appropriate IMLs to achieve a desired NA and specific resist structure.

Gapping capability allows precise measurement of prism/sample separation via frustrated total internal reflection [3] and has been recently adopted for such measurements in evanescent wave lithography systems [4]. We have integrated this technique with our SILMIL system and this has allowed for greater reproducibility and reliability when performing evanescent-coupling and has allowed prism/sample interface measurements to be quantified and various index mismatched prism/IML pairs to be analysed for their effects on large area imaging for high aspect ratio resist structures using dielectric resonant underlayers in the UHNA regime. Figure 2 shows an array of ~56 nm half-pitch resolution AFM grating images produced with a prism/sample interface air gap produced with a back plate torque of 3 Nm (corresponding to an average air gap variation of ~25 nm over a 3 mm2 area), an N-SF11 glass prism acting as the solid immersion medium, a 405 nm exposure wavelength, a TE polarized light source all for an NA of 1.81. Both good quality areas (Fig. 2B and E) and poor quality areas (Fig. 2C and G) exist.

9423-71, Session PS6

Computational analysis of hole placement errors for directed self-assembly

Kosuke Yamamoto, Takeo Nakano, Tokyo Electron Ltd. (Japan); Makoto Muramatsu, Tokyo Electron Kyushu Ltd. (Japan); Tadatoshi Tomita, Tokyo Electron Europe Ltd. (Japan); Kazuyoshi Matsuzaki, Tokyo Electron Ltd. (Japan); Takahiro Kitano, Tokyo Electron Kyushu Ltd. (Japan)

Directed self-assembly (DSA) is an attractive technology to achieve sub-20nm micro patterns by self-aggregation of block co-polymers. One of the important applications is DSA holes fabrication with guide patterns, which realize hole shrink and multiplication by grapho-epitaxial restriction. In these morphologies, it is an important issue how accurate the location of the DSA holes is, which is called “placement error” (PE). Experimental analysis of PE has been performed in hole shrink patterns. However, it is difficult for the experimental approach to obtain three-dimensional information inside the pattern guide such as the vertical profile of PE. Computational approach can address such difficulties, although, the data are still lacking of examining a variety of DSA patterns. In this report, PE in hole shrink and multiplication is analyzed computationally, and compared with experimental results.

Dissipative particle dynamics (DPD) was chosen as a calculation method for PE analysis, in which whole polymer particles were governed by thermodynamic motion. Guide wall was consisted of fixed molecules, and the affinity was controlled by its composition. Figure 1 shows the time-integrated volume fraction image of the DSA hole after micro-phase separation in cylindrical guide. Affinity of side wall and underlayer was adjusted for resist guide and SiARC based on previous studies, respectively. By dividing serial data at intervals of certain amount of time, a lot of fluctuating centroid position of DSA holes can be obtained. Figure 2(a) is the histogram of the distance between integrated centroid position and time-dependent centroid position. The PE value of 1.86-2.22 nm was deduced from Gaussian fitting, which was comparable to experimental one. Figure 2(b) explains the vertical profile of PE. PE decreased from top to middle of the cylinder. This result implies that the hole at surface region has more fluctuation because of less restrictive condition.

In addition, the effect of guide CD, guide asymmetry, and hole multiplication will be discussed in the presentation.

9423-72, Session PS6

Block copolymer defect annealing kinetics using a coarse grained molecular dynamics model

Andrew J. Peters, Richard A. Lawson, Benjamin D. Nation, Peter J. Ludovice, Clifford L. Henderson, Georgia Institute of Technology (United States)

Directed self-assembly (DSA) of block copolymers (BCPs) is a promising technique for producing sub-30 nm pitch regular patterns using larger lithographically generated template or guiding patterns. The development of such DSA techniques can however be a complex and time consuming process due to the number of variables that can influence the resulting DSA patterning behavior and the inherent difficulties in metrology of the resulting three dimensional heterogeneous thin film structures. DSA development efforts could thus benefit greatly from computer simulations of such methods that accurately capture the essential physics and chemistry of the block copolymer DSA process. For example, concerns about DSA defect density is commonly cited as one of the primary hurdles for the implementation of BCP-DSA into semiconductor fabrication. Ideally, one would like to have knowledge of both the equilibrium number of defects that should be expected in a particular system (i.e. the thermodynamic equilibrium density of defects as might be calculated from defect free energies), whether one is limited in a process by kinetic trapping of defects (i.e. as might be calculated from defect annealing rate measurements or other similar measures), and what factors most significantly influence these defect levels. The inherent dynamic nature of molecular dynamics (MD) simulations and the fact that they allow access to thermodynamic information such as free energies, make coarse-grained MD simulations an excellent tool for fast and detailed studies of defect levels, defect annealing rates, and defect annealing paths. This work has utilized such coarse grained MD simulations of BCP-DSA processes to probe many of these fundamental questions associated with defects in DSA processes.

In particular, this paper will present a study of the dynamics of BCP defect annealing using a coarse-grained BCP-DSA molecular dynamics simulation framework. The effect of χ, N, BCP film thickness, and other relevant system properties on defect levels and annealing rates and pathways have been studied. Prior work by other groups has suggested that a practical upper limit for the χN value that can be used in a BCP-DSA process is approximately 20 due to the onset of kinetically trapped defect states in BCPs with higher χN. In our current work, it has been found that while MD simulations utilizing periodic boundary conditions (i.e. representing an infinitely thick film in principle) show a sharp decrease in defect annealing rate at approximately χN = 20, BCP polymer films with thicknesses on the order of the BCP pattern pitch, as would be more likely representative of real BCP-DSA process, show significantly smaller decreases in defect annealing rate. The cause of these differences in annealing rates, an investigation of the annealing pathways, and an analysis of implications of these results for practical implementation of BCP-DSA processes and materials will be presented.

9423-73, Session PS6

Directed self-assembly of diblock copolymers in cylindrical confinement: effect of underfilling and air-polymer interactions on configurations

Corinne Carpenter, Univ. of California, Santa Barbara (United States); Kris Delaney, Department of Chemical Engineering (United States) and Materials Reasearch Laboratory, UCSB (United States); Nabil Laachi, Glenn H. Fredrickson, Univ. of California, Santa Barbara (United States)

Directed self-assembly (DSA) of block copolymers has attracted attention for its use as a simple, cost-effective patterning tool for creating vertical interconnect access (VIA) channels in nanoelectronic devices. This technique supplements existing lithographic technologies to allow for the creation of high-resolution cylindrical holes whose diameter and placement can be precisely controlled.

In this study, we use self-consistent field theory (SCFT) simulations to investigate the equilibrium configurations and energies of under-filled DSA systems with menisci. In order to simulate systems with AB diblocks (taken here to be PMMA-b- PS with fixed ABN=25) and air, we introduce a third air component “C,” modeled as a polymer of equal length and degree of polymerization as the diblock chains. This C polymer is introduced at the top of the system as homopolymer chains that are neutral to all system walls and interact with the two other blocks with equal Flory-Huggins interaction parameters (ACN=BCNχCN). The use of a polymer rather than a point solvent for the air component is a convenient artifact to fully exclude the species from the polymer film at moderate values of CN; the results are relatively insensitive to chain length.

We report on a series of SCFT simulations of this three species model in cylindrical confinement to explore the role of template diameter, under-fill fraction (i.e. volume fraction of C), along with air-polymer surface interaction (CN) and polymer-side wall/substrate interactions (AWN and BWN), on equilibrium morphologies in an under-filled template with a free top boundary. We identify parameters and system configurations where a stable meniscus appears and explore cases with PMMA-attractive, PS-attractive, and all-neutral walls to understand the effects of wall properties on meniscus geometry and DSA morphology (Fig. 1).

An important outcome is an understanding of the parameters that control

the contact angle of the meniscus with the wall, as it is one of the simplest quantitative measures of the meniscus shape. Ultimately, we seek to identify DSA formulations, templates, and surface treatments with high defect energies, low variation in CD, low placement errors, and a very shallow contact angle, as these factors would facilitate broad process windows and ease of manufacturing.

9423-74, Session PS6

Tilting of lamellar domains on neutral random copolymer brushes

Indranil Mitra, Univ. of Houston (United States); Nikhila Mahadevapuram, Intel Corp. (United States); Joseph Strzalka, Argonne National Lab. (United States); Gila E. Stein, Univ. of Houston (United States)

Thin films of lamellar diblock copolymers can spontaneously self-assemble into nanoscale striped patterns when confined between neutral interfaces. These systems could extend the resolution of projection lithography through processes such as grapho- or chemo-epitaxy. Lithographic applications require lamellar domains that are perfectly perpendicular to the substrate, i.e., the cross-section should resemble a vertical rectangle. However, many studies use surface microscopies to evaluate the thin film structure, so the effects of the buried interface on lamellar ordering are not fully understood.

This study considers the depth-dependent ordering of poly(styrene-b-methyl methacrylate) (PS-PMMA) lamellar copolymers on brushed poly(styrene-r-methyl methacrylate) silicon substrates. The brush grafting density (Σ) and PS-PMMA film thickness (t) were systematically varied from 0.2-0.6 chains/nm2 and 0.5-2.5L0, respectively, where L0 = 46 nm is the equilibrium lamellar periodicity. The outcomes were evaluated with optical microscopy, scanning electron microscopy, and grazing incidence small angle X-ray scattering (GISAXS). The films did not exhibit any roughness or island/hole formation over micrometer length scales, and high resolution imaging revealed the classic lamellar fingerprint pattern at the air interface. However, successive “etching and imaging” steps show that in-plane correlation lengths are reduced in proximity to the substrate, an effect that is particularly pronounced when Σ is low. This finding is not consistent with perfectly perpendicular domains throughout the film thickness. To better understand this behavior, GISAXS measurements were performed at a synchrotron source, and the data were quantitatively analyzed using the distorted-wave Born approximation. This analysis revealed tilted lamellar domains, where the distribution of tilt angles is well-described by a Gaussian function with standard deviation ?. The severity of tilt increases with decreasing Σ from $\sigma \approx 8^{\circ}$ to 15° with little dependence on t.

These changes in lateral and out-of-plane ordering are consistent with a slightly preferential substrate: Random copolymer brushes do not fully screen preferential interactions between PMMA blocks and the underlying silicon, so domains bend/tilt to facilitate PMMA adsorption at the brush/substrate interface, an effect that is exacerbated with low values of ?. These deformations could be stable because the small entropic penalty for these distortions is offset by a reduction in energy at the copolymer-substrate interface. This behavior is not unique to copolymers on brushed substrates, as there is indirect evidence of depth-dependent ordering in literature studies that employ cross-linked neutral coatings, and direct evidence of tilted domains in our own work with neutral silane-coated substrates. These outcomes suggest that GISAXS measurements could provide feedback for high-throughput screening of neutral coating chemistries.

9423-75, Session PS6

Sub-10nm fine lines and spaces patterning using high-chi block copolymers directed self-assembly

Hironobu Sato, Yusuke Kasahara, Shinya Minegishi, Ken Miyagi, Naoko Kihara, Yuriko Seino, Katsutoshi Kobayashi, Hideki Kanai, Katsuyoshi Kodera, Toshikatsu Tobana, Tomoharu Fujiwara, Noriyuki Hirayanagi, Yoshiaki Kawamonzen, Tsukasa Azuma, EUVL Infrastructure Development Ctr., Inc. (Japan)

Recently, directed self-assembly (DSA) attracts semiconductor manufactures as a means for extending ArF immersion lithography. Several practical applications have been reported, such as contact hole shrink [1, 2] and tri-gate structure patterning for finFETs [3]. Since DSA utilized self-assembly of polymer molecules, it is considered to be one of the promising candidates to achieve sub-10nm patterning and beyond [4]. The Froly-Haggins chi parameter is an important characteristic index of block copolymers (BCP). In order to obtain fine DSA patterns, block copolymers with high chi parameter is indispensable.

We utilized grapho-epitaxy to form lines and spaces using high chi block copolymers. Fine DSA patterns were obtained in the guide trenches where width of them was commensurate with the period of the BCPs (Fig.1).

In the conference, dry development of the high chi BCPs, pattern transfer to under layer and defectivety will be discussed.

This work was partly funded by the New Energy and Industrial Technology Development Organization (NEDO) under the EIDEC project. We would like to thank Mr. Satoshi Nomura for his technical support.

References

[1] H.Kato, et.al., Microelecrtonic Engineering 110, pp.152-155 (2013).

[2] Y.Seino, et.al., Journal of Micro/Nanolithography, MEMS, and MOEMS Vol.12 Issue 3, 031305 (2013).

[3] C.Liu, et.al, Proc. SPIE 9049, Alternative Lithographic Technologies VI, 904909 (2014).

[4] International Technology Roadmap for Semiconductors (ITRS), http://www.itrs.net

9423-77, Session PS6

Mapping self-assembled dots and line arrays by image analysis for quantification of defect density, overlay, and alignment

Claudia C. Delgado Simão, Institut Català de Nanotecnologia (Spain); Dmitri Tuchapsky, Andreas Amann, Michael A. Morris, Univ. College Cork (Ireland); Clivia M. Sotomayor Torres, Institut Català de Nanotecnologia (Spain) and Institució Catalana de Recerca i Estudis Avançats (Spain)

Linear or one dimensional nanostructures are a class of elements or components with key technological importance in many areas including electronic and lithography applications, self-assembly templates, x-ray gratings, photonic crystals, etc. Extending the limits of nanofabrication to the nanometre scale had impact on novel materials requirements and suitable specialized metrology. Self-assembled block copolymer (BCP) thin films have been used for fabrication of nanowires, nanopillars and nanopores, competing with the capacity of current photolithography techniques with added value in cost, versatility and simplicity. This self-assembly type technology produces characteristic fingerprint patterns to obtain high density aligned lines patterns on surface using state-of-the-art directed self-assembly (DSA) techniques. These procedures rely on the control of surface properties, either chemical or topological, to create a confinement commensurable with the polymer chains and have a direct impact in their regular arrangement. However, long annealing times and the lack of a defect free long range order pattern are some of the main obstacles that have been addressed, aiming to push forward the successful implementation of this technique in advanced patterning.

Other big challenges towards industrial adaptation are the control of defects and the long range order of these systems, key for the standardization of fabrication processes. Here we present the analysis of linear and hexagonal patterns generated by BCP DSA, based on the image analysis software

presented here, that maps and counts the dot line elements and is able to provide valuable insights about the typical defects from BCP DSA and their formation, namely turns, dislocations, lone and branching points. Such information is crucial for the optimization and tailoring of the assembly process to obtained desired structures. The defect density and the quantification of the alignment are then estimated based on the statistical data gathered by the image analysis.

In addition, key measurands of self-assembled lines such as size, location, overlay and alignment are described via the presented image analysis methodology. Some of the measurands, such as overlay, were found to be material and size dependent. Defect mapping and quantification through this methodology permitted to investigate sub-nm sized defects, and defect densities estimated are in the order of 1E11 defects per square cm. In summary, our work devises a highly specific image analysis method towards line patterns generated by directed self-assembly, with or without graphoepitaxy patterns, able to analyse sub-10 nm nanostructures yielding statistical information on features morphology, order and defectivity quantification. This dimensional nanometrology method has also in line potential due to its optimized computation with ultra-fast response and also is applicable to linear patterns obtained by conventional lithographic techniques.

9423-78, Session PS6

Density multiplication in directed self-assembly of block co-polymers by chemical surface modification using wide guiding stripes

Laura Evangelio, Ctr. Nacional de Microelectrónica (Spain); Marta Fernández-Regúlez, Ctr. Nacional de Microelectrónica (Spain) and CEA-LETI (France); Weihua Li, Georg-August-Univ. Göttingen (Germany); Matteo Lorenzoni, Ctr. Nacional de Microelectrónica (Spain); Celia Nicolet, Christophe Navarro, Arkema S.A. (France); Jordi Fraxedas, Institut Català de Nanociència i Nanotecnologia (ICN2) (Spain); Marcus Müller, Georg-August-Univ. Göttingen (Germany); Francesc Pérez-Murano, Ctr. Nacional de Microelectrónica (Spain)

Directed self-assembly (DSA) of block co-polymers (BCP) by chemical surface modification is driven by interfacial and surface interactions that take place between the co-polymer blocks and the surface. Therefore, to achieve the desired alignment of the BCP, there is a need to create an appropriate chemical pre-pattern, in which the guiding stripes should preferentially interact with one block, whereas the background is either neutral or slightly preferential to the other block. One of the most commonly used techniques to align BCP by chemical epitaxy consists in creating guiding stripes by electron beam lithography (EBL) followed by an oxygen plasma treatment to functionalize the substrate. However, it is becoming difficult to obtain guiding patterns with sufficiently high resolution, as required for the next generation of semiconductor devices.

In this communication, we show that by properly tuning the strength of these interactions, chemical patterns formed by wide backgrounds and guiding stripes can properly direct the alignment of BCP, relaxing the requirements on the lithography process in terms of resolution. In the experiments, brush layers formed by PS-r-PMMA-OH with styrene fractions between 0.6 to 1 are prepared under different annealing conditions and patterned by selective oxygen plasma exposure. Large density multiplication factors are demonstrated for guiding-stripes widths of 2.5L0 (where L0 denotes the periodicity of the lamella-forming BCP).

The process flow for the definition of the desirable features is depicted in figure 1. In a first step, the polymer brush is grafted on a silicon chip. The strength of the surface affinity is measured by characterizing the contact angle between the homo-polymers and the brush layer in dewetting experiments. For the realization of the guiding patterns, a layer of PMMA is deposited on the brush layer by spin-coating, and it is exposed by electron beam lithography. After development, an oxygen plasma process is performed to locally change the surface chemical affinity. The effect of the oxygen plasma consists in slightly increasing the affinity of the surface to the PMMA block of the co-polymer. Different guiding patterns with guiding-stripes widths between 0.5L0 to 2.5L0 and density multiplication factors of X5 have been created.

After removing the resist, a film of PS-b-PMMA is deposited on the chemical patterns and thermally annealed to promote lamellar structure formation. Finally, one of the blocks is removed by reactive ion etching prior to SEM inspection. As BCP, we have used lamella forming PS-b-PMMA of two different pitches: L0=28 nm and 41 nm. We have investigated in detail the dependence of the DSA patterns as a function of process conditions and guiding pattern width. Figure 2 shows some of the patterns obtained for guiding patterns made of wide stripes. The behavior is rationalized by the balance between surface free energy and grain boundary free energy according to the results of self-consistent field theory and simulations.

9423-79, Session PS6

193i lithography design strategies for contact doubling with grapho-epitaxy DSA: a simulation study

Antoine Fouquet, Jérôme Hazart, Loïc Perraud, Sébastien Berard-Bergery, Raluca Tiron, Ahmed Gharbi, Patricia Pimenta-Barros, CEA-LETI (France)

Directed self-assembly (DSA) of block copolymers BCP is a promising candidate for alternative micro lithography due to its cost effectiveness, its ability to reduce critical dimension and to increase pattern density. For contact layer design, grapho-epitaxy combined with cylindrical BCP is the preferential approach. While contact shrink has already been a well-controlled process, contact multiplication is still undergoing further studies. In this study we propose to explore different strategies to design the guiding patterns with 193i lithography for contact doubling with a physical model.

One of the key points when designing a guide to self-assemble BCP is its commensurability with the natural pitch of this BCP. Ignoring this would lead to high number of defects into the structure. Two questions are then following. How far the natural pitch (L0) can be compressed or dilated to address design requirements, depending on the guiding pattern (rectangles, peanut shapes), and what are the effects of guide edges variations induced by scanner process variations.

We propose in this study how those issues will impact the design strategies for 193i lithography combined with DSA.

First, we show how we calibrated our physical model based on DSA specific patterns through contours matching with experimental SEM images. This model is based on a phase field approach (Cahn-Hilliard equation) and numerically solved with Finite Elements Method.

Second, we show that the computed energy given by the physical model of a BCP configuration is related to the defectivity and Contact Placement Error seen on experimental data. Hence a stability criterion can be determined and serves to validate the predictability of the model (i.e. does the computed configuration has a chance to be “real” for a given process)

Finally, the cylindrical BCP Center Placement Error, for given scanner typical errors (focus & dose) is computed and we show that it highly depends on the shape of the guiding pattern, especially when “peanut” shapes are compared to rectangles. We also show that the affinities of the interfaces (underlayer, walls) play an important role in the robustness of the process.

Conference 9423:
Alternative Lithographic Technologies VII

9423-80, Session PS6

Nanomechanical properties of solvent cast PS and PMMA polymer blends and block co-polymers

Matteo Lorenzoni, Francesc Perez Murano, Laura Evangelio, Ctr. Nacional de Microelectrónica (Spain); Christophe Navarro, Celia Nicolet, Arkema S.A. (France)

Atomic force microscopy (AFM) is widely used to image surface topography at the nanometric scale andto map the qualitative differences of local surface properties such as friction, adhesion or elastic modulus. Using PeakForceTM quantitative nanomechanical mapping (QNMTM) is possible to reliably measure Young's modulus of materials with high spatial resolution and surface sensitivity[1]. With this technique is possible to acquire multiple force distance curves with improved force resolution (10-10 N) obtaining real time calculation of mechanical properties at each surface contact. The measure is particularly challenging when the material to be indented is deposited on a rigid substrate and reaches critical thicknesses in the same order of magnitude of the indentation performed.

We apply this technique to characterize the mechanical properties of thin polymer films that are of interest for optimizing the processing and technology of materials used in the area of advanced lithography and directed self assembly of block co-polymers.

In a first study, we have mapped and identified the formation of different phases of PS/PMMA homopolymer blends after dewetting on various substrates that present different affinity with the blend components. The brush layer itself used as a substrate, even if thinner than 5 nm, can be probed and characterized by PeakForce, taking into account that for small thicknesses, tipically < 40 nm, the tip senses the substrate also for very small loads so that the mechanical properties are dominated by the stiff substrate, resulting in rather large modulus values compared to the bulk one[2].

As a second application, we have probed the mechanical properties of BCP thin films oriented by lithographic patterns[3]. Thin films of block copolymers can self-assemble into ordered periodic structures at the molecular scale (5 to 50 nm) with a rich variety of nanophase-separated structures (lamellar, pillars, etc.). AFM nano-indentation brings important information regarding the changes in mechanical properties of the different oriented domains, being able to overcome typical limitations of surface analysis (as in the case of friction maps) by probing few nm underneath the surface. The mechanical stress introduced with orientation can be measured by local changes in the stiffness of the different phases of the BCP differentiating between oriented and non-oriented regions.

In terms of lateral resolution, probing nanometric length structures like the ones created by the self assembly of block co-polymers (BCP)[4], brings the technique to its spatial limits[5]. It is crucial in this sense to use ultra sharp tips (indenters) in order to minimize the indentation depth.

[1] T. J. Young, M. a Monclus, T. L. Burnett, W. R. Broughton, S. L. Ogin, and P. a Smith, "The use of the PeakForce TM quantitative nanomechanical mapping AFM-based method for high-resolution Young's modulus measurement of polymers," Meas. Sci. Technol., vol. 22, no. 12, p. 125703, Dec. 2011.

[2] B. Cappella and D. Silbernagl, "Nanomechanical properties of polymer thin films measured by force–distance curves," Thin Solid Films, vol. 516, no. 8, pp. 1952–1960, Feb. 2008.

[3] L. Oria, A. R. De Luzuriaga, J. A. Alduncin, and F. Perez-murano, "Polystyrene as a brush layer for directed self-assembly of block co-polymers," Microelectron. Eng., vol. 110, pp. 234–240, 2013.

[4] S. O. Kim, H. H. Solak, M. P. Stoykovich, N. J. Ferrier, J. J. De Pablo, and P. F. Nealey, "Epitaxial self-assembly of block copolymers on lithographically defined nanopatterned substrates.," Nature, vol. 424, no. 6947, pp. 411–4, Jul. 2003.

[5] E. T. Herruzo, A. P. Perrino, and R. Garcia, "Fast nanomechanical spectroscopy of soft matter.," Nat. Commun., vol. 5, p. 3126, Jan. 2014.

9423-81, Session PS6

Creation of guiding patterns for directed self-assembly of block co-polymers by resistless direct e-beam exposure

Laura Evangelio, Ctr. Nacional de Microelectrónica (Spain); Marta Fernández-Regúlez, Ctr. Nacional de Microelectrónica (Spain) and CEA-LETI (France); Xavier Borrisé, Matteo Lorenzoni, Ctr. Nacional de Microelectrónica (Spain); Jordi Fraxedas, Institut Català de Nanociència i Nanotecnologia (ICN2) (Spain); Francesc Pérez-Murano, Ctr. Nacional de Microelectrónica (Spain)

One of the most appropriate methods to direct self-assembly (DSA) block co-polymers (BCP) consists on creating chemical patterns on the top of a polymer brush layer. By properly tuning the chemical affinity between this brush layer and the co-polymer, highly oriented and ordered structures can be achieved. The most commonly used techniques to create chemical guiding patterns are based on deep UV lithography or electron beam lithography (EBL). However, in both cases it is becoming difficult to obtain guiding patterns with enough resolution, as required for the next generation of semiconductor manufacturing. Furthermore, a high number of steps are involved in the process due to the necessity of using a radiation sensitive resist in the patterning process.

In this communication, we present a novel approach for the creation of chemical guiding patterns to direct the self-assembly of PS-b-PMMA (L0 = 28 nm). The chemical guiding stripes are created directly on a PS-OH brush layer by exposing it to electrons, causing the crosslinking of polystyrene molecules and changing its chemical affinity to the blocks of the BCP. The resulting process is much simpler than the proposed in previous works since there is no need of spinning a resist, and thus reducing the number of processing steps involved. The overall process flow is depicted in figure 1 and it shows how the chemical guiding patterns are created.

First, the polymer brush layer is spin coated and annealed. In order to understand the chemical interactions that take place between the polymer brush and the BCP, an extensive characterization of the brush layer surface has been carried out. This characterization includes the measurement by AFM of the contact angle between the homo-polymers (PS and PMMA) and PS-OH, and XPS analysis to determine the composition of the brush after its annealing.

The guiding stripes are created by direct exposing the brush layer to electrons using a dedicated e-beam lithography system. An extensive study of the e-beam dose has been performed in order to find the optimal conditions which allow the properly alignment of the BCP. In order to comprehend which chemical changes are taking place when polystyrene is exposed directly by electrons, a second XPS analysis has been performed after creating the chemical pattern. Finally, the BCP is spin-coated and it self-assembles after a thermal annealing. The samples are characterized by SEM after removing the PMMA block by an O2 plasma treatment. The results show that the chemical guiding stripes are more attractive to polystyrene block due to its crosslinking (figure 2). Challenges and opportunities of this method will be discussed in the presentation.

9423-82, Session PS6

A simulation study for 3D defects in directed self-assembly lithography

Hideki Kanai, Katsuyoshi Kodera, Yuriko Seino, Hironobu Sato, Yusuke Kasahara, Katsutoshi Kobayashi, Ken Miyagi, Shinya Minegishi, Naoko Kihara, Yoshiaki Kawamonzen, Tomoharu Fujiwara, Noriyuki Hirayanagi, Toshikatsu Tobana, Tsukasa Azuma, EUVL Infrastructure Development Ctr., Inc. (Japan)

Recently, directed self-assembly (DSA) with lamellae phase block copolymer

has had a great progress for manufacture of semiconductor devices, but topological defects such as dislocation and disclination still remains a major concern. 3-dimensional (3D) buried defects [1-3] with staggered structures may also appear if materials, processes and integrations are not optimized for chemo or grapho-epitaxy flows, then it will cause poor etch selectivity and bad line edge roughness (LER) in their pattern transfers into underlayers. In this study, we will discuss defect analysis, in which specific types of buried defects found in our process are included. Our process uses a coordinated line epitaxy having both chemo- and grapho-epitaxy features without special pinning guide materials to control surface free energy on guide line patterns and resist strip process. The buried defects can obviously be seen in PMMA dry development after micro-phase separation of polystyrene-block-poly(methyl methacrylate) (PS-b-PMMA). The defect analysis was carried out using self-consistent field theory (SCFT) simulation for various top, bottom, pinning dimensions, AB block composition and surface affinity by calculating free energy difference among several phase configurations (Fig. 1).

This work was partly funded by the New Energy and Industrial Technology Development Organization (NEDO) under the EIDEC project.

References

[1] Marcus Müller, Kostas Ch. Daoulasa, Yuki Norizoe, Phys. Chem. Chem. Phys., 11, 2087-2097 (2009)

[2] Chi-Chun Liu, Abelardo Ramírez-Hernández, Eungnak Han, Gordon S. W. Craig, Yasuhiko Tada , Hiroshi Yoshida , Huiman Kang, Shengxiang Ji, Padma Gopalan, Juan J. de Pablo, Paul F. Nealey, Macromolecules, 46, 1415-1424 (2013)

[3] Richard A. Farrell, Erik R. Hosler, Gerard M. Schmid, Ji Xu, Moshe E. Preil, Vinayak Rastogi, Nihar Mohanty, Kaushik Kumar, Michael J. Cicoria, David R. Hetzer, Anton DeVilliers, Proc. SPIE 9051, 90510Z (2014)

9423-83, Session PS6

Increasing ease of implementation for self-assembled block copolymers (BCPs) using modified polystyrene (PS) block techniques

Mary Ann J. Hockey, Brewer Science, Inc. (United States)

Conventional polystyrene block poly(methyl methacrylate) (PS-b-PMMA) has been successfully used to study process integration requirements when using directed self-assembly (DSA) flows with values of L0 measuring 28-30 nm. We offer a simplified path for implementing graphoepitaxy DSA flows with excellent photolithographic capabilities. Initially, Brewer Science developed a multifunctional hardmask neutral layer (HM NL) to improve etch resistance capabilities and match the surface energy properties required for conventional block copolymers (BCPs) such as PS-b-PMMA. In this work, a separate brush layer is replaced by incorporating neutral layer properties into our hardmask to achieve microphase separation of the BCP during thermal annealing. In addition to providing a robust neutral layer, we continue to address the industry need to have available alternative solutions to increase the ease of implementing DSA and bridging the gap until ultrahigh-chi materials become commercially available. To meet this interim need, a series of BCP formulations were synthesized using the approach of enhancing the PS block of the BCP material. We achieved L0 values ranging from 28 nm to as low as 18 nm. We focused on providing the ability to withstand rigorous processing conditions such as harsh etch gas chemistries and surface energy modulations. Quality “fingerprint” patterns or microphase separation using thermal annealing was achieved for an array of modified BCP materials. No topcoat or solvent annealing was required to achieve alignment of the BCP inside templated graphoepitaxy features. All modified PS BCP formulations were coated directly onto both “brush” layers and the multifunctional HM NL for a direct comparison of their capabilities.

9423-84, Session PS6

An in situ study of kinetics of rapid self-assembly in block copolymer thin films during solve- microwave annealing

Parvaneh Mokarian-Tabari, Univ. College Cork (Ireland) and Tyndall National Institute (Ireland) and Trinity College Dublin (Ireland); Cian Cummins, Univ. College Cork (Ireland); Raj Sola, Technical Univ. of Denmark (Denmark); Claudia C. Delgado Simão, Institut Català de Nanociència i Nanotecnologia (ICN2) (Spain); Clivia M. Sotomayor Torres, Institut Català de Nanociència i Nanotecnologia (ICN2) (Spain) and Institució Catalana de Recerca i Estudis Avançats (Spain); Justin D. Holmes, Michael A. Morris, Univ. College Cork (Ireland) and Tyndall National Institute (Ireland) and Trinity College Dublin (Ireland); Timothy Collins, Univ. College Cork (Ireland) and Tyndall National Institute (Ireland)

Microwave annealing is an emerging technique for achieving ordered patterns of block copolymer films in substrates within seconds [1], although little detailed understanding of how microwave annealing promotes the microphase separation of the blocks exists. Here, we use controlled power microwave irradiation in the presence of a solvent tetrahydrofuran (THF), to achieve lateral microphase separation in high chi lamellar forming poly(styrene-b-lactic acid) PS-b-PLA. A highly ordered line pattern was formed within seconds on a silicon substrate. In situ temperature measurement of the silicon substrate coupled to condition changes during “solvo-microwave” annealing allowed understanding of the processes to be attained. Our results suggest that the substrate has a secondary effect on the ordering process but rather, it is direct heating of the polar THF molecules that causes microphase separation. It is postulated that the rapid interaction of THF with microwaves and the resultant temperature increase to 55 ºC within seconds causes an increase of the vapor pressure of the solvent from19.8 kPa to 70 kPa or possibly higher. This enriched vapor environment increases the plasticity of both PS and PLA chains and leads to the fast self-assembly kinetics [1]. Comparing the patterns formed on silicon, germanium and silicon on insulator (SOI) and also an in situ temperature measurement of silicon in the oven confirms the significance of the solvent over the role of substrate heating during “solvo-microwave” annealing. Besides the short annealing time (~ 60 seconds) which has technological importance, the coherence length is on a micron scale and dewetting is not observed after annealing [2,3]. The etched pattern (PLA was removed by an Ar/O2 reactive ion etch) was transferred to the underlying silicon substrate [4] fabricating sub-20 nm Si nanowires over large areas demonstrating that the morphology is consistent both across and through the film.

References

[1] Zhang, X. J.; Harns, K. D.; Wu, N. L. Y.; Murphy, J. N.; Buriak, J. M., Fast Assembly of Ordered Block Copolymer Nanostructures through Microwave Annealing. ACS Nano 2010, 4 (11), 7021-7029.

[2] Mokarian-Tabari, P., Cummins C., Rasappa R., Simao C., Sotomayor Torres C.M., Holmes J.D. and Morris M.A., “A Study of the Kinetics and Mechanism of Rapid Self- assembly in Block Copolymer Thin Films during “Solvo-microwave” Annealing”, Langmuir, Publication date: 19 August 2014, DOI: 10.1021/la503137q

[3] Simão, C. T., D.; Khunsin, W.; Amann, A.; Morris, M. A.; Sotomayor Torres, C. M. In Defect Analysis and Alignment Quantification of Line Arrays Prepared by Directed Self-assembly of a Block Copolymer, SPIE Proceeding 9050, 905028, 2014.

[4] Cummins, C.; Mokarian-Tabari, P.; Holmes, J. D.; Morris, M. A., Selective Etching of Polylactic Acid in Poly(styrene)-block-poly(D,L)lactide Diblock Copolymer for Nanoscale Patterning. J. Appl. Polym. Sci. 2014, 131.

9423-85, Session PS6

Study of DSA interaction range (DSAIR) using Gaussian convolution

He Yi, Stanford Univ. (United States); Joost P. Bekaert, Roel Gronheid, IMEC (Belgium); Germain L. Fenger, Mentor Graphics (Belgium); Kathleen Nafus, Tokyo Electron America, Inc. (United States); H. S. P. Wong, Stanford Univ. (United States)

Due to the continuous scaling of semiconductor devices, traditional conventional lithography is facing increasing challenges. Among all potential alternative patterning approaches, Directed Self-Assembly (DSA) of block copolymers (BCP) has attracted significant interest and attention due to low manufacturing cost and can be extended to sub-20 nm feature sizes on a sub-40 nm pitch that exceeds the capability of any single patterning lithography [1-4]. Realizing that most challenging IC layout patterns are irregular and that patterning them does not require any long range order [5-7], we adopted small topographical physical templates to flexibly generate and control aperiodic DSA patterns [8]. In previous studies, researchers have demonstrated that DSA patterns are determined not only by the size and shape of guiding templates, but the template density as well [9]. However, the influence of the pattern density has not been explored systematically. We will first introduce the concept of DSA Interaction Range (DSAIR). Then we investigate the influence of template density on the DSA patterns using Gaussian convolution. This approach provides us with a quantitative way to model the influence of template density and predict the location of overfilled conditions.

DSAIR is akin to the concept of interaction range in optical lithography, describing a certain range that template density starts to influence DSA patterns. It is not fixed and process-related. As the starting point, we focus on the 1-hole DSA pattern. Peanut-shape and multi-hole patterns are likely to behave similarly. In our experiment results we observed the overfilled templates appeared mostly at the corners and edges of our design block, which look like “disappeared” from a zoom-out view (Fig. 1a), while the not-overfilled templates have much higher contrast around the template edge. The distribution of the overfilled templates is caused by the fact that the density at the block corner is actually much lower than the density in the center. And lower template density leads to more reflow into the templates and tends to turn them overfilled. Therefore we choose the low-magnification SEM images to visually inspect the distribution of the overfilled templates, and we find that the distribution of the not-overfilled templates could be approximated by the Gaussian convolution of the template block. This Gaussian convolution takes the density of the guiding templates and a chosen sigma value as the input and outputs the convoluted density map (Figure 1d). There exists a set of best-fit sigma value for this Gaussian convolution. This Gaussian convolution function, once established, could be used to estimate the influence of guiding template density on DSA patterns that adopts the same process. Given the circuit layout and DSA process, we can use this Gaussian convolution function to detect the spot where the density influence is going to take place and result in overfilled conditions. It would provide an important input to the DSA models for predicting density influence for a given circuit layout, as well as providing a potential solution for correcting the influence (e.g. through sub-resolution DSA Assist Features (SDRAF)).

9423-86, Session PS6

Surface energy control for contact hole shrinkage using DSA

Kuan-Hsin Lo, Chieh-Han Wu, Ching-Yu Chang, Chung-Ju Lee, John Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

Directed Self-Assembly (DSA) has the potential to reduce critical feature sizes to 10 nm and beyond. Hence, it has been widely studied for pitch reduction, contact hole shrink, pattern profile smoothing, and pattern collapse improvement. In this paper, our study of substrate property for the formation of hole shrinking by DSA is reported. The DSA hole shrinkage process uses standard trilayer patterning to form the seeding pattern for graphoepitaxy. Several etching recipes were optimized to develop the guider pattern in the underlayer and to produce different surface properties at the bottom stop film for BCP filling and assembling. When etching finishes with hydrophobic gas, a hydrophobic bottom surface is created. To make the bottom surface more hydrophilic, etching would end with oxygen plasma. This provides an alternative to control the surface properties to improve the DSA formation. Several DSA shrink methods and their resultant defects will be reported and discussed in this paper, with an emphasis on different kinds of ending plasma conditions.

9423-87, Session PS6

Barriers to defect melting in chemo-epitaxial directed self-assembly of lamellar-forming diblock copolymer/ homopolymer blends

Kenichi Izumi, JSR Engineering Co., Ltd. (Japan) and The Materials Research Lab. (United States) and Univ. of California, Santa Barbara (United States); Bongkeun Kim, Nabil Laachi, The Materials Research Lab. (United States) and Univ. of California, Santa Barbara (United States); Kris T. Delaney, The Materials Research Lab. (United States); Michael Carilli, Univ. of California, Santa Barbara (United States); Glenn H. Fredrickson, The Materials Research Lab. (United States) and Univ. of California, Santa Barbara (United States)

Directed self-assembly (DSA) has recently attracted attention as a next-generation patterning technique to complement conventional photo-lithography. The reduction of defect concentrations in the self-assembled microdomains remains an important challenge for full integration in lithographic applications. From previous experimental and computational studies, pairs of dislocations are the most observed defects in line and space structures.

In this study, we use self-consistent field theory (SCFT) to investigate the formation energy of defects in lamellar-forming blends of AB block copolymers and A or B homopolymers on chemically prepatterned substrates. We also use the string method coupled with SCFT to investigate transition pathways and the kinetic barriers for melting of elementary dislocation pair defects into perfect lamellar morphologies.

From preliminary 2D simulations, while the dislocation pair has two T-junctions in the A-domain, no junction is present in the B-domain. A similar dislocation pair was obtained not only for the pure block polymer but also for the blended system. Similarly, 2D string calculations reveal morphologies during the melting of defects in blended systems comparable to those observed in pure melts. However, in the transition from a dislocation pair to a single dislocation, while the first barrier height increased from 10.2kT in the pure melt to 16.0kT in the blend with added A-homopolymer, it decreased to 9.1kT by the addition of B-homopolymer. As seen in the density profiles of the added homopolymer in Fig.1, homopolymer localization at the T-junction core was observed in the A-homopolymer blend. In this case, the T-junction appears to reinforce the defect stability via a large transition barrier. On the other hand, the addition of B-homopolymer did not result in any localization during the transition to the single dislocation state. The barrier height in this case is slightly decreased relative to that in the pure block copolymer melt. In the second energetic barrier from the single dislocation to perfect lamellae, the kinetic barrier was 0.5~1kT higher in all blend formulations than that in the pure block because homopolymer localization was observed in the T-junction for both A and B homopolymer addition.

Our findings from the 2D simulations suggest that the presence of A or B homopolymer in an AB block polymer melt affects the morphological stability of defective structures. More detailed 3D SCFT simulations with

chemically-patterned substrates will be conducted to test these findings in situations closer to those realized in experimental manifestations of line-space chemoepitaxy.

1. S. Xiao et al., J. Microlith. Microfab. 12, 3 (2013).

2. L. Wan et al., J. Microlith. Microfab. 11, 3 (2012).

9423-22, Session 7

Impact of materials selection on graphoepitaxial directed self-assembly for line-space patterning

Phillip D. Hustad, Dung Quach, Dow Electronic Materials (United States); Valeriy V. Ginzburg, The Dow Chemical Co. (United States); Mingqi Li, Peter Trefonas III, Dow Electronic Materials (United States); Dan B. Millward, Gurpreet S. Lugani, Scott L. Light, Micron Technology, Inc. (United States)

Directed self-assembly (DSA) of block copolymers (BCPs) is a promising technology for advanced patterning at future technology nodes, but significant hurdles remain for commercial implementation. To address these challenges, we have focused our development on more strongly segregated "high chi" block copolymers with a particular emphasis on cylinder-morphology BCPs in graphoepitaxial DSA applications for line-space patterning. In this approach, cylinder-forming block copolymers are applied onto a brush-coated surface with periodically spaced confining walls or "weirs". This paper will discuss several important materials parameters and their impact on DSA patterning, including the impact of brush chemistry, block copolymer chi parameter and glass transition temperature, etch performance, and formulation. Simulations will also be presented to guide materials and process and enhance our understanding of the observed DSA results. In particular, we will demonstrate the extension of the SCFT model to explicitly account for the brush layer and determine its impact on defect formation energy.

9423-23, Session 7

Challenge and opportunity in hexagonal and rectangular bit-patterned media template fabrication

Shuaigang Xiao, Xiaomin Yang, Yautzong Hsu, Kim Lee, David Kuo, Seagate Technology LLC (United States)

As a promising next-generation magnetic recording technology, bit-patterned media (BPM) development is under intense research by hard disk drive industry now. The first topic to be covered before talking about high-volume manufacture of BPM disks is fabricating high density BPM templates containing proper servo information for full-track read/write demonstration. Pattern transfer and servo integration are the two key points of BPM template fabrication, since directed self-assembly (DSA) of block copolymers is adopted as the lithography solution to set the pattern resolution. Research status of our lab on BPM will be updated for both hexagonal BPM approach1 and rectangular BPM approach2.

A silicon-containing block copolymer, PS-b-PDMS, is used as a model system for the application of both dot patterning (for hexagonal BPM) and line patterning (for rectangular BPM). Results on servo-integrated hexagonal BPM&templates up to 2 teradot/in2 will be illustrated. Besides, rectangular BPM seem to provide more flexibility for designing arbitrary bit architectures, by tuning cross-patterning for creating 2-D dot patterns using two 1-D line patterns with a quasi-orthogonal relationship. In that case, LER&LWR control in DSA patterns is critical to ensure final 2-D dot pattern quality. As shown in Figure 1, quality of PS-b-PDMS line patterns seems to deteriorate with smaller block copolymer nanodomains. Effects of the anneal condition and the molecular weight of block copolymers will be evaluated. Nonetheless, a DSA line pattern with 14 nm pitch has been achieved so far. Pattern transfer challenges of such narrow lines will be discussed.

9423-24, Session 7

Directed self-assembly of ABA triblock copolymer on chemical contrast pattern via solvent annealing: molecular architecture, solvent selection, and pattern transfer

Shisheng Xiong, The Univ. of Chicago (United States); Lei Wan, Yves-Andre Chapuis, Ricardo Ruiz, HGST (United States); Paul F. Nealey, The Univ. of Chicago (United States)

The directed self-assembly of symmetric ABA, poly (2-vinylpyridine-styrene-b-2-vinylpyridine) (P2VP-b-PS-b-P2VP) triblock copolymer on chemical contrast pattern, was accomplished using solvent annealing. The perpendicular lamellae with sub-10nm scale can be guided by sparse chemical patterns to form long-rang ordered, dewetting-free, and registered periodic array of features. The comparison in terms of processing window such as brush neutrality and thickness commensurability, between diblock and triblock of the same composition, will be discussed. The assembly dynamics and vitrified pitch size can both be altered by choosing different but neutral annealing solvents. Sequential-infiltration-synthesis (SIS) enhanced pattern transfer has also been investigated in details, on different cycles, purge/soak time and operating temperature.

9423-25, Session 7

Selective laser ablation in resists and block copolymers for high-resolution lithographic patterning

Deirdre L. Olynick, Pradeep N. Perera, Adam M. Schwartzberg, Lawrence Berkeley National Lab. (United States); Nathan D. Jarnagin, Clifford L. Henderson, Georgia Institute of Technology (United States); Zhiwei Sun, Lawrence Berkeley National Lab. (United States) and Univ. of Massachusetts Amherst (United States); Ilja Gunkel, Lawrence Berkeley National Lab. (United States); Thomas P. Russell, Lawrence Berkeley National Lab. (United States) and Univ. of Massachusetts Amherst (United States); Matthias Budden, Ivo W. Rangelow, Technische Univ. Ilmenau (Germany)

Previously, we demonstrated an all dry, selective laser ablation development (SLAD) in methyl acetoxy calixarene (MAC6) which produced high resolution, high aspect ratio features not achievable with wet development.1, In this paper, we investigate selective ablation in block copolymer systems. This offers an alternative to block removal using plasma etching when selectivity cannot be achieved.

We use a 532 nm CW laser (spot size ~600 nm and power density 2-4 MW/cm2) and scan over block copolymer patterns of polyhydroxystyrene-b-polystyrene (PHOST-PS) and polyvinylpyridine-b-polystyrene (PHOST-PVP). Optical absorption contrast promotes ablation of the higher absorbing regions over the overall non-absorbing regions (polystyrene). Unlike direct write laser ablation, the final pattern resolution is determined by the size of the chemical patterns and not the laser spot size. For instance, in electron beam lithography of MAC6, the 10-20 nm e-beam exposed regions ablate in the 600 nm spot size laser producing aspect ratios up to 4:1 in 15 nm half-pitch patterns whereas in the BCP systems, the block sizes determines the ablated pattern resolution. We study in detail the ablation characteristics of

the BCP materials, including neutral alignment layers, as a function of laser power using Raman spectroscopy. For the ablated materials, we identify a multi-photon ablation mechanism. In addition, material functionality, temperature, and ambient conditions all play an important role in the process. In the PHOST-b-PS system, we are able to ablate and leave behind polystyrene features whereas in the PVP-b-PS system blocks are PVP blocks are removed, but with less selectivity. Block copolymer pitches down to 20 nm have been investigated.

1 Oteyza, D. G. d.; Perera, P. N.; Schmidt, M.; Falch, M.; Dhuey, S. D.; Harteneck, B. D.; Schwartzberg, A. M.; Schuck, P. J.; Cabrini, S.; Olynick, D. L., Sub-20 nm laser ablation for lithographic dry development. Nanotechnology 2012, 23 (18), 185301.

2 Perera, P. N., et al. (2012). Selective laser ablation of radiation exposed methyl acetoxy calix(6)arene. J. Vac. Sci. Technol. B. 2012, 30 (6), 06FI02-1

This work was supported in part by the U.S. Department of Energy under Contract No. DE-AC02-05CH11231. Addition support was provided by Seagate (Z.S.)

9423-26, Session 8

Toward high-performance quality meeting IC device manufacturing requirements with AZ SMARTTM DSA process

JiHoon Kim, Jian Yin, Yi Cao, AZ Electronic Materials USA Corp. (United States); YoungJun Her, AZ Electronic Materials (Korea) Ltd. (Korea, Republic of); Hengpeng Wu, Jianhui Shan, Durairaj Baskaran, AZ Electronic Materials USA Corp. (United States); Tomohiko Tsutsumi, AZ Electronic Materials (Japan) K.K. (Japan); Guanyang Lin, AZ Electronic Materials USA Corp. (United States)

Significant progresses on 300mm wafer level DSA (Directed Self-Assembly) performance stability and pattern quality were demonstrated in recent years. DSA technology is now widely regarded as a leading complementary patterning technique for future node integrated circuit (IC) device manufacturing. We first published AZ SMARTTM DSA flow in 2012. In 2013, we demonstrated that AZ SMARTTM DSA pattern quality is comparable to that generated using traditional multiple patterning technique for pattern uniformity on a 300mm wafer. In addition, we also demonstrated that less than 1.5nm/3sigma LER (line edge roughness) for 16nm half pitch DSA line/space pattern is achievable through AZ SMARTTM DSA process. However, overall 300mm wafer DSA defectivity is still remaiding as an unanswered question for IC manufacturing. In this publication, we will update recent performance improvements on AZ SMARTTM DSA flow with focuses on 300mm wafer performance process window, pattern formation stability, CD uniformity and pattern etching transferability. DSA defectivity will be discussed as well.

9423-27, Session 8

Fin formation using graphoepitaxy DSA for SOI FinFET device fabrication

Chi-Chun Liu, Fee Li Lie, IBM Corp. (United States); Vinayak Rastogi, Nihar Mohanty, TEL Technology Ctr., America, LLC (United States); Hsinyu Tsai, IBM Thomas J. Watson Research Ctr. (United States); Kafai Lai, Melih Ozlem, IBM Corp. (United States); Wooyong Cho, Sung Gon Jung, SAMSUNG Electronics Co., Ltd. (United States); Jay Strane, IBM Corp. (United States); Mark H. Somervell, Tokyo Electron America, Inc. (United States); Sean D. Burns, Nelson M. Felix, IBM Corp. (United States); Michael A. Guillorn, IBM Thomas J. Watson Research Ctr. (United States); David Hetzer, Akiteru Ko, TEL Technology Ctr., America, LLC (United States); Matthew E. Colburn, IBM Corp. (United States)

Directed self-assembly (DSA) of block copolymers (BCPs) is an alternative approach to extend optical lithography, which utilizes a topographical or chemical guiding pattern to direct the BCPs into a desired morphology at a pre-determined location while the material properties of the BCPs control the feature size and uniformity of the resulting structures. Such a technique has drawn great attention in semiconductor, hard disk drive, and non-volatile memory applications due to its capability for pattern density multiplication and defect rectification. Recent studies on 193i/High Volume Manufacturing (HVM) compatibility, defectivity, and device demonstration of DSA further reinforce its role as a potential candidate for lithography extension rather than merely a lab-scale nanofabrication method.[1-3] However, as pattern density increases, the conventional approach for Fin structure formation in FinFET device fabrication, i.e. removing or preserving one single or multiple lines in a dense array, is limited by the combined effect of CD uniformity, LER/LWR, and placement error control of the lithography system. Recent study showed that the required placement accuracy for sub-30nm pitch pattern is beyond the capability of current manufacturing tolerance and design space constraints.

In this work, fin formation and customization is redesigned as critical cut, which is parallel to fin, and less-critical cut, which is perpendicular to fin. The critical cut pattern is then utilized as the guiding pattern for graphoepitaxy DSA, hence, the resulting fins will self-align to the critical cut patterns. Once the DSA pattern is transferred to the under-layers, a tone-inversion process is applied so that the PMMA domain in BCPs becomes the final fin structure in the SOI, as shown in Fig. 1. This approach has been validated with similar material set using e-beam lithography for critical patterns.[4] Now a first attempt of using 300mm 193i lithography tool together with a HVM-compatible tool set and processes to generate customized SOI fins at 28nm-pitch, including the critical and less-critical cut, will be presented. Fig. 2 shows the guiding pattern designs and the corresponding DSA results, which demonstrates that the non-critical area could have defects since those will be removed later by the cut process. The challenges and learnings in DSA process optimization, pattern transfer tuning, and integration scheme will be further discussed. In addition, the structural results and preliminary learnings from device fabrication will be illustrated. At last, the extendibility of using DSA for devices with smaller pitches will be discussed as well.

9423-28, Session 9

Smart plastic functionalization by nanoimprint and injection molding *(Invited Paper)*

Maksim Zalkovskij, Lasse H. Thamdrup, Kristian Smistrup, Thomas Andén, Alicia C. Johansson, NIL Technology ApS (Denmark); Niels Jørgen Mikkelsen, CemeCon Scandinavia A/S (Denmark); Morten H. Madsen, Jørgen Garnæs, DFM A/S (Denmark); Tommy T. Kristiansen, Mads Diemer, LEGO System A/S (Denmark); Michael Døssing, TOOLpartners® A/S (Denmark); Daniel Minzari, Peter T. Tang, IPU (Denmark); Anders Kristensen, Rafael J. Taboryski, DTU Nanotech (Denmark); Søren Essendrop, SE Design (Denmark); Theodor Nielsen, Brian Bilenberg, NIL Technology ApS (Denmark)

By modifying a surface with specifically designed nano-patterns, extraordinary properties such as, self-cleaning, strong-adhesion, super-hydrophobic, change of friction and coloration by diffraction or plasmons can be achieved. Particularly coloration by nano-patterns have gained a massive interest from the industrial world due the wide range of color effects that can be obtained without any use of pigments. It only takes a look at a butterfly to see the enormous variety of colors nano-patterns can provide. As illustrated in Fig. 1, the highly complex nanostructures

of butterfly wings, can be simplified and made suitable for micro- and nanofabrication, and at the same time maintain their colors. There are several techniques today that enable nano-structuring of surfaces such as e-beam lithography, deep ultraviolet lithography and nano-imprint lithography. However, those techniques are difficult to implement in large volume production of 3D plastic objects. Injection molding on the other hand is a fast, cost efficient and widely used process for large volume production of plastic parts. Standard commercial injection molding tools are poorly suited for the application of micro- and nano structures due to their rough surfaces (compared to a silicon wafer), complex forms and material composition.

In this work a nanoimprint lithography process suitable for imprinting on commercial injection molding tools has been developed together with a method to transfer the imprinted pattern onto the injection molding tool. This allows for direct nano-scale patterning of plastic parts by injection molding.

Using flexible high-resolution polymer stamps we have achieved a high quality nano-pattern transfer on a surface of a standard injection molding steel tools as shown in Fig. 2a-c. The surface roughness is described by an optical method where a characteristic values of the scattered light, Aq is measured for the surfaces. In this study, surfaces with an Aq value of approximately 3 are used. For comparison an Aq value of 0.7 is obtained for a polished silicon surface. The total nano-patterned area is 16x16 mm2, and contains line-gratings with a pitch of 700 nm to 1400 nm. Such a pattern displays coloration due to diffraction of light. Figure 2d shows the nanostructured plastic parts achieved by injection molding with the nano-patterned steel tool. The plastic parts have been injection molded using a standard injection molding process. A durability test have reviled no detectible damages to the nanostructures in the injection molding tool after the production of more than 40,000 plastic parts (the life time test is still ongoing).

Even smaller structures have been transferred onto commercial injection molding steel tools with the above described process. Figure 3 shows an optical image, SEM and AFM of a steel tool onto which a pattern with a resolution of only 100 nm, 200 nm pitch, have been transferred.

Here, decorative color effects have been presented. However, the described processing of steel tools, are adaptable for other functionalities such as super-hydrophobic, self-cleaning and anti-reflective patterns.

This work was supported by InnovationsFonden (NanoPlast, grant no: 007-2010-2) and from the European Community's Seventh Framework Programme (Plast4Future, grant no: 314345).

9423-29, Session 9

Development of NIL processes for PV applications

Hubert Hauser, Nico Tucher, Katharina Tokai, Patrick Schneider, Christine Wellens, Anne-Kristin Volk, Simon Barke, Fraunhofer-Institut für Solare Energiesysteme (Germany); Claas Müller, Univ. of Freiburg (Germany); Thomas Glinsner, Gerald Kreindl, EV Group (Austria); Benedikt Bläsi, Fraunhofer-Institut für Solare Energiesysteme (Germany)

Due to its high resolution and applicability for large area patterning, Nanoimprint Lithography (NIL) is a promising technology for PV applications. Possible applications in this field concern the optical properties (light in-coupling [1], light trapping [2], plasmonics [3]) or the patterning of device features (e.g. metallization, diffusion barriers). However, the requirements set by PV industry, especially for the fabrication of wafer-based silicon solar cells, are not easy to meet. Typical wafer sizes are 156 x 156 mm? and thicknesses are only about 180 μm. According to the International Technology Roadmap for Photovoltaic [4] thicknesses are even to be decreased within the next years to below 150 μm. This is both a challenge to perform NIL processes on such thin and brittle large area substrates as well as a chance to introduce novel processes into fabrication as sophisticated photon management structures will gain in importance. Such structures will be required to maintain high absorption and thus high quantum efficiencies. Besides the thickness, also the surface roughness due to the wire sawing and the total thickness variation of about 10 % are demanding for NIL processes.

In this work, the development of NIL processes on the novel Smart-NIL technology from EVG with a focus on PV applications is described. In this tooling, a soft stamp is used to imprint onto a resist coated substrate. The demolding of the stamp in particular is crucial when handling very thin substrates. Therefore, this step has to be realized as a very controlled sequential process, where the stamp is demolded smoothly starting on one side and being peeled off to the other side. Aspects like adaptability to uneven surfaces are tackled by using soft stamps made of PDMS or other materials. Homogeneous residual layers can be achieved by applying a uniform pressure using soft polymeric stamps.

Applications that will be presented are the realization of honeycomb textures on multicrystalline silicon solar cells, the integration of features for fine line metallization (width approx. 10 μm) into the templates for such textures and the fabrication of very fine metal contacts with prismatic profiles (width approx. 2 μm) for use in highly efficient multi-junction solar cells. In the context of the honeycomb texturing, interference lithography (IL) as mastering technology will be introduced and the efficiency enhancement of more than 0.5 %absolute on large area multicrystalline silicon solar cells (156 x 156 mm?) processed using an industrial scale pilot line will be presented. For the integration of features for metal contacts already in the template used for the stamp fabrication for NIL processes, different lithographic processes are combined (IL, photolithography, NIL). In the last application, prismatic silver fingers with a width of 2.5 μm and a height of around 2 μm are realized using NIL, evaporation and lift-off. Using such contact fingers, the effective shading can be minimized by redirecting light from the finger onto the solar cell.

[1] Hauser, H., et al., IEEE Journal of Photovoltaics, 2012. 2(2): p. 114-122.

[2] Mellor, A., et al., Optics Express, 2013. 21(S2): p. A295.

[3] Meisenheimer, S.-K., et al., Optical Materials Express, 2014. 4(5): p. 944-952.

[4] Semi PV, International Technology Roadmap for Photovoltaic (ITRPV) 2014.

9423-30, Session 9

Line-width tuning and smoothing for periodic grating fabrication in nanoimprint lithography

Yuhan Yao, He Liu, Yifei Wang, Boxiang Song, Yuanrui Li, Wei Wu, The Univ. of Southern California (United States)

Nanoimprint lithography is low-cost and mass-producible, so it is suitable for cost-sensitive applications that require a large-area patterning of nano structures. We have demonstrated the fabrication of two-dimensional high contrast gratings, in which nanoimprint lithography was used to transfer the patterns from a master mold. The master mold (with a periodic 1D grating pattern) we used was fabricated by interference lithography, which can allow us to have a good control on the pitches of the grating but not for the line width.

However, in many applications, the line widths of the grating are very crucial for an optimal device performance, so a special line width tuning method should be developed in accordance with the nanoimprint process. Moreover, reducing the roughness generated by the interference lithography can help to reduce the scattering of light and to improve the optical efficiency of the fabricated device.

For the above reasons, we developed the methods to adjust the line widths as well as to smooth the sidewalls of the gratings, which are based on the anisotropic etching of Silicon using diluted KOH. We were able to have a nice control of line widths of gratings and demonstrated smoothed master mold with different line widths. We also fabricated a special master mold (with a V-groove pattern) that was capable of generating imprinted results with various line widths by tuning the dry etching condition. More fabrication details and characterization results will be presented at the conference.

Conference 9423:
Alternative Lithographic Technologies VII

9423-32, Session 9

A nanoimprint lithography based fabrication route to obtain metallic nanoparticle of diverse/tunable shape

Nerea Alayo, Ctr. Nacional de Microelectrónica (Spain); Ana Conde, Univ. de Barcelona (Spain); Miroslavna Kovylina, Univ. de Barcelona (Spain) and Univ. of Toronto (Canada); Xavier Borrisé, Institut Català de Nanociència i Nanotecnologia (ICN2) (Spain); Joan Bausells, Ctr. Nacional de Microelectrónica (Spain); Glenn Hibbard, Univ. of Toronto (Canada); Amilcar Labarta, Xavier Batlle, Univ. de Barcelona (Spain); Francesc Perez-Murano, Ctr. Nacional de Microelectrónica (Spain)

We present a novel approach that enables the large-scale fabrication of nanoparticles with heterogeneous materials and specific shapes, such as cones and empty nanocups, hardly obtainable with methods. it the advantages of nanoimprint and stencil lithography, overcoming most of the limitations presented by common nanofabrication procedures: limited structure height, difficulties on the lift-off, blurring and dispersion of the metal.

This process is based on nanoimprint lithography and it starts by defining a SiO2 hard mask embedded in between two resist layers. The SiO2 hard mask is patterned by transferring the imprinting realized on the top resist layer, while the thickness of the bottom resist layer offers a uniform and selectable substrate-hard mask distance. In this way, the thickness of the resist where the nanoimprint lithography is performed (which has to be thin in order to achieve high resolution) is independent of the thickness of the bottom resist, which sets the maximum height of the nanoparticles. Therefore, thick metal layer can be deposited and, in consequence, high aspect ratio nanoparticles can be obtained.

The pattern defined on the SiO2 hard mask is transferred to the bottom resist, creating a cavity that influences the final shape of the nanoparticles. In particular, if direction metal evaporation is used in combination with small SiO2 hard mask, cone-shape nanoparticles are obtained. On the other hand, if the metal is deposited by un-directional sputtering, the metal covers the sides of the cavity, allowing the creation of cup-shaped nanoparticles. In both cases, the desired shape can be tuned by choosing the convenient resist thickness, SiO2 hard mask and metal deposition thickness. In particular, gold cylindrical nanocups achieved using this route have a special interest due to the onset of specific plasmonic properties, demonstrated by Finite Difference Time Domain (FDTD) simulations, that suggest their application as optical nanoresonators.

The advantages and potential applications of this method of fabrication will be discussed. The enhanced functionality that arrays of nanoparticles provide to devices and systems has been evidenced in a large number of fields, such as solar cells, growth of nanowires, plasmon resonance, enhancement of Raman spectroscopy or photochemical detection. In particular, metallic nanoparticles with defined geometry are key elements for the fabrication of highly sensitive, fast response and low cost biosensors for medical diagnosis, monitoring of diseases and the detection of environmental pollutants. When developing a practical sensor device, it is often required the massive production of nanoparticles and their accurate positioning at specific locations in pre-defined structures. While methods to synthesize nanoparticles following chemical routes are largely established, reliable processes to control their position and orientation on surfaces are not fully developed. Conversely, if the production of nanoparticles follows a top down lithography-based approach, a higher degree of order can be easily achieved but at the expenses of reducing the production yield.

9423-88, Session 9

Shape change of cured 2D and 3D nanostructures from imprint lithography

Meghali J Chopra, University of Texas at Austin, Chemical Engineering (United States); Roger T. Bonnecaze, The Univ. of Texas at Austin (United States)

Nanoimprint lithography (NIL) is a promising, low-cost, high-throughput technology for manufacturing 2D and 3D nanostructures. In NIL the template is pressed down onto a monomer resist so that it fills the mask pattern by capillary action. The resist is then cross-linked under UV radiation. Finally, the template is removed leaving a patterned resist on the substrate. There are several potential sources of error in the NIL process. Shape change due to densification is increasingly important as the critical dimensions and radii of curvature decrease for nanostructures. As the resist material polymerizes, the interaction potential between monomers shifts from van der Waal's to covalent, decreasing the average distance between them and inducing overall feature deformation. Moreover, adhesion to the template during lift off can cause the hardened resist material to fracture. Here we study the shape change and potential error introduced by polymer densification and develop a rapid forward method for predicting changes in nanoscale geometries during UV curing.

Prior research has attempted to predict the impact of resist material properties on shape deformation during curing. Hossain et al. developed isothermal elastic and viscoelastic strain models which included shrinkage effects for the curing of epoxy resins. Ye et al. analyzed the effect of exposure time on NIL resist behavior during demolding with a spring and dashpot model where the spring represents the elasticity of the resist, the dashpot represents its viscosity, and the break contact represents its plasticity. This study identified the impact of exposure time on resist moduli and feature defects. Using finite element and multiscale models, Colburn, Johnson, and Jhurani quantified the extent of elastic polymer densification as a function of the Poisson ratio, shrinkage coefficient, and modulus for different feature aspect ratios for 2D line space patterns. In this study, the shape changes of nanoscale 2D and 3D irregular geometries were analyzed using a mechanistic model.

A characteristic analysis showed that displacement is governed by the aspect ratio of the feature geometry, the Poisson's ratio, and the shrinkage coefficient. Using Abaqus, a robust finite element software, the effects of the residual layer on stress and displacement, and the impacts of densification on shapes with curves and sharp corners as well as multitiered structures were examined. The shape changes for the 3D geometries analyzed dominate in the vertical direction (Figure 1). The residual layer does not impact displacement. In addition, curved features appear to get sharper and sharp corners stay sharp.

This research demonstrates the mechanisms governing errors introduced during curing in the NIL process. Our ultimate goal is to solve the inverse template problem. That is, the design of the master template used in NIL will be tailored to account for any deformities that may a occur

during the process to achieve the desired feature layout. For NIL, this means incorporating shifts in feature design due to polymer densification, template adhesion, and anisotropic etching.

9423-33, Session 10

Electron multi-beam writer ready for use *(Invited Paper)*

Elmar Platzgummer, IMS Nanofabrication AG (Austria)

No Abstract Available

Conference 9423:
Alternative Lithographic Technologies VII

9423-34, Session 10

Performance validation of MAPPER's FLX-1200

Marco Wieland, Guido de Boer, Michel Dansberg, Remco J. A. Jager, Erwin Slot, Stijn Steenbrink, Jerry J. M. Peijster, MAPPER Lithography (Netherlands); Ludovic Lattard, Laurent Pain, CEA-LETI (France)

Mapper Lithography has introduced its first product, the FLX–1200 which is installed at CEA Leti in Grenoble (France). This is a mask less lithography system, based on massively-parallel electron-beam writing with high speed optical data transport for switching the electron beams[1]. This FLX platform is initially targeted for 1 wph performance for 10 nm technology nodes, but can also be used for less demanding imaging at 28 nm or even 40 nm. The electron source currently integrated is capable of scaling to 10 wph at the same resolution performance which will be implemented by gradually upgrading the illumination optics. The system has an optical alignment system enabling mix-and-match with optical 193 immersion systems[2] using standard NVSM marks. The tool at CEA-Leti is in-line with a Sokudo RF3 clean track.

First exposures with at CEA-Leti were done in August 2014, demonstrating the 7x7 sub-beam writing strategy[3] in a tri-layer process stack with p-CAR resist. This presentation will provide an overview of recent imaging results as well as key data on the performance of the system (i.e. electron optics, stage, metrology, data rate capabilities). We will also provide some information on the typical benefits and the application areas of the Mapper technology for customers.

The research leading to these results has been performed in the frame of the industrial collaborative consortium IMAGINE driven by CEA-Leti

[1] E.A. Hakkennes et al. "Demonstration of Real Time pattern correction for high throughput maskless lithography", Proc. SPIE 7970, Alternative Lithographic Technologies III, 79701A

[2] N. Vergeer et al. "MAPPER Alignment sensor evaluation on Process Wafers", Proc. SPIE 8680, Alternative Lithographic Technologies V, 86801E

[3] M.J. Wieland et al, "Throughput enhancement technique for MAPPER maskless lithography", Proc. SPIE 7637, Alternative Lithographic Technologies II, 76371Z

9423-35, Session 10

Thermal effect induced wafer deformation in high-energy e-beam lithography

Pei-Shiang Chen, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

The incident surface power density in Massive Electron-beam Lithography (MEBL) during exposure is ~105 W/cm2, which is much higher than ~8 W/cm2 ArF scanners and 2.4 W/cm2 EUV. In addition, the wafer is exposed in the vacuum environment, which makes dissipating energy even harder. This thermal effect causes mechanical distortion of the wafer during exposure. It has a direct influence on pattern placement error and image blur.

In this paper, the thermo mechanical distortions caused by wafer heating for high energy MEBL have been simulated with finite element (FE) models, in which local transient thermal effect affected by local pattern density, the resist thickness and its sensitivity variation are considered. The global thermal effect with structural interaction between the wafer and the wafer chuck such as friction force and different material thermal conductivity is also simulated. Furthermore the comparison of the thermal effect of different lithography systems such as e-beam mask writer, EUV scanner, and conventional optical scanner are discussed as well.

9423-36, Session 10

Comparison between e-beam direct write and immersion lithography for 20nm node

Pieter Brandt, MAPPER Lithography (Netherlands); Charu Sardana, Dale E. Ibbotson, Altera Corp. (United States); Marco Wieland, MAPPER Lithography (Netherlands); Aurélien Fay, CEA-LETI (France)

Today's soaring complexity in pushing the limits of 193nm immersion ('193i') lithography drives the development of other technologies. One of these alternatives is massively parallel electron beam direct write, (MP-)EBDW, a promising candidate in which future resolution needs can be fulfilled at competitive cost. MAPPER Lithography's MP-EBDW platform, MATRIX (FLX1200), has currently entered an advanced stage of development.

In this study EBDW process window simulations were performed on Altera designs of the 20nm node (minimum half-pitch 32nm), using similar methods and Proximity Effect Corrections as in previous work [1]. For selected layout clips, a direct comparison is made with 193i simulation results. The latter comprises a Litho-Etch-Litho-Etch (LELE) process at 80nm depth of focus (DOF), which entered the production stage in 2013.

The EBDW counterpart of DOF is the variation of the spot size in resist, which is +/-2nm with respect to the nominal value 28nm. This spot size includes contributions from the tool such as the size of the electron beam and contributions from the resist such as acid diffusion and electron scattering. In this work the process window is quantified by means of the dose latitude: the size of the process window at respectively the specified DOF and spot size variation range.

Both Local Interconnect (figure 1) and Via layers (figure 2) are considered, the former at CD tolerance of +/-10%, the latter at +/-20%. The EBDW dose latitude was found to exceed that of the LELE process by 70%. In addition, the EBDW dose latitude may be enhanced further in a trade-off with throughput.

As the electron beam total spot size is of the order of the CD, a single exposure per layer suffices and interference between neighboring features is low. This results for the Local Interconnect test case in a 'clean' process window in which the curves for the various CD sites roughly overlap (figure 1a), in as opposed to the 193i case in which they differ significantly (figure 1b).

The lithography performance of EBDW is mainly limited by the edge placement error (EPE) of line ends (figure 3). The EBDW capability for Altera designs was validated by exposures on the MAPPER pre-alpha tool installed at CEA-Leti [2] (figure 4).

The research leading to these results has been performed in the frame of the industrial collaborative consortium IMAGINE driven by CEA-Leti.

9423-37, Session 10

Alternative stitching method for massively parallel e-beam lithography

Pieter Brandt, MAPPER Lithography (Netherlands); Céline Tranquillin, Aselta Nanographics (France); Marco Wieland, MAPPER Lithography (Netherlands); Sébastien Bayle, Matthieu Milléquant, Guillaume Renault, Aselta Nanographics (France)

Today's soaring complexity in pushing the limits of 193nm immersion lithography drives the development of other technologies. One of these alternatives is massively parallel electron beam direct write, (MP-)EBDW, a promising candidate in which future resolution needs can be fulfilled at competitive cost.

MAPPER Lithography's MATRIX (FLX1200) platform has currently entered an advanced stage of development. This tool will operate using more than 13,000 beams, each one writing a stripe 2.2?m wide. 0.2?m overlap from stripe to stripe [1].

In order to mitigate the effect of beam to beam position error on CD, stitching strategies from one beam (stripe) to another can be deployed in the overlapping regions. The strategies of smart boundaries (SB) and soft edges (SE) were discussed in [2]. In addition to SB and SE, a third strategy at enhanced exposure latitude (EL) is now presented.

By applying a negative CD bias, throughput can be exchanged for Exposure Latitude [3]. In the overlapping region, without cost in throughput, the two passing neighboring beams can deposit a total dose up to 2x higher than the nominal dose (Figure 1). As a result the EL can be increased in the stitching region. The effect of the better EL is twofold: The robustness against beam to beam position errors is improved as well as the performance with respect to other internal (e.g. dose control) and external (e.g. electron shot noise) CDu sources.

As an initial test case 32nm half-pitch unbiased dense lines and spaces are considered a nominal CDu of 3.2 nm. For this case it was found that at a sinusoidal dose profile, reduction of non-stitching related CDu components can completely compensate the residual CDu contribution from stitching error (Figure 2). Hence, with the presented method the imaging performance in the stitching region is at the same level as outside the stitching region. As a result the requirement on beam to beam position errors is determined by the overlay requirement, and no longer by the CDu requirement.

In the paper we will analyze the performance of this method applied to realistic 16nm node Metal 1 patterns. For this it is required to combine the proximity effect correction and the calculation of the stitching strategy in one dataprep solution.

The research leading to these results has been performed in the frame of the industrial collaborative consortium IMAGINE driven by CEA-Leti.

9423-38, Session 10

Development of ballistic hot electron emitter and its applications to parallel processing: active-matrix massive direct-write lithography in vacuum and thin films deposition in solutions

Nobuyoshi Koshida, Tokyo Univ. of Agriculture and Technology (Japan); Akira Kojima, Naokatsu Ikegami, Tohoku Univ. (Japan); Ryutaro Suda, Mamiko Yagi, Junichi Shirakashi, Tokyo Univ of Agriculture and Technology (Japan); Takashi Yoshida, Hiroshi Miyaguchi, Masanori Muroyama, Hitoshi Nishino, Shinya Yoshida, Tohoku Univ. (Japan); Masanori Sugata, Crestec Corp. (Japan); Kentaro Totsu, Masayoshi Esashi, Tohoku Univ. (Japan)

Nanocrystalline Si (nc-Si) diode emits uniformly energetic hot electrons with a small angular dispersion [1]. The nc-Si emitter is composed of a thin metal surface electrode, an nc-Si dot layer, an n+-Si substrate, and an ohmic back contact. The emission mechanism is based on multiple-tunneling cascade through quantum-sized nc-Si dots interconnected with tunnel oxides. Being a surface-emitting cold cathode with relatively low operating voltages, insensitivity to ambient pressure, quick dynamic response, and compatibility with planar fabrication process, the nc-Si emitter is useful either as an excitation source in vacuum or an active electrode supplying highly reducing electrons. Here we show recent progress in topics of applications to parallel patterning processes. As previously reported [2,3], the characteristics of the nc-Si emitter are suitable for an exposure source of parallel electron beam lithography in vacuum. The nc-Si emitter array was fabricated on the SOI substrate by sequential planar process. Arrays of the nc-Si emitter with a size of 10?10 ?m2 in active area were prepared by selective patterning, electrochemical anodization, and subsequent oxidation. In addition to the planar-type emitter, Pierce-type device with a dimple structure was also arrayed [4]. The back contact of each electron-emitter was interconnected with Through-Silicon-Via (TSV) plugs. The relatively low operating voltage makes it possible to drive the emitter array in CMOS active-matrix mode. The unit was designed to be able to simultaneously drive all the pixels of the nc-Si electron emitter array in accordance with pattern data stored in a built-in memory. The schematic cross-sectional structures of two-type emitter arrays are shown in Figs. 1(a) and 1(b). Combining the integrated emitter array with an electron optics for collimation, focusing, and acceleration, the system development is underway toward a mask-less high throughput nanolithography (Fig. 2). The nc-Si ballistic emitter operates even in solutions as a supplier of highly reducing electrons into chemical species. In metal salt solutions this enables to deposit thin metal films without using any counter electrodes. When driven in SiCl4 [5], GeCl4, and their mixture solutions, injected energetic electrons directly reduce Si4+ and Ge4+ ions, and then lead to the nucleation of the growth of thin amorphous Si, Ge, and SiGe films at the emitting area with neither contaminations nor byproducts. When the nc-Si device with patterned emission windows is used, thin films array of Si can be fabricated in parallel, as shown in Figs. 3(a) and 3(b). These effects provide means as alternative approach toward clean, low-temperature, and power-effective deposition of thin films of metals and group IV semiconductors.

References

1. N. Koshida et al, Current Opinion in Solid State and Mater. Sci. 15, 183 (2011).

2. A. Kojima et al, Proc. SPIE Symp. on Advanced Lithography, 9049-43, 2014.

3. N. Ikegami et al, J. Vac. Sci. & Tech. B 31, 06F703 (2013).

4. H. Nishino et al, Proc. 27th IEEE Int. Conf. on MEMS (San Francisco, USA., 2014), pp. 467-470.

5. T. Ohta et al, Appl. Phys. Lett. 102, 022107 (2013).

9423-39, Session 11

Self-aligned line-space pattern customization with directed self-assembly grapho-epitaxy at 24nm pitch *(Invited Paper)*

Hsinyu Tsai, Hiroyuki Miyazoe, IBM Thomas J. Watson Research Ctr. (United States); Joy Y. Cheng, IBM Research - Almaden (United States); Markus Brink, Simon Dawes, David Klaus, James Bucchignano, IBM Thomas J. Watson Research Ctr. (United States); Daniel P. Sanders, IBM Research - Almaden (United States); Eric A. Joseph, IBM Thomas J. Watson Research Ctr. (United States); Matthew E. Colburn, IBM Corp. (United States); Michael A. Guillorn, IBM Thomas J. Watson Research Ctr. (United States)

Fully-depleted multi-gate FETs composed of discrete Si fins, such as FinFETs, are likely to play a role in silicon device scaling because of their improved electrostatics and elimination of random dopant fluctuations [1]. Fin pitch scaling provides capacitance improvements to FinFET devices, but the customization of such fin patterns becomes challenging due to resolution and alignment limitations in the fin customization process. Because current patterning schemes are based on a “sea of fins plus cut” technique, overlay accuracy limits edge placement of cut mask patterns with respect to the more grating-like patterns and ultimately limits pitch scaling.

Grapho-epitaxy directed self-assembly (DSA) of lamellae forming block copolymers (BCPs) generates groups of lines that are aligned to lithographically defined template patterns. By applying a tone inversion process to turn template regions into spaces, group of fins with self-aligned cuts along the fin direction can be formed [2]. Electrical characterization confirms that the “cut first” fins at 28nm pitch yield FinFET devices with good electrostatics and reasonable performance [2]. Such self-aligned customization techniques will become even more critical as we continue to scale beyond 28nm pitch.

In this paper, we explore further scaling of the Tone-Inverted Grapho-Epitaxy (TIGER) technique with 24nm pitch PS-b-PMMA polymers. We use e-beam patterned HSQ templates to study three key aspects for DSA at 24nm pitch: material, self-aligned customization, and etch.

Continued scaling with PS-b-PMMA becomes more challenging as the polymer chain length approaches the lower limit for phase separation. Bridging is a major type of defects and can be alleviated by material engineering. Figure 1 shows two types of 24nm pitch PS-b-PMMA polymers after grapho-epitaxy and etch transfer into a 10nm silicon nitride hard mask. Material A shows high density of bridging defects that were hard to observe after DSA, but became very obvious after etch transfer.

Two-dimensional pattern customization is demonstrated with 24nm pitch PS-PMMA, confirming the scalability of this approach. Figure 2 shows that PMMA domains are terminated on the HSQ sidewalls perpendicular to the major direction of the template flow, effectively cutting the PMMA lines. The tone inversion process is successfully exercised at 24nm pitch, although further etch tuning is required to improve LER. DSA lines are etch-transferred into 30nm of silicon nitride hard mask, as shown in Figure 3.

In summary, TIGER offers self-aligned customization and therefore provides a path to further fin pitch scaling without tighter cut mask overlay control.

[1] H. Kawasaki, et al, Proc. IEDM (2008).

[2] H. Tsai, et al., ACS Nano (2014).

9423-40, Session 11

Impact of BCP asymmetry on DSA patterning performance

Lance D. Williamson, The Univ. of Chicago (United States) and IMEC (Belgium); JiHoon Kim, Yi Cao, Guanyang Lin, AZ Electronic Materials USA Corp. (United States); Roel Gronheid, IMEC (Belgium); Paul F. Nealey, The Univ. of Chicago (United States)

Directed self-assembly (DSA) of block copolymers (BCP) via chemo-epitaxy is a potential lithographic solution to patterns of dense features. The LiNe (Liu-Nealey) flow for fabricating the chemical pattern is illustrated in Figure 1. The volume fraction of each block in the block copolymer determines the morphology. On a finer scale, small changes in the volume fraction of a lamellae-forming BCP have been shown to change the connectivity of unguided domains. When an asymmetric lamellae-forming BCP is assembled on chemical patterns generated with the LiNe flow, the patterning performance and defect modes change depending on whether the majority or minority volume fraction phase is guided by the chemical pattern.

Asymmetric BCP formulations were generated by blending homopolymer with a symmetric BCP. The patterning performance of the BCP formulations was assessed for different pattern pitches, guide stripe widths, backfill materials and annealing times. Optical defect inspection and SEM review are used to track the majority defect mode for each formulation. Formulation-dependent trends in defect modes show the importance of optimizing the BCP formulation in order to minimize the defectivity.

9423-41, Session 11

Directed self-assembly lithography using coordinated line epitaxy (COOL) process

Yuriko Seino, Yusuke Kasahara, Ken Miyagi, Shinya Minegishi, Hironobu Sato, Katsutoshi Kobayashi, Hideki Kanai, Katsuyoshi Kodera, Naoko Kihara, Toshikatsu Tobana, Tomoharu Fujiwara, Noriyuki Hirayanagi, Yoshiaki Kawamonzen, Tsukasa Azuma, EUVL Infrastructure Development Ctr., Inc. (Japan)

In order to carry out process verification of directed self-assembly (DSA) lithography on 300 mm wafer for semiconductor device manufacturing, we developed a novel simple sub-15 nm line and space (L/S) patterning process and evaluated process performances of the DSA lithography and pattern transfer. Several sub-15nm L/S patterning processes using polystyrene-block-poly(methyl methacrylate) (PS-b-PMMA) lamellar block copolymer (BCP) have been reported such as lift-off flow [1], LiNe flow [2,3] and SMARTTM flow [4]. The novel simple sub-15 nm L/S patterning process, "coordinated line epitaxy (COOL) process", using grapho- and chemo-hybrid epitaxy requires neither special pinning guide materials to control surface free energy on guide line patterns nor resist strip process after guide line patterns fabrication. We demonstrated the process performances of the DSA lithography and pattern transfer such as process windows, critical dimension uniformity (CDU), pattern roughness (LER and LWR) and defects (3-dimensional BCP internal defects) on 300mm wafer.

Figure 1 shows sub-15 nm L/S patterns using the COOL process. In the DSA lithography process, firstly 45 nm L/S resist patterns were formed using ArF immersion exposure on a stacked substrate consisting of SOG (Spin-on-Glass), SOC (Spin-on-Carbon) and hard mask layer. Secondly, pining guide lines with PMMA affinity were formed using resist trimming and SOG partial etching. Thirdly, the SOG layer was processed by neutral layer grafting. Finally, sub-15 nm L/S patterns were formed after micro-phase separation by BCP anneal and subsequent PMMA dry development. In the pattern transfer process, the sub-15 nm L/S patterns were successfully transferred into SOG/SOC stacked substrates. We found that the pattern roughness after the SOC etching has drastically been improved compared to that after the ArF immersion exposure.

9423-42, Session 11

Contact hole shrink and multiplication by directed self-assembly of block copolymers: from materials to integration

Raluca Tiron, Ahmed Gharbi, MINATEC (France); Celine Lapeyre, Patricia Pimenta-Barros, Sandra Bos, Antoine Fouquet, Jerome Hazart, Sebastien Barnola, Sebastien Berard Bergery, Maxime Argoud, CEA-LETI (France); Shayma Bouanani, Cedric Monget, Vincent Farys, STMicroelectronics (France); Xavier Chevalier, Christophe Navarro, Celia Nicolet, Arkema S.A. (France); Guillaume Fleury, Georges Hadziioannou, Lab. de Chimie des Polymères Organiques (France)

Density multiplication and contact shrinkage of patterned templates by directed self-assembly (DSA) of block copolymers (BCP) stands out as a promising alternative to overcome the limitations of conventional lithography [1, 2]. The main goal of this paper is to investigate the potential of DSA to address contact and via levels patterning with high resolution by performing either CD shrink or contact multiplication. Different DSA processes are benchmarked based on several success criteria such as: CD control, defectivity (missing or multiple holes) as well as placement control. More specifically, the methodology employed to measure DSA contact overlay and the impact of process parameters on placement error control is detailed.

Using the 300mm pilot line available in LETI [3] and Arkema's materials [4], our approach is based on the graphoepitaxy of PS-b-PMMA block copolymers. Our integration scheme, depicted in figure 1, is based on BCP auto-organization inside organic hard mask guiding patterns obtained using 193i nm lithography. The process is monitored at different step: the generation of guiding patterns, the directed self-assembly of block copolymers and PMMA removal, and finally the transfer of PS patterns into the metallic under layer by plasma etching.

Furthermore, several process flows are investigated, either by tuning different material related parameters such as the block copolymer intrinsic period or the interaction with the substrate (sidewall and bottom-side affinity). The final lithographic performances are finely optimized as a function of the self-assembly process parameters such as the film thickness and bake (temperature and time).

By corroborating defectivity measurements with CDU and placement error measurements, process windows are identified. As an example, results obtained with a block copolymer of intrinsic period L0 = 35 nm are depicted

in figure 2. The CD measured post DSA (in blue on the graph) and Hole Open Yield (HOY in red) are reported as a function of the CD of guiding patterns. Thus, for CDguiding < 45nm (region 1) there are missing contacts; for CDguiding > 55nm (region 3) contacts are distorted or multiplied and CH shrink process window is associated with region 2 on the graph. CDU and placement control are finally measured in this regime. In this paper, the implementation of this methodology has been employed for the integrated flow process developed for both contact shrink and contact doubling.

Finally, DSA performances as a function of guiding patterns density are investigated. Thus, for the best integration approach, defect-free isolated and dense patterns for both contact shrink and multiplication (doubling and more) has been achieved on the same processed wafer.

These results show that contact hole shrink and multiplication approach using DSA is well compatible with the conventional integration used for CMOS technology.

References:

1. C.Bencher et al., Proc. of SPIE 2012, 8323-22

2. H.Yi et al., Adv. Mater, 2012, 24, 3107-3114

3. R. Tiron et al, Proc. of SPIE 2012, 8323-23

4. X. Chevalier &al., J. Micro/Nanolith. MEMS MOEMS 12(3), 031102 (2013).

9423-43, Session 11

Cross-sectional imaging of directed self-assembly block copolymers

Kye Okabe, He Yi, Maryann Tung, Richard C. Tiberio, H. S. P. Wong, Stanford Univ. (United States)

Block Copolymer Directed Self Assembly (DSA) has gained great interest in recent years as a potential next-generation lithography technique for a wide variety of applications [1-10]. For the cylinder-forming diblock copolymers in particular, much work has been put into understanding the statistical distribution of hole diameter and pitch as well as the dependence of defects on the guiding template dimensions and layout [11, 12]. However, most studies thus far have been based on observations from top view images obtained from scanning electron microscopes (SEM), resulting in information limited by its spatial resolution and viewing angle, and without information about the 3D shapes inside the holes.

With applications at ultra-scaled dimensions, such as contact holes for the upcoming 10 nm technology node [13], it has become increasingly important to capture the detailed nanostructure in order to study the relationships between the templates, holes, and especially defects. The practical resolution capability of the SEM often prohibits one from clearly imaging features with few nm lengths due to the relatively large sampling volume of incoming electrons, and is becoming more and more unsuitable for such tasks as scaling continues. Moreover, judging the defectively of DSA holes based solely on top view images could lead to misconceptions due to hidden defects under the surface. For these reasons, a cross-sectional image with resolution beyond the capability of the SEM would be of significant value for enriching our understanding.

In this study, we address these two challenges by demonstrating a technique for obtaining cross-sectional transmission electron microscope (TEM) images for single-hole template patterns (Figure 1). A 70:30 PS-b-PMMA diblock copolymer dissolved in propylene glycol monomethyl ether acetate (PGMEA) was self-assembled in etched silicon templates. The PMMA was selectively dissolved by immersing the sample in glacial acetic acid. TEM sample preparation was performed on a focused ion beam (FIB)/SEM dual beam system. To prevent the cylinder cavity structures from deforming during sample preparation due to physical or thermal stimulation caused by the Ga ion beams or high flux e-beams, a thin protective Pt layer was deposited prior to ion milling. This layer was formed with in-situ e-beam assisted chemical vapor deposition (CVD), followed by the use of ion beam assisted CVD to deposit 2 ?m of Pt. The benefits of e-beam and ion-beam assisted CVD over other methods such as evaporation and sputtering are that it can be performed at room temperature (no thermal damage) and that the cylinder can be filled densely due to the precursor gas being decomposed molecule by molecule. The thin Pt layer by e-beam assisted deposition with slower deposition rate was performed first because ion beam assisted deposition can cause damage to the surface of the underlying layer due to Ga ions which reach the sample surface.

From images obtained, we find the template depths, template sidewall angles, and hole depths to be tightly distributed. The average hole extends 61.3% into the depth of the average template. Though there is noticeable variation in the hole curvatures, the general shape agrees qualitatively with previously obtained simulation results [14]. This technique can be expanded to a wide range of template patterns and can help us understand the 3D nature of a variety of structures with further experimentation.

9423-44, Session 12

High-speed e-beam defect inspection: enabling next-generation patterned defect inspection technology for high-volume manufacturing *(Invited Paper)*

Matt Malloy, SEMATECH Inc. (United States); Brad Thiel, SUNY College of Nanoscale Science and Engineering (United States); Benjamin D. Bunday, Michael J. Lercel, SEMATECH Inc. (United States); Kathy Quoi, Maseeh Mukhtar, SUNY College of Nanoscale Science and Engineering (United States); Stefan Wurm, Kevin D. Cummings, SEMATECH Inc. (United States)

SEMATECH's Metrology program aims to identify and enable disruptive technologies to meet the ever-increasing demands of semiconductor high volume manufacturing (HVM) metrology. As such, SEMATECH initiated a program in 2012 focused on high-speed e-beam defect inspection as a complement, and eventual successor, to bright field optical patterned defect inspection. The primary goal is to enable a new technology to overcome the key gaps that are limiting modern day inspection in the fab; primarily, throughput and sensitivity to detect ultra-small critical defects. The program specifically targets revolutionary technologies, such as massively parallel e-beam inspection, as opposed to incremental improvements to existing e-beam and optical inspection platforms. Wafer inspection is the primary target, but attention is also being paid to next generation mask inspection. During the first phase of the multi-year program multiple technologies were reviewed, a down-selection was made to the top three candidates, and evaluations began on proof of concept systems. As of late 2014 the program has begun to move into the core technology maturation phase in order to enable eventual commercialization of an HVM system.

This paper lays out the performance requirements and justification for high-throughput e-beam inspection and explains both the technical and business requirements for such a technology. Performance data from early proof of concept systems will be shown along with roadmaps to achieving HVM performance. A modeling and simulation effort is also being implemented in order to support and guide hardware development, interpret experimental assessment data, and to enable more efficient exploration of application and material sets. SEMATECH's vision for moving from early-stage development to commercialization will be shown, including plans for alpha, beta, and HVM development with industry leading technology providers. A brief discussion is also included on some recent advancements in the miniaturization of key electron-beam system components that may enable novel inspection strategies for far future technology nodes. Furthermore, we provide a short introduction to other key metrology capability gaps foreseen by SEMATECH which are garnering future attention through new, targeted projects.

9423-45, Session 12

Fabrication of NIL templates and diffractive optical elements using the new Vistec SB4050 VSB e-beam writer

Mathias Irmscher, Jörg Butschke, Stephan Martens, Holger

Sailer, Institut für Mikroelektronik Stuttgart (Germany); Bernd Schnabel, Vistec Electron Beam GmbH (Germany); Corinna Köpernik, Institut für Mikroelektronik Stuttgart (Germany)

Nanoimprint Lithography (NIL) is a cost-effective way to generate nano-structures in a high volume manufacturing for versatile applications. Typical areas are photonics, energy harvesting, optics, bio sciences or nano-electronics. Complex optical functionalities can be realized by Diffractive Optical Elements (DOE) at reasonable costs. Both, NIL templates and DOEs need similar structuring technologies.

According to the particular application the requirements for templates or for DOEs can be manifold. At first they can be different in size, weight or shape. Typical materials for the fabrication of templates are silicon, quartz, nickel or even steel while DOEs are made of transparent material as quartz.

Frequently used standard form factors are 150mm, 200mm or 300mm wafers and 6inch or 9inch blanks.

Furthermore, the application determines the patterning specifications such as resolution, aspect ratio, feature slope and placement accuracy including all the tolerances. Single-level, multi-level or 3D patterning, regular or arbitrary designs are additional characteristics of template and DOE structuring.

E-beam, laser, stepper, and interference lithography are well established solutions for NIL template and DOE exposure. The appropriate lithography solution will be selected according to the design requirements and considering cost-issues.

The e-beam lithography has the highest potential in terms of resolution and flexibility but is the most expensive choice.

The new Vistec SB4050 VSB e-beam writer offers some remarkable features which are beneficial for the state-of-the-art NIL template and DOE making. The writer has a new air bearing stage for writing large and heavy substrates with high placement accuracy. The stage allows the exposure of a variety of substrates with a diameter up to 450mm and a thickness up to 20mm. For multi-level patterning a precisely working alignment system is available. The column operates at 50kV with a current density of 20A/cm2. The address grid of the stage is 0.6nm.

We evaluated the Vistec SB4050 regarding its capability for NIL template and DOE making. At first we figured out the placement accuracy for different substrates, important for multi-level or mix & match solutions. On 9inch quartz blank we achieved 9nm/8nm (3sigma). The second level alignment accuracy was measured on a 9035 blank, as well. The result was 10nm/13nm (3sigma) across the entire plate.

Resolution is driven by both, the tool and the resist. In order to achieve reasonable exposure times we used Chemically Amplified Resists for the evaluation, only. For dense gratings we could prove 30nm half pitch at a film thickness of 60nm. A 3D structuring capability enables the fabrication of blazed gratings or micro lenses. We realized 3D features by applying GenISys' Layout Beamer calibrated for an appropriate negative tone resist.

Finally, we will demonstrate the patterning capability of the SB4050 by some NIL template and DOE examples.

9423-46, Session 12

Integration of e-beam direct write in BEOL processes of 28nm SRAM technology using mix and match

Christoph K. Hohle, Fraunhofer-Institut für Photonische Mikrosysteme (Germany); Kang-Hoon Choi, Manuela S. Gutsch, Norbert Hanisch, Fraunhofer-Ctr. Nanoelektronische Technologien (Germany); Robert Seidel, GLOBALFOUNDRIES Dresden Module One LLC & Co. KG (Germany); Katja Steidel, Xaver Thrun, Fraunhofer-Ctr. Nanoelektronische Technologien (Germany); Thomas Werner, GLOBALFOUNDRIES Dresden Module One LLC & Co. KG (Germany)

Electron beam direct write lithography (EBDW) potentially offers advantages for low-volume semiconductor manufacturing, rapid prototyping or design verification due to its high flexibility without the need of costly masks.

However, the integration of this advanced patterning technology into complex CMOS manufacturing processes remains challenging. The low throughput of today's single e-Beam tools limits high volume manufacturing applications and maturity of parallel (multi) beam systems is still insufficient. Additional concerns like transistor or material damage of underlying layers during exposure at high electron density or acceleration voltage have to be addressed for advanced technology nodes. Last year we successfully proved that potential degradation effects of high-k materials or ULK shrink can be neglected and excluded by demonstrating the integrated electrical results of 28nm node transistor and BEOL performance following 50kV electron beam dry exposure.

This time we will report on the integration of EBDW in the CMOS manufacturing processes of advanced integrated circuits at the 28nm SRAM node of GLOBALFOUNDRIES Dresden. We will demonstrate e-Beam patterning results of BEOL metal and via layers with a dual damascene integration scheme using a 50kV VISTEC SB3050DW variable shaped electron beam direct writer at Fraunhofer IPMS-CNT.

Since the original layout was not designed for e-Beam exposure, significant efforts were spent on data preparation. INSCALE® from ASELTA Nanographics has been used for advanced DataPrep and Proximity Effect Correction (PEC). Results will be shown on shot count reduction and optimized e-Beam exposure time.

Integrated 300mm wafers with a 28nm back-end of line (BEOL) stack from GLOBALFOUNDRIES, Dresden, were used for the experiments. For the patterning of the metal layer a mix & match concept based on the sequence litho - etch - litho – etch (LELE) was developed and evaluated. Therefore several exposure fields were blanked out during the optical exposure. After the first hard mask open step these fields have been exposed by EBDW and consecutively etched into the same hard mask. The optical lithography requires a 3-layer scheme of anti-reflective coating, planarization layer and hard mask which enables a lateral shrink during the etch step. In contrast to that the e-beam lithography allows a direct hard mask patterning with smaller structures. We will give an update on our integration work including electrical results.

9423-47, Session 12

Ready for multi-beam exposure at 5kV on MAPPER tool: Lithographic and process integration performances of advanced resists/stack

Ndeye A. Thiam, Patricia Pimenta-Barros, Isabelle Servin, Marie-Line Pourteau, Armel-Petit Mebiene, Julien Jussot, Jonathan Pradelles, CEA-LETI (France); Marie-Laure Cordini, STMicroelectronics (France); Philippe Essomba, Ludovic Lattard, CEA-LETI (France); Pieter Brandt, Marco Wieland, MAPPER Lithography (Netherlands)

Maskless electron beam lithography is an attractive solution to address sub-40 nm technology nodes with high throughput and manufacturing costs reduction . One of the key challenges is to meet the process specifications for the machine developed by MAPPER Lithography and installed at CEA-Leti.

The process has to meet specific requirements such as resolution, throughput target of 20-40μC/cm2, roughness (ITRS target LWR<2.2nm for 26nmhp), resist sensitivity to e-beam shot noise , stack sheet resistance (Rsheet < 105 ?) which demands a charge dissipation layer, etch transfer into underlayers and outgassing mitigation to prevent contamination of the electron optics .

The aim of this study was to identify and optimize the process stack,

including e beam resists and related layers (SOC/SiARC, top-coat and conductive layer), for all of the above-mentioned requirements.

In this paper resolution, sensitivity, process window, LWR, L-CDU, contrast, stability have been evaluated on 2 exposure tools: the MAPPER multi-beam tool at 5kV (figure 1a) and a VISTEC shaped-beam tool at 50kV.

After recipe optimization, etch transfer was demonstrated to preserve pattern fidelity (bias), roughness and CD uniformity (figure 1b).

We also discuss the introduction of a conductive layer in the CMOS process flow. Preliminary results show standard metallic layer as TiN to be compliant to the sheet resistance specification.

Resist outgassing leading to carbon contamination of the electron optics is particularly critical for the lifetime and uptime of the multi e-beams exposure tools that use several thousands of parallel electron beams. Reducing the contamination process at the root is thus crucial. A specifically designed top-coat layer has been evaluated and shows a 43% reduction of the outgassing rate without jeopardizing imaging performance and throughput. The resist alone as well as integrated on the trilayer stack has been evaluated for outgassing performances.

This paper will report recent progress to achieve robust patterning process for multi-beam application.

The research leading to these results has been performed in the frame of the industrial collaborative consortium IMAGINE driven by CEA-Leti.

9423-48, Session 12

A contour-based kernel modeling and verification approach to electron-beam lithography

Jan-Wen You, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

In E-beam lithography, the double or multiple Gaussian kernels to describe the electron scattering behavior are discussed extensively while critical dimensions (CDs) are larger than the electron beam blur size. However in e-beam direct write for wafer, CD is similar with beam blur size, the kernel need to be re-examined.

This paper presents a contour-based kernel modeling and verification approach for electron beam lithography. In edge contour extraction of CD-SEM images, the hole array with duty ratio split is used as the test vehicle in this Gaussian kernel modeling study. A 2-step optimization sequence is proposed to improve the fitting efficiency and robustness. In the first step, roundness is the primary and the most effective index at the corner region which is sensitive to beam blur changes. To mitigate the influence of through-pitch proximity effect caused by the electron forward scattering and backscattering, the more accurate cost index, hole area or edge placement error (EPE), is applied in the subsequent optimization step with constrained beam blur size extracted by the previous step. The optimum kernel parameters can be obtained by the lowest cost deviation of the simulation contour and the CD-SEM extracted edge contour after optimization iterations. For early study of the proximity impact on future EBDW systems, the experiment is performed on the EBM8000 mask writer. Not only the regular 2D array but also the real circuit patterns are evaluated in the final model accuracy verification.

9423-49, Session 13

Verification of directed self-assembly (DSA) guide patterns through machine learning

Seong-Bo Shim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of) and KAIST (Korea, Republic of); Sibo Cai, Samsung Electronics (Korea, Republic of); Seung-Hune Yang, Jungdal Choi, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Youngsoo Shin, KAIST (Korea, Republic of)

A device of sub 10-nm node requires contacts and vias smaller than 40nm, which is beyond the resolution limit of traditional lithography. In directed self-assembly (DSA), a guide pattern is formed through conventional lithography; it is then filled with block copolymers (BCPs), in which two polymers are self-aligned after being heated; one of the polymers is etched away leaving contact (or via) holes. Verifying whether correct contacts can be obtained from a given guide pattern requires a DSA simulation, which however takes impractical amount of time. Note that a guide pattern, in turn, is obtained from mask image through a lithography simulation.

We prepare a few test contacts, perform DSA simulations on the corresponding guide patterns, and classify them into good and bad ones; the guide patterns are then generalized through machine learning; during actual verification, each guide pattern in the layout is checked through simple look-up instead of lengthy simulations.

Test contacts are grouped depending on the number of contacts; each group is further classified by the location of contacts. Some neighbor contacts are randomly placed around the main test contacts.

An ideal guide pattern is submitted to OPC and lithography simulations (while lithography settings are varied), which yield a set of real guide patterns or guide pattern process variation band (PVB). DSA simulations are performed on the real guide patterns that correspond to the inner and outer boundary of PVB; two contact images, called contact PVB, are obtained. We finally examine the size and position of contact PVB with original contact layout as a reference; a guide pattern is labeled DSA hotspot if differences exceed the quantities provided by fab.

To generalize the guide pattern that have been tested, three types of parameters are chosen for model learning process. These include edge placement error (EPE) between ideal and real guide patterns, side wall angle, and distance between adjacent contacts. EPE and side wall angle are measured at three sets of points, namely the points along arc, the points at peak, and the points at valley; in each set, a root mean square value is calculated and used as a single representative value. EPE in turn has two values, one between ideal guide pattern and outer boundary of PVB, and the other between ideal guide pattern and inner boundary of PVB. In total, 10 parameters (6 EPEs, 3 side wall angles, and 1 contact distance) are submitted to model learning process, which is based on support vector machine (SVM); it then yields a binary model that determines whether a given guide pattern is DSA hotspot or not. During actual verification, the parameters of each guide pattern are extracted and assessed against those trained through model learning; we evaluate the model in terms of prediction accuracy and runtime.

9423-50, Session 13

Experimental study of sub-DSA resolution assist features (SDRAF)

He Yi, Stanford Univ. (United States); Joost P. Bekaert, Roel Gronheid, Geert Vandenberghe, IMEC (Belgium); Kathleen Nafus, Tokyo Electron America, Inc. (United States); H. S. P. Wong, Stanford Univ. (United States)

As the scaling of semiconductor devices continues, traditional optical lithography is counting on EUV lithography or multiple exposures to print the increasingly smaller and denser patterns. Directed Self-Assembly (DSA) has become a promising candidate as a complementary lithography technology as it could generate sub-20 nm features on pitches that are denser than any lithography can achieve in a single patterning step, with a much lower cost. Among all the DSA morphologies, the cylindrical DSA structures have attracted significant attention, due to its potential for patterning contacts. To generate the aperiodic contact patterns in a IC layout, physical guiding templates are adopted. By varying the size and shape of guiding templates, single and multi-hole DSA patterns could be generated and positioned in a well-controlled manner. Previous works have demonstrated the flexible control of DSA patterns using small guiding templates; contact hole patterning was also demonstrated for sub-10

nm IC circuits. In previous studies, many researchers have also reported the influence of template density on DSA patterns. Specifically, when the template density becomes low, the reflow of the polymers will cause templates to be overfilled, leading to defects formed inside the template. As the contact density of a full-chip layout is never uniform and there are always isolated contacts, it becomes essential to come up with a solution to reduce the overfilled conditions for the low-density contacts. In this paper, we demonstrate an effective solution to mitigate overfill conditions using sub-DSA resolution Assist Features (SDRAF) through experiments.

Sub-DSA resolution Assist Features (SDRAF) are small openings in the template layer that are designed to artificially create a more uniform density, leading to a reduced number of overfilled templates and therefore improved DSA performance. Unlike the Sub-Resolution Assist Features (SRAF) in optical lithography which are not printed on the wafer, SDRAFs need to be printed to be functional. There are two advantages of SDRAF: 1. Allowing these small features to be printed can increase the process window of lithography. 2. When placing these SDRAFs around the low-density guiding templates, the SDRAF could become the polymer reservoirs to store the extra polymers, therefore preventing the low-density guiding templates of becoming overfilled, thereby improving the quality of DSA and reduce defects. However, it is very important to note that the SDRAF sizes need to be controlled within a certain range to make sure that no etch-transferrable DSA patterns are generated inside the SDRAF. On the other hand, the SDRAF sizes also cannot be too small such that they cannot store enough polymer to reduce the overfilled conditions. We show the comparison between DSA performance with SDRAFs and without SDRAFs. It is important to note that the location of not-overfilled templates are detected through the contrast of their edges. Then the location of the overfilled templates are identified by a zoom-in view as these overfilled templates look as "disappeared" in the zoom-out view. These experimental data clearly show that SDRAFs help prevent the overfilled conditions, especially at the corner of the design pattern, where the template density is the lowest. However, as the SDRAFs size continues to increase, there will be DSA holes appearing inside the SDRAFs, which is counted as failure.

9423-51, Session 13

DSA-aware assist features

Azat M. Latypov, Tamer H Coskun, GLOBALFOUNDRIES Inc. (United States)

Directed Self-Assembly (DSA) of block copolymers (BCP) uses inter-molecular forces acting between the BCP macro-molecules to form the patterns ranging from low tens to few nanometers in size, guided by graphoepitaxy or chemical epitaxy patterns formed by coarser patterning techniques of DUV or EUV lithography [1]. Thus, DSA patterning complements and refines the patterning capabilities of DUV and EUV lithography, the latter being limited by the minimal achievable scale in the spatial variation of the external electromagnetic field in the resist material.

The DSA patterns are formed in the film of the BCP material, spin-coated on top of the substrate to be patterned. Following the formation of the DSA patterns in the BCP annealing process step, one of the segregated BCP components is selectively removed in a development or etching step of the DSA process, and the DSA pattern is etched into the substrate through the resulting openings in the BCP film.

Depending on the size and the shape of the graphoepitaxy confinement well, the BCP annealing step may form 3D DSA patterns in the BCP film which do not etch transfer into the substrate [2],[3] . Such properly shaped and sized confinement wells may be used to form "DSA fill features" serving to absorb the excess BCP material and to make the DSA process conditions more uniform across the wafer. Another important application of such non-etch transferable DSA features is that they can be used as "DSA-aware assist features" expanding the advantages provided by DUV/EUV lithography assist features (AFs) by further improving the process window and reducing the width of the process variation band (PV band) for the DUV/EUV process used to pattern the graphoepitaxy confinement wells.

The paper presents and discusses the concept of DSA-aware AFs [2],[3]. Such assist features can be viewed as an extension of an idea of printing AFs (PrAFs) (see [4], for example). For instance, in a graphoepitaxy DSA process, where the confinement wells are formed by DUV lithography, the DUV lithography process may use PrAFs, as long as the confinement wells resulting from printed AFs are sized and shaped so that they are "sealed" by the non-etch transferrable outcomes of the DSA process.

We also present the results of the tests for methods to place DSA-aware PrAFs optimally, for confinement wells fabricated using DUV lithography. These results are verified in DUV lithography simulations, combined with the simulation of the DSA process in these confinement wells. These simulations quantify the effect and the advantages provided by DSA-aware PrAFs in terms of the PV band of the DUV lithography process and the metrics of the DUV lithography process window.

REFERENCES

[1] D. Herr, "Directed block copolymer self-assembly for nanoelectronics fabrication," Journal of Materials Research, vol. 26, no. 02, pp. 122-139, 2011

[2] Azat Latypov, Tamer H. Coskun, Grant Garner, Moshe Preil, Gerard Schmid, Ji Xu and Yi Zou "Simulations of spatial DSA morphology, DSA-aware assist features and block copolymer-homopolymer blends", in Proc. SPIE 9049, Alternative Lithographic Technologies VI, 904908, San Jose, 2014

[3] W.-L. Wang, A. Latypov, Y. Zou and T. Coskun, "A full-chip DSA correction framework," in Proc. SPIE 9049, Alternative Lithographic Technologies VI, 90491J, San Jose, 2014

[4] Jason E. Meiring, Henning Haffner, Carlos Fonseca, Scott D. Halle and Scott M. Mansfield "ACLV driven double-patterning decomposition with extensively added printing assist features (PrAFs)", Proc. SPIE 6520, Optical Microlithography XX, 65201U, San Jose, 2007

9423-52, Session 14

Directed self-assembly of blends of block copolymers from different architectures in confinement: trends in morphology and defectivity

Bongkeun Kim, Univ. of California, Santa Barbara (United States); Peter Trefonas, The Dow Chemical Co. (United States); Kris T. Delaney, The Materials Research Lab. (United States); Glenn H Fredrickson, The Materials Research Lab. (United States) and Univ. of California, Santa Barbara (United States)

The directed self-assembly (DSA) of linear diblock copolymers to produce robust 10 nm scale line and space patterns or contact holes in topologically defined templates is a promising avenue to extend current lithographic tools. In this study, we use self-consistent field theory (SCFT) to investigate the DSA of blends containing cylinder-forming diblock copolymers both in narrow trenches and in single and multiple contact hole templates. We focus on wetting conditions and systems that form lying-down cylinder monolayers in narrow channels and vertical cylinders in hole-shrink configurations. Specifically, we explore the influence on the DSA process of blending small amounts of non-linear block copolymers with variable length and volume fraction of dissimilar species, into the linear diblock copolymers. Defect types, defect formation energies, critical dimensions, center-to-center distances and eccentricity in the self-assembled morphologies computed by SCFT are contrasted in the blends and pure diblock reference case. Parametric studies reveal the relationship between the architectural parameters defining non-linear copolymer additive and the concentration of the additive on process windows and defectivity in both line and space and contact hole DSA applications.

9423-53, Session 14

Advantages and limitations of density functional theory in block copolymer directed self-assembly

Jimmy Liu, Nabil Laachi, Kris T. Delaney, Glenn H. Fredrickson, Univ. of California, Santa Barbara (United States)

Directed self-assembly (DSA) of block copolymers is a promising emerging technique for cost-effective patterning in lithography applications. A major challenge in its implementation is the exploration of the design space, including the selection of confinement shape and size, wetting condition, copolymer chain length and block fraction. A wide range of models and simulation techniques have been applied to the study of this expansive design space.

Of these models, self-consistent field theory (SCFT) is among the most successful. Although the speed of SCFT calculations is sufficient for investigation of some applications, a faster model capable of broadening the range of parameter sweeps and simulating very large templates is still desirable. A popular approach is to construct a density functional, an expression for a polymer system's free energy as a functional of the local species density, typically through an asymptotic expansion about a homogeneous state. The resulting expression is an approximation of an SCFT model; however, controlling the validity of the approximation is presently more of an art than a systematic procedure.

In this study, we investigate various incarnations of the density functional theory (DFT) approach and evaluate their suitability to DSA applications via criteria such as predictions of commensurability and defectivity relative to SCFT. We also suggest methods to capitalize on the potential advantages of a DFT approach while minimizing the loss of accuracy relative to SCFT.

First, we compare the functional forms for diblock copolymers proposed by Leibler; Landau and Brazovskii; Bohbot-Raviv and Wang; Ohta and Kawasaki; and Uneyama and Doi. We then present a framework appropriate for running simulations with a general (modular) density functional, including an optimization procedure to fit parameters to SCFT calculations. Finally, we evaluate the results predicted by various functional forms under lamellar and cylindrical domain-forming conditions and in confinement. Based on the density fields and free energies of stable and metastable states predicted by both SCFT and DFT, we recommend procedures best suited to DSA applications and provide warnings about the limitations of DFT models with regard to defect prediction and commensurability windows.

9423-54, Session 14

Effect of chemoepitaxial guiding underlayer design on the pattern quality and shape of aligned lamellae for fabrication of line-space patterns

Benjamin D. Nation, Andrew J. Peters, Richard A. Lawson, Peter J. Ludovice, Clifford L. Henderson, Georgia Institute of Technology (United States)

Chemoepitaxial guiding of block copolymer (BCP) thin films, a version of directed self-assembly (DSA), is one method that can be used to achieve pattern density multiplication of patterns formed using conventional lithographic techniques such as optical lithography. Chemoepitaxy relies on the creation and use of guiding layers that contain chemically patterned surfaces with pattern-wise variation in properties such as surface energy. When making these underlayers with the purpose of guiding line-space type patterns formed from lamellar-forming block copolymers, typically a repeating pattern will be made that consists of a thin, highly preferential stripe (i.e. with respect to the regions energetic interaction with one of the copolymer blocks), known as a pinning stripe. These pinning stripes are spaced apart from one another generally by a larger, more neutral region in terms of its interaction with the blocks of the copolymers, known as the neutral or background region. This type of chemoepitaxy approach has been shown to be capable of yielding large areas of defect free lamellae by varying properties of the underlayer, such as altering the composition of the background region. It has also been shown that making the background region moderately preferential to the block of the BCP that does not preferentially wet the pinning stripe is actually ideal with regards to aligning the BCP film. However, varying the composition of the background region in this way can cause the lamellae quality to degrade by causing the lamellae to "foot" near the bottom, which can be problematic when anisotropic etching is performed on the BCP film to achieve relief pattern structures. The extent to which the shape of the aligned BCP is altered is not fully understood, and is quite difficult to probe experimentally. In this paper, a coarse-grained molecular dynamics model is used to systematically study these underlayers in order to determine what penalties to lamellae quality might exist when designing the neutral or background compositions and making such large, defect free, density multiplied pattern areas. The process windows based on (1) achieving best pattern alignment metrics (i.e. edge placement error), (2) best edge quality metrics (i.e. LER/LWR), and (3) best sidewall angle metrics will be compared with the goal of elucidating design rules for the optimum underlayers to be used in chemoeptiaxial DSA.

9423-55, Session 14

The effects of geometry and chemistry of nanopatterned substrates on the directed self-assembly of block-copolymer blends

Grant P. Garner, The Univ. of Chicago (United States); Paulina A. Rincon Delgadillo, IMEC (Belgium); Lance D. Williamson, The Univ. of Chicago (United States); Roel Gronheid, IMEC (Belgium); Paul F. Nealey, Juan J. de Pablo, The Univ. of Chicago (United States)

Directed self-assembly of block copolymers over chemically patterned substrates has proven to be an effective method for sublithographic patterning. Features on these chemical patterns can be multiplied by the natural domain-spacing of the block copolymer assembled on top of the substrate through pattern interpolation. The Liu-Nealey (LiNe) chemo-epitaxy flow for directed self-assembly allows for modification of the geometry and chemistry of the nanopatterned substrate. The critical dimensions and period along with the chemical composition of the patterned features in the LiNe flow govern the equilibrium morphology of the assembled block copolymer. Altering the composition of the copolymer melt assembled on top of the substrate by adding homopolymer changes the natural domain spacing as well as assembly behavior. We demonstrate how the construction of the chemical pattern affects the assembled three-dimensional equilibrium structure of different block copolymer blends by using a theoretically informed coarse-grained many-body model of block copolymers. The molecular simulations are compared with recent experimental findings to provide an explanation for how to best design the guiding features and the block copolymer blends used in the LiNe flow to achieve desired morphologies.

9423-56, Session 14

Effect of ?N and underlayer composition on self-assembly of thins films of block copolymers with energy asymmetric blocks

Richard A. Lawson, Andrew J. Peters, Benjamin D. Nation, Peter J. Ludovice, Clifford L. Henderson, Georgia Institute of Technology (United States)

Directed self-assembly (DSA) of block copolymers (BCPs) is receiving

much attention as a complementary or alternative lithographic technique to conventional top-down optical lithography. Much of the early learning for this technique has been done with relatively low ? (Flory-Huggins interaction parameter) BCPs such as polystyrene-block-poly(methyl-methacrylate) (PS-PMMA). In order to obtain the high quality sub-15 nm features needed for next generation high volume manufacturing, different BCP materials must be used with higher - values in order to obtain the desired smaller feature sizes. Unlike many lower - BCPs, higher - materials often have large block energy and/or density asymmetry, meaning that each block has a different homopolymer density or cohesive energy density (CED). CED is a particularly important parameter because BCPs with large differences in CED can lead to a number of problems that have only just begun to be investigated such as preferential wetting or "skinning" of the top-surface of a BCP film by one of the blocks. In order to accelerate the understanding of the effect of block asymmetry on self-assembly, simulation tools that allow independent manipulation of the density and CED of each block are required. This is difficult for many simulation tools which don't explicitly consider or lack the capability to vary the CED or density of each block. We have developed a simulation of BCP behavior and DSA processes based on molecular dynamics (MD) of coarse-grained polymer chains simulated using graphics processing units (GPUs) to perform the calculations. Since this simulation uses off-lattice Lennard-Jones type interactions, it is easy to vary the CED and density of each block by changing their force-field parameters. Recently1, we used the model to examine the effect of block asymmetry on a broad variety of BCP behaviors such as the order-disorder transition (ODT), domain scaling, and self-assembly of thin films of BCPs. Energy asymmetry leads to large deviations in thin film behavior and morphology compared to symmetric BCPs because the lowest CED block tends to segregate to the top of the film, making the formation of vertical lamellae difficult or impossible without additional surface energy modification at the free interface such as a top-coat. For some simulation conditions, we found that if the χN value of the energy asymmetric BCP is sufficiently high, some asymmetric material would actually form vertical lamellae that would not at lower χN values. Figure 1 shows a symmetric BCP (top) and asymmetric BCP (bottom) on a neutral substrate for different χN values. The symmetric BCP forms vertical lamellae over the whole χN range, while the asymmetric BCP shows horizontal lamellae driven by preferential wetting of the air interface by the low energy block until the χN value for the block copolymer is sufficiently high. This paper seeks to understand which conditions are most favorable for vertical lamellae formation in block copolymers by examining the effect of domain size, χN, underlayer composition, film thickness, and amount of block asymmetry on thin film morphology. Figure 2 shows an example of some of these results for an energy asymmetric BCP with different χN on each row and different underlayer composition in each column. The optimal underlayer composition changes with χN.

Conference 9424: Metrology, Inspection, and Process Control for Microlithography XXIX

Monday - Thursday 23–26 February 2015

Part of Proceedings of SPIE Vol. 9424 Metrology, Inspection, and Process Control for Microlithography XXIX

9424-1, Session 1

Tactical and strategic metrology perspectives for advanced integrated circuit development and manufacturing *(Keynote Presentation)*

Eric Solecky, Alok Vaid, GLOBALFOUNDRIES Inc. (United States)

No Abstract Available

9424-3, Session 2

More systematic errors in the measurement of power spectral density

Chris A Mack, Lithoguru.com (United States)

Measurement of the power spectral density (PSD) of a rough surface or feature involves large random and systematic errors. While random errors can be reduced by averaging together many PSDs, systematic errors can be reduced only by carefully studying and understanding the sources of these systematic biases. In a previous study, [1] several significant sources of systematic bias in the measurement of the PSD for line-edge or linewidth roughness measurements were identified and characterized. Spectral leakage is caused by the measurement of a finite length of line and can be mitigated through the use of data windowing. Aliasing is caused by the use of a non-zero sampling distance and can be mitigated by adjusting the sampling distance in relation to the interaction range of the SEM measurement spot (or the tip size for AFM). SEM measurement noise has also been characterized as a source of bias. [2]

In this paper, further sources of systematic errors, specifically for the measurement of line-edge roughness (LER), will be described and analyzed. LER involves the fitting of a line to a measured edge and using the residuals to calculate the roughness and the PSD. The use of an arbitrary best-fit line allows for the possibility of SEM sample rotation, which is taken out because of the arbitrary slope of the best-fit line. However, roughness with a wavelength on the order of the measurement length will also be removed. Thus, this best-fit line biases the lowest frequencies of the PSD measurement downward, and systematically changes the shape of the autocorrelation function extracted from a PSD. This bias is complicated when multiple lines are in the SEM field of view, and only one rotation is taken out universally for all measured edges.

This paper will define mathematically the impact of SEM sample rotation subtraction on the PSD, discuss its impact on PSD interpretation, and suggestion possible mitigation strategies. Simulations using the previously described MetroSim metrology simulator [1] will also be used to confirm the analytical derivations.

[1] Chris A. Mack, “Systematic Errors in the Measurement of Power Spectral Density”, Metrology, Inspection, and Process Control for Microlithography XXVII, Proc., SPIE Vol. 8681 (2013) p. 86812I.

[2] J. S. Villarrubia and B. D. Bunday, “Unbiased Estimation of Linewidth Roughness”, Proc. SPIE, 5752, 480-488 (2005).

9424-4, Session 2

Application of frequency domain line-edge roughness characterization methodology in lithography

Lei Sun, Wenhui Wang, Obert R. Wood II, Ryoung-Han Kim, GLOBALFOUNDRIES Inc. (United States)

No Abstract Available

9424-5, Session 2

The effect of sidewall roughness on line edge roughness in top-down scanning electron microscopy images

Thomas Verduin, Sebastiaan R. Lokhorst, Cornelis W. Hagen, Pieter Kruit, Technische Univ. Delft (Netherlands)

This work addresses the delicate issue of roughness characterization of line edges.

In a previous study we determined the Line Edge Roughness (LER) in low dose top-down Secondary Electron Microscopy (SEM) images.

However, the true size, shape and roughness characteristics of resist features are not fully determined in the analysis of top-down SEM images.

The reason is that in reality, resist features are three dimensional structures.

The characterization of roughness of resist features naturally extends to the analysis of Sidewall Roughness (SWR) which can be measured, for instance, by using an Atomic Force Microscopy (AFM).

However, in view of the large volume of wafers being produced in a typical production line, AFM is not considered as a suitable metrology tool.

Another problem with AFM involves the complexity of the measurement, in which the exact shape of the tip plays a crucial role.

Numerical Studies on SWR in literature reveal that the true SWR is larger than the measured LER in a top-down image.

Roughness, however, is typically characterized by more than just the standard deviation and involves parameters, such as correlation length and roughness exponent.

In this study we extend the roughness analysis by including standard deviation, correlation length and roughness exponent in SWR.

At first we randomly generate edges with SWR using the Palasantzas model and the algorithm of Thorsos.

We then generate top-down SEM images from the (three dimensional) rough edges by using a Monte-Carlo (MC) simulation of electron scattering.

Finally, the line edges are analyzed from the top-down SEM images by using power spectral density analysis.

In a first attempt, we have used (in view of computational time) a simplified scattering model for simulating SEM images.

For the SPIE conference, we intend to use a more sophisticated scattering model for simulating SEM images.

The preliminary results suggest that LER not only depends on the standard deviation of SWR, but also the correlation length and roughness exponent.

Our ultimate goal is to characterize SWR from top-down SEM images.

Conference 9424: Metrology, Inspection, and Process Control for Microlithography XXIX

9424-6, Session 2

Line profile measurement of advanced-FinFET features by reference metrology

Kiyoshi Takamasu, Yuuki Iwaki, Satoru Takahashi, The Univ. of Tokyo (Japan); Hiroki Kawada, Hitachi High-Tech Science Corp. (Japan); Masami Ikota, Hitachi High-Technologies Taiwan Corp. (Japan); Atsuko Yamaguchi, Hitachi, Ltd. (Japan); Gian F. Lorusso, Naoto Horiguchi, IMEC (Belgium)

A novel method of sub-nanometer uncertainty for the line profile measurement using TEM (Transmission Electron Microscope) images is proposed to calibrate CD-SEM line width measurement and standardize line profile measurement with reference metrology. In accordance with the proposed method, we have already established the methodology for profile of Si line and photoresist feature for reference metrology in our previous investigations. In this article, we apply the proposed method to the line profile measurement of advanced-FinFET features. The FinFET features are sliced as thin specimens of 100 nm thickness by FIB (Focused Ion Beam) micro sampling system. Then cross-sectional images of the specimens are obtained by TEM. The line profile of FinFET features is defined using TEM images. We compare the line width of the fin measured by the proposed method and CD value by CD-SEM measurement. Moreover, for the high speed measurement, we examine FIB-scrape method. As we can reconstruct the line profile of the fin, we compare it with the cross-section TEM image. The results will be applied to CD-SEM and CD-AFM reference metrology.

9424-7, Session 2

Induced e-beam charge impact on spatial orientation of gate-all-around silicon wires device fabricated on Boron Nitride substrate

Shimon Levi, Konstantin Chirko, Ofer Adan, Applied Materials, Ltd. (Israel); Guy Choen, IBM Corp. (United States)

For Gate-all-around (GAA) MOSFETs the nanowires are suspended between sources and drain bulks to allow conformal deposition of the gate around (i.e., GAASiNW) the silicon nanowire channel. 3DSEM measurement results demonstrate that silicon wires tend to buckle between the source and drain bulks as function of their diameter and length. This phenomenon can impact device performance and therefor need to be measured. Resent metrology research performed on Silicon wires fabricated on Boron Nitride substrate demonstrated that silicon wires spatial orientation is influenced by local electrostatic charge induced by the SEM electron beam irradiation. The scanning electron beam is generating different trapped charge accumulation in the conductive silicon wires and the dielectric material Boron Nitride substrate that leads to appearance of a coulomb forces acting between them.

Controlling the amount of charging by modifying scan rate, we were able to change the spatial orientation of Silicon wires. Strong charging, which corresponds with slow scan rate, causes strong attraction between the silicon wires and Boron Nitride substrate.

It is manifested as silicon wires sagging toward the wafer substrate, their appearance are straightening in SEM top view image plane. Reducing charging by the means of scan rate increase saves the silicon wires buckled in their natural state.

In this work we present a scenario of charge accumulation based on our analysis of the SEM signal dynamics, depending on scan parameters. We reveal scanning conditions that allows de-coupling charging degree and scanning rate that obtain the required SNR while not influencing Silicon wires buckling orientation. The sensitivity of this ultra-small device to local surface charge can be used as a probe to evaluate efficacy of SEM charge control techniques.

9424-8, Session 3

Hybrid overlay metrology with CDSEM in a BEOL patterning scheme

Philippe J. Leray, IMEC (Belgium); Yutaka Okagawa, Osamu Inoue, Hitachi High-Tech Science Corp. (Japan); David Laidler, Jan V. Hermans, IMEC (Belgium)

Overlay metrology accuracy is a major concern for our industry. Advanced logic process require more tighter overlay control for multipatterning schemes. TIS (Tool Induced Shift) and WIS (Wafer Induced Shift) are the main issues for IBO (Image Based Overlay) and DBO (Diffraction Based Overlay). Methods of compensation have been introduced, some are even very efficient to reduce these measured offsets. Another related question is about the overlay target designs. These targets are never fully representative of the design rules, strong efforts have been achieved, but the device cannot be completely duplicated. Ideally, we would like to measure in the device itself to verify the real overlay value.

Top down CDSEM can measure critical dimensions of any structure, it is not dependent of specific target design. It can also measure the overlay errors but only in specific cases like LELE (Litho Etch Litho Etch) after final patterning. In this paper, we will revisit the capability of the CDSEM at final patterning by measuring overlay in dedicated targets as well as inside a logic and an SRAM design. In the dedicated overlay targets, we study the measurement differences between design rules gratings and relaxed pitch gratings. These relaxed pitch which are usually used in IBO or DBO targets. Beyond this “simple” LELE case, we will explore the capability of the CDSEM to measure overlay even if not at final patterning, at litho level.

We will assess the hybridization of IBO,DBO and CDSEM in 2 way , one is for reference to optical tools and another is for production use . (after final patterning and after litho). We will show that these reference data can be used to validate the IBO and DBO overlay results (correctables and residual fingerprints).

9424-9, Session 3

Scatterometry or imaging overlay: a comparative study

Nuriel Amir, KLA-Tencor Israel (Israel); Simon C. C. Hsu, Yuan Chi Pai, Charlie Chen, Chun Chi Yu, United Microelectronics Corp. (Taiwan); Henry Hsing, Robert H. C. Wu, Kelly T. L. Kuo, KLA-Tencor Taiwan (Taiwan)

Most fabrication facilities today use imaging overlay measurement methods, as it has been the industry’s reliable workhorse for decades. In the last few years, third-generation Scatterometry Overlay (SCOL™) technology was developed, leading to question of where the technology should be implemented for overlay measurements. Scatterometry has been adopted for high volume production in a few cases, but is considered by many as the technology of the future. In this paper we compare imaging-based and scatterometry-based overlay technologies by means of measurements and simulations. We outline issues and sensitivities for both technologies, providing guidelines for the implementation of each. For several of the presented cases, data from two different scatterometry-based overlay measurement vendors are compared as well. Key indicators of overlay measurement quality include: accuracy, TMU, MAM time and process robustness. Measurement data from real cases are compared and the conclusions are also backed by simulations. Accuracy is benchmarked with electrical testing, showing good results for both technologies, in most cases. Process sensitivity and metrology robustness are mostly simulated with MTD (Metrology Target Designer) comparing the same process variations for both technologies. The study was done on ten state of the art 14 nm node layers and three 28 nm node layers, for all phases of the IC fabrication process (FEOL, MEOL and BEOL). The metrology tools used for the study are KLA-Tencor’s next-generation Archer 500 system (scatterometry- and imaging-based measurement technologies on the same tool) and a second vendor’s scatterometry-based tool.

Finally, we conclude that both technologies are successful and have a valid roadmap for the next few design nodes, with some use cases better suited for one or the other measurement technologies. Having both options available in parallel, allows fabs a mixed-mode overlay measurement strategy, providing back up when encountering difficulties with one of the technologies and benefiting from the best of both technologies for every use case.

9424-10, Session 3

64nm pitch metal1 double-patterning metrology: CD and OVL control by SEMCD, image-based overlay and diffraction-based overlay

Florent Dettoni, Julien Ducoté, Régis Bouyssou, Bertrand Le-Gratiet, STMicroelectronics (France); Damien Carau, STMicroelectronics (France) and LTM CNRS (France); Christophe Dezauzier, STMicroelectronics (France)

Patterning process control of advanced nodes has required major changes over the last few years. Process control needs of critical patterning levels since 28nm technology node is extremely aggressive showing that metrology accuracy/sensitivity must be finely tuned.

The introduction of pitch splitting (Litho-Etch-Litho-Etch) at 14nm node requires the development of specific metrologies to adopt advanced process control (for CD, overlay and focus corrections). The pitch splitting process leads to final line CD uniformities that are a combination of the CD uniformities of the two exposures, while the space CD uniformities are depending on both CD and OVL variability.

In this paper, investigations of CD and OVL process control of 64nm minimum pitch at Metal1 level of 14FDSOI technology, using various metrology types and tools at several steps within the double patterning process flow (litho, hard mask etch, line etch) are presented. Based on those results correlations between different metrologies are demonstrated and evaluation of models of sampling plan and process corrections is proposed.

Various measurements with SEMCD tools (Hitachi), scatterometry tools (Nanometrics) and overlay tools (KT for Image Based Overlay – IBO, and ASML for Diffraction Based Overlay – DBO) are compared. Metrology targets are embedded within a block instanced several times within the field to perform intra-field process variations characterizations.

Specific SEMCD targets were designed for independent measurement of both line CD (A and B) and space CD (A to B and B to A) for each exposure within a single measurement during the DP flow.

Based on those measurements correlation between overlay determined with SEMCD and with standard overlay tools can be evaluated. The figure below illustrates the correlation between overlay extracted from SEMCD measures after hard mask etch of exposure B and overlay measured by DBO after lithography of exposure B.

Such correlation at different steps through the DP flow is investigated regarding the metrology type. Process correction models are evaluated with respect to the measurement type and the intra-field sampling.

9424-11, Session 3

Influence of the process-induced asymmetry on the accuracy of overlay measurements

Tetyana Shapoval, KLA-Tencor Germany (Germany); Bernd Schulz, GLOBALFOUNDRIES Dresden Module Two, GmbH & Co. KG (Germany); Tal Itzkovich, KLA-Tencor Israel (Israel); Sean Durran, KLA-Tencor Ireland (Ireland); Ronny Haupt, KLA-Tencor Germany (Germany); Agostino Cangiano, KLA-Tencor Italy SRL (Italy); Barak Bringoltz, KLA-Tencor Israel (Israel); Matthias Ruhm, GLOBALFOUNDRIES Dresden Module One LLC & Co. KG (Germany); Eric Cotte, Rolf Seltmann, Tino Hertzsch, GLOBALFOUNDRIES Dresden Module Two, GmbH & Co. KG (Germany); Eitan Hajaj, KLA-Tencor Israel (Israel); Carsten Hartig, GLOBALFOUNDRIES Dresden Module Two, GmbH & Co. KG (Germany); Boris Efraty, KLA-Tencor Israel (Israel); Daniel Fischer, GLOBALFOUNDRIES Dresden Module Two, GmbH & Co. KG (Germany)

The accuracy of overlay metrology becomes crucial when shrinking device dimensions to nodes below 2X nm. The commonly used characteristic performance metrics of overlay measurements like TMU (Total Measurement Uncertainty), which includes precision, tool induced shift (TIS) and TIS variability, do not appear to be sufficient for the 2X nm nodes and below. Having very reliable and well defined TMU of the metrology does not address how one can be sure that the precisely measured overlay is representative of the behavior in the device. The main cause of inaccuracy is symmetry breaking process variations. However, as reported previously, the misalignment of the layers with distinct wafer signature could be induced by stress [1] or other non-litho related processes such as etch [2]. In this paper, we will address three questions relevant for accuracy: 1. Which target design (pitch and segmentation) has the best performance and depicts the behavior of the actual device? 2. Which metrology signal characteristics could help to distinguish between the target asymmetry related overlay shift and the real process related shift (e.g. stress released)? 3. How does uncompensated asymmetry of the previous layer target, generated during after-litho processes, affect the propagation of overlay error through different layers?

We are presenting the correlation between simulation data based on the optical properties of the measured stack and KLA-Tencor Archer overlay measurements on a 28 nm product through several critical layers (active area, gate, contact, metal and via) for those accuracy aspects.

Based on the optical simulation we defined optimal segmentation and pitch for the AIM target. Overlay measurements confirmed the best TMU and target symmetry (Qmerit accuracy flag [3]) for the new design. Additionally, color selection based on the Qmerit value correlates with the best performance of the target. Due to the wavelength dependence of the material's optical properties, the color filter used for image grab not only influences the performance of the target but also the accuracy and sensitivity to asymmetry. The influence of the tilted etched target of the previous layer on the overlay failure in the following layer is investigated both by simulation and by measurements.

9424-12, Session 3

Overlay accuracy investigation for advanced memory device

Hong-Goo Lee, Byongseog Lee, Sangjun Han, Myoung Soo Kim, Won-Taik Kwon, Sung-Ki Park, SK Hynix, Inc. (Korea, Republic of); Dong-Sub Choi, Do-Hwa Lee, KLA-Tencor Korea (Korea, Republic of); Sanghuck Jeon, Kangsan Lee, SK Hynix, Inc. (Korea, Republic of); Amnon Manassen, Yuri Paskover, KLA-Tencor Israel (Israel); David C. Tien, KLA-Tencor Corp. (United States); Negri Daria, Tal Itzkovich, David Gready, Eitan Herzel, KLA-Tencor Israel (Israel)

Overlay in the lithography becomes much more challenging due to the shrink of device node and multi-patterning approach. Consequently, the specification of overlay becomes tighter and more complicated overlay control method like high order or field-by-field control becomes mandatory. In addition, the tight overlay specification starts to raise another fundamental question, accuracy. Overlay inaccuracy is dominated by two main components; one is measurement quality and the other is representing device overlay. The latter is because overlay is being measured on overlay

target, not on the real device structure.

We investigated the followings for accurate overlay measurement

- Optimal target design by simulation: both Imaging and SCOL
- Optimal recipe including measurement algorithm
- Correlation with device pattern's overlay

Simulation was done for advanced memory stack for optimal overlay target design which provide robustness for the process variation and sufficient contrast/signal for the stack. Robustness factor and contrast factor normally contradicting each other, therefore there is trade-off between these two factors. Simulation helped to find the design to meet the requirement of both factors

The investigation involves also recipe optimization which decide the measurement conditions like wavelength, focus position, ...etc. KLA-Tencor also introduced new measurement algorithm which enhance the measurement itself, especially for the target which damaged by production process. Obviously, target design is one knob to maintain the robustness from process, but we also enhanced the robustness with new algorithm as well.

In this investigation, we used CD-SEM to measure the overlay of device pattern after etch or de-cap process to check the correlation between the overlay of overlay mark and the overlay of device pattern.

9424-13, Session 3

Stack and topography verification as an enabler for computational metrology target design

Michael E. Adel, Inna Tarshish-Shapir, David Gready, Mark Ghinovker, KLA-Tencor Israel (Israel); Stephane Godny, IMEC (Belgium)

The pushout of EUV has set the stage for double and quadruple patterning to dominate the 10 and 7 nm nodes. This has major ramifications for metrology target design. The number of layers per stack, even for what was previously considered a single patterning step such as the poly layer has compounded. Since overlay metrology needs to probe both current and previous patterned layers, the effects are two-fold. Firstly, the previous layer is now buried under complex strata of functional and sacrificial layers, each of which may suffer from surprisingly large process variations at least in the process development stages when targets are designed. Secondly, in order to probe the underlayer, in many cases, metrology wavelengths have been driven into the near infra-red to penetrate multiple carbon and sometimes silicon based hard masks, BARCs and photo-resists. Pupil and real imaging based metrology methods rely on collection of at least two diffraction orders, so Bragg's law dictates a widening gap between measureable target pitches and device design rule pitches.

These large pitch target structures have been set adrift by process integration teams who are primarily focused on optimizing advanced processes for single digit nanometer features. For several generations now target designs have become more complex in an attempt to maintain process compatibility as the gap widens between minimum device pitch and target pitch. Parallel and orthogonal feature segmentation is a familiar strategy to all metrology engineers but to these have been added under and intermediate layer dummification and more recently CMP assist features. The space of a target Design of Experiment (termed t-DOE) has become enormous when process variations and their impact on sensitivity and accuracy are to be taken into account in simulations comparing various geometric design contenders.

And if this isn't enough we now throw in the real curve balls of CMP dishing and induced topography. If one wants to predict accuracy, sensitivity and in particular process robustness as a function of geometry and wavelength, one needs to know the magnitude, or at least, the presence or absence of these process effects. This sets the stage for the metrology engineer who now has to become a stack and topography verification expert. So in this paper we shall focus on a comparison of different methods for stack and topography verification in advanced processes but in the practical light of a real process development environment. Methods characterized will include cross-section SEM, FIB HR-SEM, TEM and OCD on dedicated targets. The improvement in matching between simulation and measurement resulting from stack and topography verification will be quantified.

9424-14, Session 3

Overlay metrology solutions in a triple patterning scheme

Philippe J. Leray, Ming Mao, Bart Baudemprez, IMEC (Belgium); Nuriel Amir, KLA-Tencor Israel (Israel)

Overlay metrology tool suppliers are offering today several options to their customers: Different hardware (Image Based Overlay or Diffraction Based Overlay), different target designs (with or without segmentation) or different target sizes (from 5 um to 30 um). All these variations are proposed to resolve issues like robustness of the target towards process variations, be more representative of the design or increase the density of measurements.

In the frame of the development of a triple patterning BEOL scheme of 10 nm node layer, we compare IBO targets (standard AIM, AIMid and multilayer AIMid), CDSEM (in design measurements) and third-generation Scatterometry Overlay (SCOL™) technology. The metrology tools used for the study are KLA-Tencor's next-generation Archer 500 system (scatterometry- and imaging-based measurement technologies on the same tool).

The overlay response and fingerprint of these targets will be compared using a very dense sampling (up to 51 pts per field). The benefit of indie measurements compared to the traditional scribes is discussed. The contribution of process effects to overlay values are compared to the contribution of the performance of the target. Different targets are combined in one measurement set to benefit from their different strengths (performance vs size).

The results are summarized and possible strategies for a triple patterning schemes are proposed.

9424-15, Session 4

Analytical linescan model for SEM metrology

Chris A. Mack, Lithoguru.com (United States); Benjamin D. Bunday, SEMATECH Inc. (United States)

A critical dimension (CD) scanning electron microscope (SEM) converts a measured linescan into a single dimension number. To better understand how the linescan relates to the actual dimensions of the feature being measured, it is important to understand how the systematic response of the SEM measurement tool to wafer structures impacts the shape of the resulting linescan. Rigorous 3D Monte Carlo simulations of SEM linescans can be extremely valuable for this purpose, but they are often too computationally expensive for day-to-day use. Thus, one approach will be to develop a simplified, analytical linescan model that will be more computationally appropriate to the task of analyzing linescans. This analytical linescan expression will then be fit to the rigorous Monte Carlo simulations to both validate and calibrate its use.

In this work, JMONSEL simulation [1] is used to better understand how various SEM parameters, beam size/shape, and sample profile influence the linescan (Figure 1). In a previous study [2], a simplified linescan model was developed for a vertical, isolated step.

This model was shown to fit JMONSEL simulations extremely well (Figure 2) for silicon and PMMA steps at various landing voltages. In this study, the linescan model will be extended to different step materials, various step heights, sloped edges, and interacting edges (lines and trenches of varying widths and pitch). The result will be a calibrated linescan model that could prove very useful for better analyzing and interpreting experimental linescans.

9424-16, Session 4

Solving next-generation (1x node) metrology challenges using advanced CDSEM capabilities: tilt, high energy, and backscatter imaging

Xiaoxiao Zhang, Alok Vaid, Patrick W. Snow, Eric Solecky, GLOBALFOUNDRIES Inc. (United States); Jessica Zhou, Adam Ge, Shay Yasharzade, Applied Materials, Inc. (United States); Ori Shoval, Ofer Adan, Ishai Schwarzband, Maayan Bar-Zvi, Applied Materials, Ltd. (Israel)

Traditional metrology solutions are facing a range of challenges at the 1X node such as three dimensional (3D) measurement capabilities, shrinking overlay and critical dimension (CD) error budgets driven by multi-patterning and via in trench CD measurements. Hybrid metrology offers promising new capabilities to address some of these challenges but it will take some time before fully realized. This paper explores new capabilities currently offered on the in-line Critical Dimension Scanning Electron Microscope (CD-SEM) to address these challenges and move the CD-SEM beyond primarily measuring bottom CD using top down imaging.

Device performance is strongly correlated with Fin geometry causing an urgent need for 3D measurements (Figure 1). New beam tilting capabilities enhance the ability to make 3D measurements in the front end of line (FEOL) of the metal gate FinFET process in manufacturing. We explore these new capabilities for measuring Fin height and build upon the work communicated last year at SPIE1. Furthermore, we extend the application of the tilt beam to the back end of line (BEOL) trench depth measurement.

According to International Technology Roadmap for Semiconductors (ITRS) from 2013, the overlay 3 sigma requirement will be 3.3 nm in 2015 and 2.9 nm in 2016. Advanced lithography requires overlay measurement in die on features resembling the device geometry. However, current optical overlay measurement is performed in the scribe line on large targets due to optical diffraction limit. Both its measurement location and physical geometry do not represent the true behavior of the device2. We explore using high voltage imaging to address the urgent need on overlay (Figure 2). Novel CD-SEM based overlay targets that optimize the restrictions of process geometry and SEM technique were designed and spread out across the die. Measurements are done on these new targets both after photolithography and etch. Correlation is drawn between the two measurements. These results will also be compared to conventional optical overlay measurement approaches and we will discuss the possibility of using this capability in high volume manufacturing.

Lastly, in the back end of line (BEOL), another increasingly challenging measurement for the traditional CD-SEM is the bottom CD of the self-aligned via (SAV) in a trench first via last (TFVL) process. Due to the extremely high aspect ratio of the structure (Figure 3) secondary electron (SE) collection from the via bottom is significantly reduced requiring the use of backscatter electrons to increase the relevant image quality. Even with this solution, the resulting images are difficult to measure with advanced technology nodes. (Figure 4) We explore new backscatter methods to increase measurement robustness and combine this with novel segmentation-based measurement algorithm generated specifically for BSE images. The results will be contrasted with data from previously used methods to quantify the improvement. We also compare results from this segmentation algorithm (applied on improved BSE imaging) to electrical test data to evaluate and quantify the measurement performance improvements.

9424-17, Session 4

Methodology for determining CD-SEM measurement condition of sub-20nm resist patterns for 0.33NA EUV lithography

Nobuhiro Okai, Hitachi, Ltd. (Japan); Erin Lavigne, IBM Corp. (United States); Keiichiro Hitomi, Hitachi America, Ltd. (United States); Scott D. Halle, IBM Corp. (United States); Shoji Hotta, Hitachi, Ltd. (Japan); Shunsuke Koshihara, Hitachi High-Tech Science Corp. (Japan); Junichi Tanaka, Hitachi, Ltd. (Japan); Todd C. Bailey, IBM Corp. (United States)

Establishing a BKM (best known method) in CD-SEM metrology has been a longstanding challenge because there are many CD-SEM parameters to be optimized and conflicting requirements to meet both small resist shrinkage and high precision. We developed a methodology using Taguchi method with L18 array to predict shrinkage and precision at all the combinations of the parameter settings in L18 array to establish BKM for ArF resist pattern in 2012. However, the transition from ArF to EUV lithography may require new methods to establish BKM because resist material, pattern formation mechanism in the resist, resist thickness, and delineated CDs and pitches of the patterns are totally different.

In this paper, we developed a new BKM methodology which can be applied to optimization of measurement conditions for sub-20 nm EUV resist patterns created by 0.33 NA EUV tool. We found that the conventional method to predict shrinkage is no longer applicable to fine EUV resist pattern because there is a large prediction error. Then, we proposed a new method to predict shrinkage for any combinations of parameter settings using shrinkage curve obtained in advance to reduce prediction error of shrinkage. On the other hand, precision was predicted accurately by conventional method, so the same procedure was applied in the new method regarding prediction of precision. The optimum condition is determined based on the predicted shrinkage and precision. Our new method is a versatile technique which is applicable not only to fine EUV resist pattern but also to ArF pattern, and it should be a great help for finding optimum CD-SEM measurement condition.

9424-18, Session 4

Fast analytical modeling of SEM images at a high level of accuracy

Sergey Babin, Sergey S. Borisov, Vladimir Trifonenkov, abeam Technologies, Inc. (United States)

SEMs are an indispensable part of manufacturing, especially in CD metrology and defect inspection and review. A detailed understanding of the mechanisms behind image formation would improve setup optimization in factories and help in system development. Monte Carlo simulators of electron scattering and image formation provide highly accurate results by modeling the scattering of each electron, including slow secondary electrons, until they reach the detector. Advanced simulators include electron scattering of primary and secondary electrons, as well as the detectors, electromagnetic fields and charging. However, the high accuracy comes at the cost of long simulation times. During the last few years, a few extremely simple models of SEM, or emulators, have been developed. While the modeled images looks roughly like SEM images, the capabilities of such emulators are extremely limited and, in fact, misleading.

We developed an analytical model of the SEM which takes into account the major effects of electron scattering and image formation in the SEM. The beam voltage and size, scanning parameters of the beam, physical properties of the materials and 3D shapes of features are considered. The locations and properties of both the backscattering and secondary electron detectors are modeled. Extracting or suppressing electrical fields over the sample is also taken into account. Finally, sample charging is also considered.

This complex modeling makes the simulation results accurate. In this way, this is a true analytical model of an SEM, not just an emulator. On the other hand, simulation time is short. It has been proven that the typical simulation time is within one minute - a huge improvement compared to Monte Carlo simulators that take multiple hours. ASEM is a software developed for the analytical modeling of SEMs. Simulations of a variety of test samples at variable beam settings were performed. These examples of simulations are discussed and compared to SEM images.

9424-19, Session 4

Simulating multi-electron-beam wafer inspection for sub-20nm defects

Benjamin D. Bunday, SEMATECH Inc. (United States); Brad Thiel, Kathryn W. Quoi, Maseeh Mukhtar, SUNY College of Nanoscale Science and Engineering (United States)

Fast wafer inspection for patterned defects within maximum density patterns is a key metrology capability gap at upcoming ITRS nodes.[1] Brightfield inspection for such critical defects, meaning those larger than half a node's pitch, is already facing sensitivity issues as critical defects become smaller than 20nm.[2] Electron beam inspection tools can be sensitive to defects which are 5nm or smaller, although the speed of such tools with a single electron beam column is, by two or three orders of magnitude, inadequately slow for replacing brightfield inspection in the traditional high volume manufacturing role of full wafer defect inspection. One approach to overcome this speed deficit is to use a small number of parallel beams, say ten, with faster scanning capabilities. While this approach is being pursued by vendors at present, it is likely not enough to meet the "1 hour per wafer" capacity demanded by chip manufacturers. To address this gap in defect inspection capability, SEMATECH has initiated a program to accelerate the development and commercialization of multi-electron beam based technologies, exploring massively-parallel scanning by hundreds or thousands of electron beams.[3] In implementing such tooling, many factors must be considered. Among these are influences of tool design and choice of operating parameters on the defect signature sensitivity. These choices are likely process/application dependent, and also should be dependent on the types and sizes of the defects of interest.

It is not always possible to construct samples to experimentally determine the performances of the wide range of possibilities in the parameter space above, in a controlled manner to exactly replicate a defined situation of exact pattern with exact defined defects; nor is it possible to construct all the possible variations in tools for addressing such parameters. However, simulations can be used to model the possibilities and identify the trends. In this paper, we explore the impacts of material set, electron beam conditions and scanning parameters on defect signature sensitivity. Defect types include a few important test cases, such as point particles on unpatterned and patterned backgrounds, bridge defects, etc., with these defects spanning the size range from 15nm to 5nm. To generate test images for virtual experiments, we use JMONSEL simulations [4][5][6] to generate the expected responses to a few chosen cases of patterns and defects, with ability to vary parameters for beam energy, spot size, pixel size, and/or defect material and form factor. The patterns will be representative of the design rules for an aggressively-scaled FinFET-type design. With these simulated images and resulting shot noise on the chosen test cases, a basic signal-to-noise framework is developed, which gives us the ability to estimate defect detection probabilities. Additionally, with this infrastructure the effect of detection chain noise and frequency dependent system response can be made, allowing for targeting of the best recipe parameters for MCEBI validation experiments. Ultimately, this study will give insights into how such parameters will impact the design of an MCEBI tool, including the necessary doses for defect detection, estimations of scanning speeds and, ultimately, for achieving the high throughput rates needed for high volume manufacturing.

References:

[1] International Technology Roadmap for Semiconductors, 2013 ed.

[2] Crimmins, T. "Defect metrology challenges at the 11-nm node and beyond", Proc. SPIE 7638, Metrology, Inspection, and Process Control for Microlithography XXIV, 76380H (2010).

[3] Brad Thiel, Michael Lercel, Benjamin Bunday, and Matt Malloy, "Assessing the Viability of Multi-Electron Beam Wafer Inspection for sub-20 nm Defects", Proc. SPIE 9236 (in press) (2014).

[4] J. R. Lowney, A. E. Vladár, and M. T. Postek, "High-accuracy critical-dimension metrology using a scanning electron microscope," Proc. SPIE 2725, pp. 515-526 (1996); J. R. Lowney, "Application of Monte Carlo simulations to critical dimension metrology in a scanning electron microscope," Scanning Microscopy 10, pp. 667-678 (1996).

[5] J. S. Villarrubia and Z. J. Ding, "Sensitivity of SEM width measurements to model assumptions," Proc. SPIE 7272 (2009).

[6] Aron Cepler, Benjamin Bunday, Bradley Thiel, John Villarrubia. "Scanning electron microscopy imaging of ultra-high aspect ratio hole features". Metrology, Inspection, and Process Control for Microlithography XXVI. Proceedings of the SPIE, Volume 8324, pp. 83241N-83241N-14 (2012).

9424-20, Session 4

Investigating SEM metrology effects using a detailed SEM simulation and stochastic resist model

Richard A. Lawson, Clifford L. Henderson, Georgia Institute of Technology (United States)

There have been several simulation studies seeking to understand the effect of stochastic resist effects such as acid diffusion, EUV photoacid generation, and development of resist aggregates on line edge roughness (LER). Likewise, several other simulation studies have sought to understand the effect SEM metrology on the apparent critical dimension due to different sidewall angles, number of linescans, and other parameters. More recently, some simulation studies have attempted to better understand the effect of SEM metrology on the measurement of LER. However, very few of these studies have combined both a stochastic resist model and a detailed SEM simulator capable of measuring LER. This is problematic because it is unclear exactly how the sidewall roughness in a resist or resist model translates into measured LER in a SEM. Some forms of sidewall roughness that resist models might suggest are important contributors to LER may not appear in an SEM. Likewise, detailed SEM models that use "synthetic" sidewall roughness or simple geometry assumptions regarding sidewall angle may not accurately reproduce the complex geometry and various length scales of roughness inherit in real resists. Additionally, SEM simulations that assume smooth sidewalls will incorrectly attribute the broadening of the SEM linescan signal that is due to roughness to the wrong physical origin such as sidewall angle because they have poor representations of real resists. Thus, the solution to these problems is to use both a detailed SEM simulation capable of probing sidewall roughness and stochastic resist model that contains the relevant resist physics. We have previously developed both such types of models.1,2 The resist model was a kinetic Monte Carlo type model developed to simulate design and processing effects on the line edge roughness and patterning of photoresists. The model is capable of simulating most all of the important parameters involved in resist processing from film formation and exposure to development. Figure 1 shows a typical output of a 3D resist line profile. The SEM model is a rigorous Monte Carlo simulation of scanning electron microscopy and uses the differential Mott cross section to compute elastic scattering, while inelastic scattering and secondary electron generation are handled using dielectric function theory. The model can calculate the electron scattering for any arbitrary three-dimensional geometry. Figure 2 shows a comparison between an experimentally measured SEM image and an SEM image generated by the SEM model using the output of the resist model. In this paper, we examine the effect of various resist and exposure parameters such as aerial image contrast and diffusion length on the apparent LER in the SEM in relation to the actual sidewall roughness. We also compare the SEM output of a more realistic resist profile to many of simplified geometric assumptions commonly used in SEM simulations such as smooth, angled sidewalls and synthetic roughness.

9424-21, Session 5

Effect of wafer geometry on chucking in advanced lithography processes

Kevin T. Turner, Univ. of Pennsylvania (United States); Jaydeep K. Sinha, KLA-Tencor Corp. (United States)

Wafer flatness during exposure in modern lithography tools is critical and is

becoming more important as feature sizes in devices shrink. While chucks are used to support and flatten the wafer during exposure, it is essential that wafer geometry be controlled as well. Thickness variations of the wafer and high frequency wafer shape components can lead to poor flatness of the chucked wafer and ultimately patterning problems such as defocus errors. The objective of this work is to investigate approaches for setting control strategies for the process to reduce and control spatial frequencies that can cause chuckability issues on lithography scanners. While advanced metrology tools for measuring wafer geometry exist, establishing the limits of acceptable wafer shape requires an understanding of the chucking and patterning process. In this paper, we will discuss: (1) acceptable limits of wafer shape that permit complete chucking to be achieved, and (2) how residual stresses in patterned films can induce high spatial frequency shape components that can prevent complete chucking.

Specifically, we use analytical and computational mechanics models to establish acceptable levels of wafer shape as a function of spatial wavelength. The results show that wafer shape components with wavelengths of less than 10 mm are most critical in chucking. We examine different filtering approaches and metrics for identifying particular wafer geometry features that will prevent complete chucking. We demonstrate the use of these strategies through experimental measurements. In the second part of the work, we investigate how wafer processing, notably the deposition and patterning of stressed films, can induce high frequency wafer geometry components that lead to flatness problems during exposure. These process-induced wafer geometry changes are more likely to cause chucking problems than the bare wafer geometry, thus there is a critical need to understand the origins of such wafer geometry variations. Both of these complementary studies will aid in establishing metrology requirements for advanced lithography processes. In addition the fundamental understanding developed here may also have applicability in assessing the role of high spatial frequency wafer geometry components in other processes where wafers are mechanically flattened during processing, such as chemical mechanical polishing.

9424-22, Session 5

Improvement of process control using wafer geometry for enhanced manufacturability of advanced semiconductor devices

Honggoo Lee, Jongsu Lee, Sang Min Kim, Changhwan Lee, Sangjun Han, Myoung Soo Kim, Wontaik Kwon, Sung-Ki Park, SK Hynix, Inc. (Korea, Republic of); Pradeep Vukkadala, KLA-Tencor Corp. (United States); Amartya Awasthi, KLA-Tencor Corp (India); J. H. Kim, Sathish Veeraraghavan, KLA-Tencor Corp. (United States); DongSub Choi, KLA-Tencor Korea (Korea, Republic of); Kevin Huang, Prasanna Dighe, KLA-Tencor Corp. (United States); Cheouljung Lee, KLA-Tencor Korea (Korea, Republic of); Soham Dey, Jaydeep K. Sinha, KLA-Tencor Corp. (United States)

Aggressive advancements in semiconductor technology have resulted in integrated chip (IC) manufacturing capability at sub-20nm half-pitch nodes. With this, lithography overlay error budgets are becoming increasingly stringent. The delay in EUV lithography readiness for high volume manufacturing (HVM) and the need for multiple-patterning lithography with 193i technology has further amplified the overlay issue. Thus there exists a need for technologies that can improve overlay errors in HVM. The traditional method for reducing overlay errors predominantly focused on improving lithography scanner printability performance. However, processes outside of the lithography sector known as process-induced overlay errors can contribute significantly to the total overlay at the current requirements. Monitoring and characterizing process-induced overlay has become critical for advanced node patterning. Recently a relatively new technique for overlay control that uses high-resolution wafer geometry measurements has gained significance.

In this work we present the implementation of this technique in an IC fabrication environment to monitor wafer geometry changes induced across several points in the process flow, of multiple product layers with critical overlay performance requirement. Several production wafer lots were measured and analyzed on a patterned wafer geometry tool. Changes induced in wafer geometry (by the combination of all process steps between metrology points) were related to down-stream overlay error contribution using the analytical in-plane distortion (IPD) calculation model. Through this segmentation, process steps that are major offenders to down-stream overlay were identified. Subsequent process optimization was then isolated to those process steps where maximum benefit might be realized.

Several process steps were thus identified for optimization including PECVD, ALD, and RTA process tools. As a validation test IPD induced by the PECVD step was compared with measured overlay residuals. A high correlation was observed thus indicating that the process step contributes significantly to down-stream overlay errors. In addition to high magnitude IPD, the process step also induced significant wafer-to-wafer IPD variation. This was caused by differences in processing that exists between different stations within the process tool. Root-cause for the within-wafer and wafer-to-wafer variation was further investigated using local shape curvature changes – local curvature is obtained using the same metrology technique. Full-wafer curvature maps of wafers processed in different stations of a Metal Hard-Mask ALD tool revealed the presence of stress/thickness variation signatures in the film-stack that were station dependent. A detailed analysis on station/chamber induced process signatures was performed. Differences in process signatures induced by different tool vendors were also analyzed. In multiple instances it was possible to tweak process parameters such as gas flow rate, machine power, temperate, etc and reduce stress in the wafer. These results are also presented in this paper. We conclude that process control using wafer geometry monitoring could have substantial impact on improving the manufacturability of advanced node devices.

9424-23, Session 5

Lithography overlay control improvement using patterned wafer geometry for sub-22nm technology nodes

Jaydeep K. Sinha, KLA-Tencor Corp. (United States); Joel D. Peterson, Gary Rusk, Micron Technology, Inc. (United States); Sathish Veeraraghavan, Kevin Huang, Telly S. Koffas, KLA-Tencor Corp. (United States); Greg Gray, KLA-Tencor Idaho (United States)

The semiconductor industry continues to push the limits of immersion lithography through multiple patterning techniques for printing features with critical dimensions of 20 nm and below. As a result overlay has become one of the critical lithography control parameters impacting device performance and has stringent budget for yielding at smaller half pitch nodes. Overlay error has several sources including intrinsic scanner performance, lens aberration, mask error, and process induced wafer geometry effect. Lithographers have developed both linear and higher order models to successfully compensate for the static fingerprints from different sources of errors. To further compensate for some of the unique process dependent static signature lithographers have also developed complex feedback models such as higher order process corrections (HOPC), and corrections per exposure (CPE). The overlay residuals after these corrections reflect the process variation in the fab which can be observed from lot to lot (L2L) and wafer to wafer (W2W).

A primary source of these variations is wafer geometry changes induced by wafer processing between two litho-steps. From past research it has been theoretically proven that deposition of a single film with axi-symmetric non-linear residual film stress on a silicon substrate causes overlay errors. This theory has been experimentally verified for a controlled experiment of a single nitride film on silicon substrate. In this paper, the fundamental relationship between residual overlay and geometry induced overlay by several processes between two litho-steps is proven experimentally. For litho-steps with large geometry induced overlay errors, the feasibility of

feed forward to reduce the L2L variations and W2W variation are also addressed in this paper.

To illustrate the feasibility of the feed forward concept, two critical FEOL litho-steps along the 3D NAND process flow which exhibited large L2L and W2W overlay variations were chosen for the study. The geometry of the patterned wafer was measured at the two litho-steps and the geometry induced overlay (GIO) was computed. The high correlation between GIO and measured overlay (R2 ~0.9) shows that geometry induced overlay was the primary cause of large overlay variations observed. The test lot was reworked by feeding forward the corrections from GIO. From the experimental results it was observed that there was ~ 25% improvement in overlay for the entire lot. Moreover, improvements in both static as well as non-static components of overlay induced by geometry were observed. The successful demonstration of the geometry induced overlay feed forward concept opens a new methodology to tackle overlay challenges for advanced technology nodes with significant process induced overlay and tight overlay budgets.

9424-24, Session 6

Demonstration of parallel scanning probe microscope for high-throughput metrology and inspection

Hamed Sadeghian, Rodolf W. Herfst, Jasper Winters, Tom Bijnagte, Bert Dekker, Alexander Eigenraam, Ramon Rijnbeek, Nicole Nulkes, TNO (Netherlands)

With the device dimensions moving towards the 1X node and below, the semiconductor industry is rapidly approaching the point where existing metrology, inspection and review tools face huge challenges in terms of resolution, the ability to resolve 3D and the throughput.

Scanning probe microscope (SPM) and specifically atomic force microscope (AFM), due to the advantages of sub-nanometer resolution and the ability of true 3D scanning are considered as alternative technologies for CD-metrology, defect inspection and review of 1X node and below.

In order to meet the increasing demand for resolution and throughput of CD-metrology and defect inspection and review, we have previously introduced the parallel SPM concept [1], consisting of parallel operation of many miniaturized SPMs [2] on a 450 mm wafer. In this paper we will present the proof of principle of the ultimate parallelization as shown in Figure 3.

Figure 1 illustrates the parallel system. Last year we have shown the proof of principle and the experimental results of one single unit consists of ultra-fast miniature AFM head and an accurate, fast positioning unit to position scan head with respect to the wafer. The system was capable of scanning areas on a wafer as large as 100?100 μm2 in several tens of seconds. The scan head showed a measurement bandwidth of 50 KHz, and a resolution as low as 0.1 nm. The closed loop positioning unit results in an positioning accuracy better than 100 nm.

Figure 2 shows the demonstration of one single unit of miniature AFM and the positioning unit to be parallelized in the final system.

In the next step we have designed and realized the final parallel AFM system to experimentally show the feasibility of parallel scanning on both wafer and mask. The system consists of 4 parallel miniature scan heads and positioning units that simultaneously scan a wafer or a mask. The system can then be scaled up to more than 40 parallel units. The user can insert several locations on a mask and wafer to be scanned. figure 3 shows the 4 parallel AFM system. The defect inspection and review is done in two steps; first the coarse scanning to quickly detect the defects or particles as small as 5 nm and then the fine scanning to image the true 3D image of the defect or the particle. The results of the scanning an EUV mask and reviewing a particle is shown in figure 4.

In conclusion, we show the ultimate proof of principle of parallel AFM equipment for metrology and inspection. With 4 parallel AFMs system we show the feasibility of all technical challenges involved. The system can now be scaled up for the ultimate required throughput by parallelizing more than 40 scan heads.

9424-25, Session 6

Self-actuated, self-sensing cantilever for fast CD measurement

Ahmad Ahmad, Tzvetan Ivanov, Technische Univ. Ilmenau (Germany); Alexander Reum, nano analytik GmbH (Germany); Elshad Guliyev, Tihomir Angelov, Andreas Schuh, Marcus Kaestner, Technische Univ. Ilmenau (Germany); Ivaylo Atanasov, Manuel Hofer, Mathias Holz, nano analytik GmbH (Germany); Ivo W. Rangelow, Technische Univ. Ilmenau (Germany)

The fundamental measurement issues in microelectronic manufacturing comprise the determination of lithographic features such as its length, pitch, width, height, shape, surface morphology, line edge roughness and layer thickness. For this, Atomic Force Microscopes (AFMs) offer a non-destructive and non-vacuum metrology method. Conventional AFM cantilevers are made out of silicon or silicon compounds. The tip displacement is usually detected optically based on laser deflection of the beam. The maximum imaging speed of cantilevers is determined by the spring constant, the effective mass, the cantilever damping induced by the surrounding medium (e.g. air or water) and the surface.

The conventional optical lever detection technique involves optical components and its precise mechanical alignment. An additional technical limit is the weight of the optical system, in case a top-scanner is used in high speed and high precision metrology [1]. Here, we have achieved significant improvement employing integrated 2DEG as piezoresistive deflection read-out. The performance of such cantilevers with respect to deflection sensitivity and temperature drift compensation has been further enhanced by using an integrated Wheatstone bridge configuration [2]. The thermo-mechanical noise floor of our cantilevers is estimated to 89 fm/Hz$^{1/2}$ [3]. With this technique today, the overall noise floor of the piezoresistive detection scheme is typically in the range of 10-3 Å/Hz$^{1/2}$ to 10-4 Å/Hz$^{1/2}$.

In 1996 we proposed the integration of bi-material thermal actuators onto the self-sensing SPM-cantilevers. Due to the integration of both, the scan speed of the AFM could be increased by an order of magnitude over the standard AFM [4]. Self-actuated, piezoresistive cantilevers are usually manufactured using silicon-on-insulator (SOI) wafers in combination with standard M(N)EMS processes (Fig.1) [5].

Our AFM tool offers great versatility and ease of use. For highest AFM productivity, the cantilevers are manually exchangeable in less than 10 sec., a fast approach technology allows a tip-to-sample approach time of approx. 5 sec. from more than 2 mm above the sample surface and an AFM imaging time of 20 to 40 sec. Scanning speeds of 100 l/sec. (10 x 10 μm2 scan area, 50 nm topography height and 256 pixels/line) are routinely achieved using a novel adaptive scan speed control (ASSC) method (Fig. 2) [6]. In this article we will discuss the current state of development in metrology with self-actuated, piezoresistive cantilevers for measuring critical dimensions and describe our work in advancing this technique as a new promising technology.

9424-26, Session 6

High-speed AFM for 1x node metrology and inspection: Does it damage the features?

Hamed Sadeghian, Teun C. van den Dool, TNO (Netherlands); Yoram Uziel, Ron Bar Or, Applied Materials, Ltd. (Israel)

This paper aims at unraveling the mystery of damage in high speed AFMs for 1X node and below. With the device dimensions moving towards the 1X node and below, the semiconductor industry is rapidly approaching the point where existing metrology, inspection and review tools face huge challenges in terms of resolution, the ability to resolve 3D and the throughput.

Scanning probe microscope (SPM) and specifically atomic force microscope (AFM), due to the advantages of sub-nanometer resolution and the ability of true 3D scanning are considered as alternative technologies for metrology, inspection and review of 1X node and below. Recent developments have led to substantially increase of the speed of the measurement, hence, the process throughput [1, 2]. Despite the advantages of AFM, substrate or tip damage can occur because of tip-sample interactions. Since AFM is a contact or semi-contact method (depends on the chosen scanning mode), strong interaction forces between the tip and the features on a wafer exist. Due to nanometer size of the tip the indentation area is very small and results in very high Hertzian stresses. The contact stress depends on numerous parameters including scanning parameters (i.e. amplitude of vibration, speed of the measurement and gains of the feedback controller), sample and AFM cantilever properties. Therefore, if appropriate parameters are not selected the contact stress exceeds one of the failure stresses and therefore damage can occur. Damage can present in forms of fracture, indentation, plastic deformation, buckling and collapsing of the features, tip wear, etc.

In this paper, we critically asses the important issue of damage in high speed AFM for metrology and inspection of semiconductor wafers. The issue of damage in three major scanning modes (contact mode, tapping mode/non-contact mode, peak force tapping mode) is described to show which mode for which applications and which condition is damaging.

The effects of all important scanning parameters on resulting damage are taken into account for materials such as silicon, photoresists and low K materials.

Finally, we introduce a method for selecting appropriate scanning conditions for several use cases (FinFET, patterned photoresist, HAR structures) that voids exceeding a critical contact stress to minimize the sample damage.

In conclusion, we show using our analysis to select parameters that exceed the target contact stress indeed leads to significant damage. This method provides AFM users for metrology with a better understanding of contact stresses and enables selection of AFM cantilevers and experimental parameters that prevents the sample damage.

9424-27, Session 6

Multiple height calibration reference for nano-metrology

Marc Christophersen, Bernard F. Phlips, Andrew J. Boudreau, Michael K. Yetzbacher, U.S. Naval Research Lab. (United States)

Modern nano-metrology instruments require calibration references with nanometer accuracy in x, y, and z directions. A common problem is the accurate calibration in the z direction (height). For example, it is generally not difficult to obtain accurate x- and y- calibration references for an Atomic Force Microscope (AFM). It is, however, much more difficult to obtain accurate z-axis results. It is difficult to control z-axis piezo dynamics because during scanning in the xy-plane the x-and y-axes move at a constant rate whiles the z axis does not. Furthermore due to the high cost of producing calibration standards, the microscope is often calibrated at only one height. However, if the relationship between the measured z height and the actual z height is not linear, then the height measurements will not be correct. In this paper, we will present a method for the fabrication of calibration references with: (i) sub-6 nm features and (ii) multiple step heights on one reference, allowing for better calibration of the non-linearity in the z direction.

Traditionally, the cost driver for multiple-height references has been the use of multiple lithography and etch/deposition steps. One can use so-called “combinatorial etching”, which reduces the number of lithography steps to log2(N) where N is the number of distinct levels of material. However, significant yield loss results from the several lithography steps required in this process. We introduce a new digital etching technique that allows for the creation of an arbitrary number of distinct levels with a single grayscale lithography technique followed by a single RIE (reactive ion etch) step. Our technique has been used for the fabrication of distinct levels of 0.2 nm rms roughness with a controlled < 6 nm features. This technique has been used to fabricate a staircase reference with more than 120 distinct steps. We will present multiple AFM scans/images and optical profilometer scans from multiple calibration references in addition to the fabrication method. The individual step height can be varied over a wide range from a few nanometers to hundreds of nanometers, even on the same reference. AFM scans clearly show a roughness of less than 2 Angstroms for the top surfaces of the reference heights. Furthermore, the method is fully compatible with semiconductor processing and can be done on full wafers and on any substrate such as Si, quartz, etc.

9424-28, Session 6

Development of a comprehensive metrology software platform dedicated to dimensional measurements of CD atomic force microscopy tips

Johann Foucher, Pollen Technology (France); Sebastian W. Schmidt, nanotools GmbH (Germany); Aurelien Labrosse, Alexandre Derville, Pollen Technology (France); Sandra Bos, CEA-LETI (France); Sebastian Schade, Bernd Irmer, nanotools GmbH (Germany)

The dimensional scaling in IC manufacturing strongly drives the demands on CD metrology techniques and their measurement uncertainties. With the introduction of hybrid metrology, i.e. the approach to control process steps and parameters on the basis of complementary CD metrology methodologies, atomic force microscopy (AFM) has become more and more relevant as reference monitoring tool.

Over the last years, extensive improvements have been made on AFM tool stability and its abilities to serve as advanced 3D monitoring system. However, its applicability for CD features is still crucially determined by the AFM tip shape and dimensions.

The vital need for AFM tips applicable to critical device features thus requires highly accurate and precisely fabricated tip dimensions. With electron beam induced processing (EBIP) the current dimensional limitations given by state-of-the-art silicon etch technologies can be overcome. The reduction in tip dimensions, however, is accompanied by challenging demands on process control, quality inspection, and data extraction. With the ability to best meet these requirements, measurements are usually performed with dedicated scanning electron microscopy (SEM) tools allowing for optimized imaging at minimized contamination. However, whatever improvement is made on the SEM regarding precision, real dimensions on the nanometer level extracted from free-standing 3D structures are hardly to obtain directly since its pretended accuracy remains ambiguous. As a consequence, only reference measurements, e.g. CD-AFM measurements, are able to fill the gap in order to reach the accuracy needed for an acceptable measurement uncertainty.

In this paper, we will present our most recent approach on the extraction of reliable tip dimensions from SEM in order to answer future requirements on AFM tips. We demonstrate the capabilities of a newly developed, fully automatic analysis software based on advanced SEM image modelling and user a-priori knowledge integration in SEM image analysis algorithm. The impact of such breakthrough technology will be shown as a function of its stability and robustness by varying tip shape, imaging settings, and SEM setup parameters. The extracted values are compared to data yielded from commonly used analysis approaches, and directly related to reference CD-AFM measurements. We will discuss the prospective challenges accompanied with shrinking tip dimensions and the potential of a comprehensive data fusion approach.

9424-29, Session 7

Optical CD metrology for directed self-assembly assisted contact hole shrink process

Dhairya J. Dixit, Alain C. Diebold, SUNY College of Nanoscale Science and Engineering (United States); Erik R. Hosler, Moshe E. Preil, GLOBALFOUNDRIES Inc. (United States); Joseph Race, Nick Keller, Nanometrics Inc. (United States); Jun Sung Chun, Michael O'Sullivan, M. Warren Montgomery, SUNY College of Nanoscale Science and Engineering (United States)

Scatterometry based on Mueller matrix spectroscopic ellipsometry (MMSE) is used for optical characterization of directed self assembly (DSA) based contact hole structures for the phase-separated polystyrene-b-polymethylmethacrylate (PS-b-PMMA) before and after etch. The optical signature of Mueller matrix (MM) elements have complex dependence on the topography and orientation of the structures, depolarization, and optical properties of the materials associated with the grating and any layers underneath the structure. The symmetry properties associated with MM elements provide an excellent means of measuring and understanding the topography of the periodic nanostructures. A forward problem approach of scatterometry or optical model based simulations is used to investigate MMSE sensitivity to different DSA based contact hole structures and its limits to characterize DSA induced defects such as hole placement inaccuracy, missing vias, profile inaccuracy of the PMMA cylinder, and process induced defects such as presence of residual PMMA layer after etching. In addition, effect of these defects on anisotropy and depolarization values is evaluated.

9424-30, Session 7

Metrology of DSA process using TEM tomography

Tamar Segal-Peretz, Nestor J. Zaluzec, Argonne National Lab. (United States); Jiaxing Ren, The Univ. of Chicago (United States); Mahua Biswas, Argonne National Lab. (United States); Jonathan Winterstein, Alexander J. Liddle, National Institute of Standards and Technology (United States); Jeffery W. Elam, Argonne National Lab. (United States); Paul F. Nealey, The Univ. of Chicago (United States)

Directed self-assembly of block copolymers (DSA) has been explored extensively for patterning periodic nanostructures for transistors and bit-pattern media manufacturing with tremendous progress in last few years. Nonetheless, DSA still lacks accurate meteorology tools and in particular metrology of the three dimensional structure of block copolymer (BCP) films. Here we use high resolution scanning transmission electron microscopy (STEM) tomography to resolve the three dimensional structure of block copolymer films. Using a series of tilted STEM images the 3D structure can be reconstructed and examined with nanometric resolution. Sequential infiltration synthesis (SIS), an atomic layer deposition technique which enables block-selective incorporation of inorganic composites within the polar blocks, was used to enhance the contrast between the BCP blocks and its stability under the electron beam.

STEM tomography was used to decipher the three dimensional structure of lamellae-forming, cylinder-forming, and sphere-forming polystyrene-block-poly(methyl methacrylate) (PS-b-PMMA) films and to image the 3D structure of a single BCP domain as well as the structure of single defect. In addition, since the BCP film is characterized after the SIS process, the method characterizes the exact structure that will be transferred to the underlying layer.

We show that by using STEM tomography detailed 3D characterization of DSA films can be obtained, leading to understanding of self-assembly of BCP in ways that were not possible before.

9424-31, Session 7

Line-edge roughness on directed self-assembly: impact of process conditions

Vijaya-Kumar Murugesan Kuppuswamy, IMEC (Belgium) and Katholieke Univ. Leuven (Belgium); Lance D. Williamson, IMEC (Belgium) and The Univ. of Chicago (United States); Hari Pathangi, IMEC (Belgium); Paul F. Nealey, The Univ. of Chicago (United States); Roel Gronheid, IMEC (Belgium); Guanyang Lin, Yi Cao, AZ Electronic Materials USA Corp. (United States)

Directed Self Assembly (DSA) lithography has recently gained significant attention as potential technology for the fabrication of integrated circuit features at <20nm scale. One of the main challenges for implementation of DSA lithography is to control the block copolymer domain alignment with respect to guide pattern. In a chemo-epitaxy line-space process flow for DSA, minor loss of alignment will result in roughness before dislocation defects are formed. The sidewall roughness is critical, since it induces local deviations from designed dimension as well as placement errors. Consequently, roughness leads to degradation of device performance. For this reason, the issue of roughness has attracted a lot of interest during the last two decades in semiconductor industry, concerning mainly the effects of gate roughness on transistor performance. This work has mainly focused on roughness after projection lithography and subsequent pattern transfer. So it is important to study the Line Edge Roughness (LER) and Line Width Roughness (LWR) in the DSA process. The study the LER and LWR as a function of the wavelength of the roughness may give insight into how roughness is impacted by the various processing steps. In addition, the different frequencies of roughness can affect device performance in different ways1.

In this work, we study the transfer function of line edge roughness at different processing steps in the LiNe flow for 14nm line/space patterning, illustrated in Figure 1. We also study the impact of interaction strength and roughness of the guide stripe on the LER/LWR of the DSA pattern. To study the impact of the guide stripe on the LER, it is measured individually for lines on the top of the guided stripe and lines in between the guided stripe. In addition, impact of guide stripe CD and pitch are also studied

The baseline LER and LWR analysis at different process stages after DSA of block copolymer (BCP) and PMMA removal shows same LER and LWR, indicating correlated roughness (figure 2&3). The full frequency content of the LER is evaluated by using power spectrum. In addition, impact of BCP formulation, neutral layer composition, Molecular weight and anealing conditions on LER and LWR are studied. Further, mechanisms for the explanation of the experimental findings are also discussed and investigated.

[1]Y.Chuang et al, Advanced Functional Materials, vol. 23, pp.173-183, 2013.

[2] Liu, C. et al, "Macromolecules 44, 1876-1885 (2011).

9424-32, Session 8

Improvements of traceability and tool matching in scatterometry

Bernd Bodermann, Physikalisch-Technische Bundesanstalt (Germany); Bernd Löchel, Helmholtz-Zentrum Berlin für Materialien und Energie GmbH (Germany); Frank Scholze, Hermann A. Gross, Jan Wernecke, Johannes Endres, Physikalisch-Technische Bundesanstalt (Germany); Jürgen Probst, Helmholtz-Zentrum Berlin für Materialien und Energie GmbH (Germany); Lars

K. Nielsen, Danish Fundamental Metrology Institut (Denmark); Matthias Wurm, Physikalisch-Technische Bundesanstalt (Germany); Mark-Alexander Henn, Physikalisch-Technische Bundesanstalt (Germany) and National Institute of Standards and Technology (United States); Max Schoengen, Michael Krumrey, Physikalisch-Technische Bundesanstalt (Germany); Morten H. Madsen, Dansk Fundamental Metrologi (Denmark); Nitish Kumar, Technische Univ. Delft (Netherlands) and ASML Netherlands B.V. (Netherlands); H. Paul Urbach, Technische Univ. Delft (Netherlands); Peter Petrik, Technische Univ. Delft (Netherlands) and Hungarian Academy of Sciences (Hungary); Petr Klapetek, Czech Metrology Institute (Czech Republic); Poul-Eric Hansen, Danish Fundamental Metrology Institut (Denmark); Sebastian Heidenreich, Physikalisch-Technische Bundesanstalt (Germany); Sven Burger, JCMwave GmbH (Germany); Victor Soltwisch, Physikalisch-Technische Bundesanstalt (Germany)

Recently a joint research project “Scatterometry” has been performed within the European Metrology Research Programme [1] by several European partners. This project aimed to establish scatterometry as traceable and absolute metrological method for dimensional measurements and in particular for CD metrology. To reach this goal an in-depth understanding of the measurement process and a quantification of experimental and numerical limitations as well as the approximations, which usually have to be applied for efficiency reasons, is required.

For this purpose we investigated both experimentally and by numerical simulations the influences of different tool or sample specific limitations like the plane wave approximation, the influence of a limited interaction area and of line edge roughness, to enable a significant reduction of possible systematic measurement deviations and to enable reliable measurement uncertainty budgets for scatterometric measurements. Additionally different novel promising approaches such as EUV scatterometry, Grazing Incidence Small Angle X-ray Scattering (GISAXS), Mueller polarimetry and coherent scanning focussed beam scatterometry (CSFS) have been developed, tested and compared with conventional methods such as goniometric scatterometry and spectroscopic ellipsometry. The comparison of these different approaches supported by AFM and SEM reference measurements enables and improves the identification of possible systematic measurement errors.

Systematic measurement comparisons on different 1D gratings, both on Si gratings and on a COG photomask have been performed. We present exemplarily results of these comparisons and discuss the performance and the advantages and disadvantages of the different methods.

Additionally sophisticated modelling approaches and data analysis methods for scatterometry, such as advanced modelling of line edge roughness effects, rigorous and fast computation of sensitivities and linear approximations for a maximum likelihood approach or combined data analysis have been developed and investigated and will be discussed.

Finally, to support the evaluation and testing of different scatterometry-based metrology tools and the tool matching between different optical CD tools as well as the matching with CD-SEM and CD-AFM tools, we worked on the realisation of suitable scatterometry reference standard samples. Two different standard samples based either on Si or on Si3N4 have been developed and tested. The etched gratings currently have periods down to 50 nm and contain areas of reduced density to enable AFM measurements for comparison. We present first characterisations of these samples. Structure details like line edge and line width roughness and edge angles have been measured measured by AFM, optical and EUV scatterometry as well as GISAXS and spectroscopic ellipsometry. We report on the status of these developments and discuss the final design and aimed specifications of these standard samples and of possible future extensions.

[1] http://www.ptb.de/emrp/ind17.html, http://www.euramet.org

9424-33, Session 8

Improved scatterometry time-to-solution using virtual reference

Alok Vaid, GLOBALFOUNDRIES Inc. (United States); Gilad Wainreb, Yinon Katz, Nova Measuring Instruments Ltd. (Israel); Cornel Bozdog, Matthew J. Sendelbach, Nova Measuring Instruments Inc. (United States)

Advanced processes and integration schemes (such as multi-patterning and FinFET) require precise detection and control of intricate profile details on the complex structures such as sidewall angle, spacer widths, spacer pull-down, epitaxial proximity, footing/undercut, overfill/underfill, etc. Scatterometry is the primary non-destructive method to address such detailed requirements for in-line profile metrology.

Scatterometry is a model-based technique, where the calculated optical response from a geometrical / optical model is fitted to a measured optical signal and the most probable profile is extracted. In order to mitigate the risk of using an imperfect model (with wrong details and degrees of freedom, possibly leading to inaccuracies or instability), best industry practice is to qualify scatterometry models prior to in-line implementation at each process step against different possible process modifications using costly and time-consuming, sometimes destructive cross-sectional imaging as reference. This practice is not only expensive for the user, but also delays scatterometry solutions from being deployed and used immediately at the onset of process development.

This work is aimed to significantly reduce (or eliminate entirely) the need for reference metrology. To enable this we developed a novel methodology whereby we use spectral information already measured during scatterometry, in order to predict “virtual” reference data.

One element of the new methodology is the measured spectra, which optically encodes the information about the scatterometry structures measured. Another element is flexibility of geometrical / optical model where the “real” structure is implicitly included as one of the possible modifications of the model. The “glue” lies in the algorithm used to identify the “right” virtual reference data. Examining the geometry in different ways, the flexible model, and its relationship to the spectral response, the algorithm is automatically adapted to the specific application.

We developed and later qualified this methodology on several key applications from the 20 and 14nm node (in the area of FinFET epitaxy and deposition, on 2D and 3D structures). For each application the algorithm’s predictive methodology is first validated theoretically; next the algorithm is applied to measured data, and a set of virtual reference results is extracted. This data is then used as “the reference” for scatterometry model setup instead of the “real” reference data. The success of the method is measured by comparing the performance of recipe developed solely based on the virtual reference (no real reference) to the one that uses full, real reference.

We find that the performance of the solution developed using the proposed methodology of virtual reference is indeed similar to the performance of solution obtained using real reference data. This result is significant, as takes the first step towards independent usage of scatterometry without waiting for complex recipe validation. Scatterometry development without reference can result in significant time-to-solution improvement and cost savings for those using the best practice of third-party reference validation.

We are currently developing applications in Fab production environment using virtual reference, and continue to monitor its match to real reference data, while gradually reducing the amount of external reference in a phased implementation approach.

9424-34, Session 8

Data refinement for robust solution to the inverse problem in optical scatterometry

Jinlong Zhu, Hao Jiang, Chuanwei Zhang, Xiuguo Chen, Shiyuan Liu, Huazhong Univ. of Science and Technology (China)

Optical scatterometry, also referred to as optical critical dimension (OCD) metrology, has been widely used in the process control of 2D and 3D microelectronics structures due to its low cost, high throughput, and minimal sample damage. It is essentially a model-based technique, whose success highly relies on the accurate and precise solution to an ill-posed inverse problem. Currently, the inverse problem is usually formulated as a problem of least square (LSQ) fitting or maximum likelihood (ML) estimation, with the objective of finding the profile parameters whose calculated signature can best match the measured one. Moreover, the precision, or approximate 95% confidence intervals of the extracted profile parameters, is obtained by calculating the square root of the main diagonal entries of the covariance matrix of the extracted parameters. The above procedures for parameters extraction and 95% confidence intervals estimation imply a statistical hypothesis that the measurement errors in the measured signature are normally distributed with zero mean. However, in an actual measurement system, normality is only a myth. The superimposed effect from different error sources such as the power fluctuation of the incident beam, the imperfect modeling, the spectral resolution of the monochromator, and the collimation of the light source will bias the actual statistical property of measurement errors from normal distribution. These abnormally distributed measurement errors will significantly affect the estimation of parameters as well as the 95% confidence intervals.

In this work, we propose to add an additional data refinement (DR) procedure before the LSQ fitting or ML estimation to detect those data points that correspond to the relatively large abnormal measurement errors from the full wavelength range. The DR procedure is conducted by performing an additional robust regression procedure at the end of each iteration of the Gauss-Newton method, and then those data points corresponding to the large residuals are treated as the ones containing the relatively large abnormally distributed measurement errors. By rejecting those data points corresponding to the large errors and leave the rest "good" ones for the LSQ fitting or ML estimation, the more accurate parameters as well as the more reliable 95% confidence intervals can be achieved.

Figure 1 presents the measurement setup of a dual-rotating compensator Mueller matrix ellipsometer (DRC-MME) as well as the scanning electron microscope (SEM) cross-section image of a trapezoidal etched Si grating. We can obtain the full Mueller matrix elements of the Si grating under measurement with the DRC-MME setting. Figure 2 depicts the weighted fitting differences of the measured and the best matched Mueller matrix elements. It is well known that if the measurement errors are normally distributed, the weighted measurement errors obtained by dividing the measurement errors by the weighted factors are then following standard normal distribution and fall into the range of -3 ~ 3 with the probability of 99.7%. However, as can be seen in Fig. 2, many large data points are out of the range -3 ~ 3. To make a comparison, we use the proposed DR procedure to detect those data points that correspond to large measurement errors, and then extract an optimal set of parameters with the rest "good" data points. Table 1 displays the extracted results with the DR procedure and that without DR procedure and by SEM We can find that the results obtained with the DR procedure is closer to the SEM measured one than that of the traditional LSQ fitting without the DR procedure. The above measurements are conducted at 45° incident angle and 10° azimuthal angle, and the wavelength range is from 200 nm to 800 nm.

9424-35, Session 8

Method to simulate light scattering from complex 3D structures

Sven Burger, Lin Zschiedrich, Jan Pomplun, Frank Schmidt, JCMwave GmbH (Germany)

The availability of methods to accurately simulate light scattering from complex 3D structures is a challenge for the semiconductor industry.

It is of importance for both, computational metrology and lithography simulation [1].

We develop finite-element methods for electromagnetic field simulations.

Performance of these methods has been demonstrated for lithography and metrology applications [2-4].

In this contribution we comment on new methods for fast and accurate simulations of 3D structures.

This includes both, accurate geometry meshing adapted to small, non-rectangular, and rounded features and an hp-adaptive finite-element kernel.

[1] International Technology Roadmap for Semiconductors (2013)

[2] J. K. Tyminski, et al. Proc. SPIE 8683, 86831C (2013)

[3] S. Burger, et al. Proc. SPIE 8166, 81661Q (2011)

[4] B. Kleemann, et al. Proc. SPIE 8083, 808309 (2011)

9424-36, Session 8

Scatterometry-based metrology for the 14nm node double-patterning lithography

Damien Carau, STMicroelectronics (France) and LTM CNRS (France); Régis Bouyssou, Julien Ducoté, Florent Dettoni, Christophe Dezauzier, Alain Ostrovsky, Bertrand Le Gratiet, STMicroelectronics (France); Maxime Besacier, LTM CNRS (France); Cécile Gourgon, LTM CNRS (France)

Critical dimension and overlay measurements have become a key challenge in microelectronics process control, and the weight of metrology in the success of a patterning technique is increasing. For the 14 nm node, the limit of the scanner resolution can be overcome by the double patterning technique, which requires a maximum overlay error between the two reticles of few units of nanometers. In a simple patterning case, critical dimension and overlay are treated separately, but such an approach is much more complex in double patterning context, because space dimensions and overlay are no longer independent. For the first metal level, key parameters are the widths of lines and spaces after final etch. The challenge is to anticipate these dimensions at the second lithography step in order to enable a rework if necessary.

This paper shows a sensitivity study demonstrating that scatterometry is able to measure simultaneously critical dimensions of upper and lower gratings in a device-like target by fitting spectra of several Mueller Matrix elements. This aims to measure overlay and critical dimensions in the same target. However, overlay sensitivity is too low compared to those of critical dimensions. This is why only overlay values higher than 5 nm have been measured in a device-like target, whereas the expected precision is 0.25 nm.

Consequently, a feed-forward strategy of overlay data from usual overlay measurements in a dedicated target close to the device-like one is being considered.

These overlay measurements have been performed by diffraction-based overlay and image-based overlay methods. Several targets have been tested for each method and have been ranked according to accuracy and precision criteria. In order to estimate the accuracy of each metrology recipe, a specific wafer with a scanner induced overlay has been processed. As for precision, total measurement uncertainty, including tool-induced shift and dynamic precision, has been estimated for every target.

Another significant concern for overlay measurements is target pattern size. Indeed, grating lines used in diffraction-based or in advanced image-based methods are designed with dimensions that are much higher than critical dimension of the level. As process is optimized for dimensions close to critical dimension, patterns of overlay targets can suffer from asymmetry such as a difference in sidewall angles. This asymmetry can be read as a virtual overlay value by both overlay measurement methods. For the diffraction-based overlay method, a simple simulation code, based on the Rigorous Coupled Wave Analysis, has been written to determine the optimal target configuration in order to minimize the impact of this kind of artifact.

Finally, trench and line width measurements have been compared successfully after lithography and after etch. After etch measurements have been performed by top-view Scanning Electron Microscopy, while after lithography measurements have been done with this scatterometry-based method. These measurements are well correlated, which proves that this approach is ready to be implemented in an industrial process control context.

9424-37, Session 8

Scatterometric analysis of a plasmonic test structure

Samuel O'Mullane, SUNY College of Nanoscale Science and Engineering (United States); Nick Keller, Joseph Race, Nanometrics Inc. (United States); Brian Martinick, Alain C. Diebold, SUNY College of Nanoscale Science and Engineering (United States)

For traditional ellipsometric targets, slightly changing the thickness of a layer or the composition of a material results in a similarly small change in the observed spectra. If structures are designed to allow for plasmonic coupling, slightly varying those same parameters can result in vastly different spectra. This work focusses on inducing localized plasmonic resonances in metallic grating structures allowing for extraordinary sensitivity to parameters such as CD, sidewall angle, and pitch.

Existing metallic grating structures are arrays of long, thin lines of copper often so large that they can be described as one dimensional and infinite with regard to ellipsometry. The typical resolution for ellipsometric CD measurements on these structures ranges from nanometers to Angstroms. Because there is no confining second dimension, localized plasmons cannot be produced for these structures.

The structure we have designed and simulated is a cross-grating structure produced by adding a second metallic grating perpendicular to the original grating. Note that the added pitch and linewidth are an order of magnitude larger than the original parameters. This results in fully localized plasmonic resonances so that CD variation on the order of tens of picometers can be detected through ellipsometric measurements. Other parameters such as pitch-walking, side wall angle, material composition have shown likewise extraordinary results.

Due to the nature of the fabrication process, we will be limited in the parameters that we can vary. Regardless of the produced parameters, our simulations show consistent results over a large portion of the possible parameter space. Though not as rigorously investigated, simulations on normal incidence polarized reflectometry for BEOL use have shown similarly extraordinary enhancement. Compared to existing metallic gratings, the cross-grating has shown a 50x improvement with NIR-OCD.

9424-38, Session 9

Target design optimization for overlay scatterometry to improve on-product overlay

Henk-Jan H. Smilde, Richard J. F. van Haren, Willy van Buel, Xing Lan Liu, Jerome Depre, Jan Beltman, ASML Netherlands B.V. (Netherlands); Florent Dettoni, Julien Ducoté, Christophe Dezauzier, STMicroelectronics (France); Yoann Blancquaert, CEA-LETI (France)

On-product overlay can be improved in several ways. During the last years, emphasis has been given to the actual measurement of overlay by metrology tools. This is not only to accurately determine the overlay performance in a production environment but also to enable accurate corrections for observed fingerprints using feed-forward or feed-back methodologies to further improve the overlay. The correction capabilities depend on the availability of accurate overlay data. The accurate overlay data is required both in time, i.e. inline measurement after wafer exposure to enable fast feedback to APC and future exposures, and in location, enabling higher order corrections based on dense intra-field sampling. The latter requires metrology targets to be available in the product field of e.g. logic devices, and therefore to be small enough to fit within the chip product area.

In this paper, which is the result of common work by ASML and STMicroelectronics, we will specifically elaborate on methods that improve the design of small scatterometry targets in order to optimize the metrology performance. With decreasing size of targets, from a signal response point of view, these can no longer be seen as infinite size targets, and effects caused by target edges have to be taken into account. Theoretical background of the effects caused by mark edges to the read-out in the metrology tool will be presented first. After that, proposed methods to improve the design of marks to minimize the impact of the mark edge effects are discussed. In these improvements, the fact that the Numerical Aperture of the metrology tool itself is large but finite and therefore enables filtering information, will be used. Finally, experimental results will be presented that are achieved using the optimized targets designs on product wafers at STMicroelectronics. Both metrology results (accuracy, reproducibility) as well as on-product overlay performance will be shown.

The outcome of the work can be applied in different ways. In the first place it can be applied to optimize the repeatability and accuracy of the metrology at a given mark size. Secondly, functionality can be added to existing marks within the current mark area (for example asymmetry information or information from multiple layers). And thirdly, the size of overlay metrology marks at equal performance can be further miniaturized to enable intra-field positioning. It is noted that the solution for overlay marks can also be applied to metrology marks in other metrology applications (e.g. focus).

9424-39, Session 9

Overlay improvement by exposure map based mask registration optimization

Irene Shi, Eric Guo, Ming Chen, Max Lu, Gordon Li, Rivan Li, Eric M. J. Tian, Semiconductor Manufacturing International Corp. (China)

Along with the increased miniaturization of semiconductor electronic devices, the design rules of advanced semiconductor devices shrink dramatically. [1] One of the main challenges of lithography step is the layer-to-layer overlay control. Furthermore, DPT (Double Patterning Technology) has been adapted for the advanced technology node like 28nm and 14nm, corresponding overlay budget becomes even tighter. [2][3] After the in-die mask registration (pattern placement) measurement is introduced, with the model analysis of a KLA SOV (sources of variation) tool, it's observed that registration difference between masks is a significant error source of wafer layer-to-layer overlay at 28nm process. [4][5] Mask registration optimization would highly improve wafer overlay performance accordingly. It was reported that a laser based registration control (RegC) process could be applied after the pattern generation or after pellicle mounting and allowed fine tuning of the mask registration. [6]

In this paper we propose a novel method of mask registration correction, which can be applied before mask writing based on mask exposure map, considering the factors of mask chip layout, writing sequence, and pattern density distribution. Our experiment data show if pattern density on the mask keeps at a low level, in-die mask registration residue error in 3sigma could be always under 5nm whatever blank type and related writer POSCOR (position correction) file was applied; it proves random error induced by material or equipment would occupy relatively fixed error budget as an error source of mask registration. On the real production, comparing the mask registration difference through critical production layers, it could be revealed that registration residue error of line space layers with higher pattern density is always much larger than the one of contact hole layers with lower pattern density. Additionally, the mask registration difference between layers with similar pattern density could also achieve under 5nm performance. We assume mask registration excluding random error is mostly induced by charge accumulation during mask writing, which may be calculated from surrounding exposed pattern density. Multi-loading test mask registration result shows that with x direction writing sequence, mask registration behavior in x direction is mainly related to sequence direction, but mask registration in y direction would be highly impacted by pattern density distribution map. It proves part of mask registration error is due to charge issue from nearby environment. If exposure sequence is chip by chip for normal multi chip layout case, mask registration of both x and y direction would be impacted analogously, which has also been proved by real data.

Therefore, we try to set up a simple model to predict the mask registration error based on mask exposure map, and correct it with the given POSCOR (position correction) file for advanced mask writing if needed.

9424-40, Session 9

Improving full-wafer on-product overlay using computationally designed process robust and device-like metrology targets

Young-Sik Kim, SK Hynix, Inc. (Korea, Republic of); Kevin Ryan, ASML Netherlands B.V. (Netherlands); Young-Sun Hwang, SK Hynix, Inc. (Korea, Republic of); Paul Tuffy, ASML US, Inc. (United States); Mi-Rim Jung, SK Hynix, Inc. (Korea, Republic of); Kyu-Tae Sun, ASML Korea Co., Ltd. (Korea, Republic of); Ji-Hwan Yoo, SK Hynix, Inc. (Korea, Republic of); Jin-Moo Byun, ASML Korea Co., Ltd. (Korea, Republic of); Won-Taik Kwon, SK Hynix, Inc. (Korea, Republic of); Nang-Lyeom Oh, ASML Korea Co., Ltd. (Korea, Republic of); Roy Werkman, Mir Shahrjerdy, ASML Netherlands B.V. (Netherlands); Seung-Hoon Park, Ki-Yeop Chris Park, Youping Zhang, ASML US, Inc. (United States)

In order to handle the upcoming 1x DRAM overlay and yield requirements, metrology needs to evolve to more accurately represent product device patterns while being robust to process effects, including at wafer edge. One way to address this is to optimize the metrology target design. A viable solution needs to address multiple challenges. The target needs to be resistant to process damage. A single target needs to measure overlay between three layers. Targets need to meet design rule and depth of focus requirements under extreme illumination conditions. These must be achieved while maintaining good precision and throughput with an ultra-small target. In this publication, a holistic approach is used to address these challenges, using computationally designed diffraction-based overlay (DBO) metrology targets.

Designing metrology targets that mimic device behavior is becoming one of the key components of overlay process control. The extreme illumination methods needed for the DRAM technologies makes it harder to control the aberration induced overlay delta between metrology target and device patterns. This mismatch can be minimized through the right choice of target and measurement recipe for best possible on-product-overlay performance and device yield.

In contrast to the traditional 'trial and error' approach to target design, this paper will evaluate a computational method. The algorithm simultaneously optimizes targets for process robustness and device matching, while applying constraints for precision and simulated throughput of the DBO metrology system. These optimized targets are then used to feed an advanced overlay control loop in the latest DRAM process. This paper reports on the on-product-overlay performance improvements which were achieved using this methodology, and the correlation between predicted and verified DBO target device-matching performance.

9424-41, Session 9

Advanced overlay analysis through design-based metrology

Sunkeun Ji, Gyun Yoo, Gyoyeon Jo, Hyunwoo Kang, Minwoo Park, Jungchan Kim, Chan-Ha Park, Hyun-Jo Yang, DongGyu Yim, SK Hynix, Inc. (Korea, Republic of)

As design rule shrink, overlay has been critical factor for semiconductor manufacturing. However, the overlay error which is determined by a conventional measurement with an overlay mark based on IBO and DBO etc. often does not represent the physical placement error in the cell area. The mismatch may arise from the size or pitch difference between the overlay mark and the cell pattern. Pattern distortion caused by etching or CMP also can be a source of the mismatch. In 2014, we have demonstrated that method of overlay measurement in the cell area by using DBM(Design Based Metrology)tool has more accurate overlay error than conventional method by using an overlay mark. We have verified the reproducibility by measuring repeatable patterns in the cell area, and also demonstrated the reliability by comparing with CD-SEM data.

We have focused overlay mismatching between overlay mark and cell area until now, further more we have concerned with the cell area having different pattern density and etch loading. There appears a phenomenon which has different overlay values on the cells with diverse patterning environment. In this paper, the overlay error has evaluated between cell edge and center. For this experiment, we have verified critical layer in DRAM by using improved(Better resolution and speed) DBM tool, NGR3520.

9424-42, Session 10

9nm node wafer defect inspection using three-dimensional scanning, a 405nm diode laser, and a broadband source

Renjie Zhou, Christopher A. Edwards, Casey Bryniarski, Gabriel Popescu, Lynford L. Goddard, Univ. of Illinois at Urbana-Champaign (United States)

The critical dimensions in the semiconductor manufacturing process have been shrinking rapidly over the past decades. Integrated circuit (IC) devices based on the 14nm node process have been developed recently. At the same time, three-dimensional (3D) and monolayer based transistors are also being developed. Thus, detection of killer defects in a patterned silicon wafer has become a grand challenge. In this paper, we present key results in our work over the past year. We demonstrated a 405nm laser based interferometric microscopy system for defect inspection of 9nm node densely patterned Si-wafers. Defects smaller than 15nm by 90nm by 35 nm have been detected in this wafer. We have verified our detection results with scanning electron microscopy (SEM). The success of the defect detection was ensured by the common optical path interference geometry, wafer mechanical scanning, and image post-processing.

To further improve our detection sensitivity, we investigated the wafer scanning stage and the light source. We first built a wafer scanning stage with < 10nm stepping precision and improved repeatability. This wafer scanning stage is capable of performing scanning in x, y, and z. It is also equipment with tip/tilt and rotation correction. Then, we replaced our laser source with a broadband source. In contrast to lasers, broadband or incoherent light sources have low spatial and temporal coherence. The spatial coherence is determined by the spreading of the wavevector k in space, while the temporal coherence is determined by the spreading of the wavelength. Incoherent light imaging systems are speckle free due to their low coherence, thus allowing for highly sensitive measurements. We incorporated these modalities into a bright-field microscope for the 9nm node wafer defect inspection. We performed both transverse and vertical wafer scanning. By volumetric processing the scanning images, we successfully detected the intentionally fabricated defect. At the same time, our system can detect dust particles, sort them according to their size, and localize them in all three dimensions.

Interferometric measurement gives both the phase and amplitude information of the scattered field coming from the wafer. It allows us to obtain both the topography and the reflection information of the wafer structure. Thus, we added a common optical-path interferometer to the bright-field microscope system. The reference beam was achieved with a projector-based spatial light modulator (SLM). The signal beam can also be filtered spectroscopically with the SLM. We have verified the phase and amplitude measurement accuracy of our system by measuring reference samples.

9424-43, Session 10

Material characterization at sub-50nm dimensions using coherent EUV beams

Kathleen M. Hoogeboom-Pot, Jorge N. Hernandez-Charpak, Damiano Nardi, Travis Frazer, Emrah Turgut, Univ. of Colorado at Boulder (United States); Erik H. Anderson, Weilun L. Chao, Lawrence Berkeley National Lab. (United States); Justin M. Shaw, National Institute of Standards and Technology (United States); Margaret M. Murnane, Henry C. Kapteyn, Univ. of Colorado at Boulder (United States)

Advanced materials development and device design require reliable characterization tools to discover, optimize and monitor new nanomanufacturing techniques. Moore's Law scaling has pushed the frontiers of nanofabrication so far that the thinnest films and smallest nanostructures being made today cannot easily be measured using current metrology techniques. Yet precise characterization of materials in nanostructured devices is necessary for understanding the unique physics which applies to such small-scale systems: how elastic properties change with scaling from monolayers to bulk material, for example, or how phonon spectra in materials govern thermal dissipation in the deep nanoscale regime << 100nm.

To overcome the challenges, we implement a non-destructive photoacoustic technique that uses coherent extreme ultraviolet (EUV) light from tabletop high harmonic generation (HHG) in place of more conventional optical-wavelength laser probes. The shorter wavelength of EUV beams is sensitive to picometer-scale displacements of the surface, while the femtosecond duration of HHG pulses is fast enough to capture sub-picosecond thermal and acoustic dynamics in few-nm scale structures.

Our samples consist of periodic gratings of metallic nanowires deposited on dielectric or semiconductor substrates. A femtosecond 800nm laser pump pulse is focused onto the samples to impulsively heat the nanostructures and launch acoustic waves: surface acoustic waves (SAWs) in the substrate with a wavelength set by the grating period and longitudinal waves (LAWs) within the nanostructures. All these dynamics can be monitored simultaneously by diffracting a 30nm-wavelength EUV probe beam from the surface. Expansion and cooling of the nano-gratings, as well as acoustic wave propagation dynamically change the EUV diffraction efficiency, and this signal is recorded by a CCD camera as a function of delay time between pump and probe pulses.

The SAW and LAW resonances of the nano-gratings yield information about the mechanical properties of the materials. In particular, by studying how these resonances shift for bilayer nickel-tantalum structures as the Ta capping-layer thickness is varied between 1 and 6nm (with Ni at a constant thickness of 10nm), we determine the densities and longitudinal acoustic velocities of both materials in the ultrathin layers. In doing so, we confirm for the first time that the densities of Ni and Ta are not changed substantially by their confinement to such thin layers, but the elastic properties differ significantly from their bulk values.

Moreover, the thermal decay signal reveals transitions among various heat dissipation regimes as the Ni heat source linewidth varies between 750 and 30nm. While previous work has observed and understood a decrease in thermal transport efficiency from nanoscale heat sources as the heat transfer process becomes increasingly non-diffusive, we observe for the first time that collective diffusion from closely-spaced nanoscale heat sources can restore efficiency toward the diffusive limit. Furthermore, the direct relationship between this new 'collectively-diffusive' regime and the particular phonon spectrum of the substrate material enables the characterization of these spectra in novel materials with the detail necessary for accurate predictions of heat dissipation in nanostructured systems.

9424-44, Session 10

Spectral emission of a tunable LPP light source for inspection applications from the sub-200nm range to the EUV range

Nadia Gambino, Bob Rollinger, Duane Hudgins, Alexander Sanders, Markus Brandstätter, Reza Abhari, ETH Zürich (Switzerland); Fariba Abreau, Adlyte (Switzerland)

In order to reach chip node sizes below 10 nm, the semi-conductor industry does not only need to investigate new lithography techniques such as Extreme Ultraviolet Lithography (EUVL), but the optical wafer inspection tools operating in the Deep Ultraviolet (DUV) range needs to be scaled to the sub-150 nm range in order to detect smaller device defects on wafers. Laser-Produced Plasmas (LPPs) are promising sources for EUV scanners and Actinic Mask (AIMSTM) inspection tools, but show potentials also for other metrology and optical inspection applications. Inspection applications require lower power levels, but higher brightness and stability with respect to the high-volume manufacturing (HVM) lithography light sources.

At the Applied Laser Plasma Science (ALPS) laboratory of LEC-ETH Zürich, a droplet-based laser-produced plasma source with application in EUV high volume metrology has been developed. The main source ALPS II is today fully operational and is equipped with a large capacity droplet dispenser. The dispenser generates micrometer-sized droplets with frequencies up to 100 kHz that are irradiated with a high power (1.6 kW), high repetition rate Nd:YAG laser, resulting in a high brightness and high power continuously operating light source. The source is also equipped with several plasma diagnostics such as radiation detectors and spectrometers that allow us to study the plasma emission proprieties from the EUV to the visible range. In this work, the spectral emission proprieties of the LPP are investigated in the VUV range from 30 nm to 150 nm. These studies are realized with a spectrograph operating from 30 nm to 550 nm at a spectral resolution of 0.06-0.1 nm. The emission spectra were studied for different droplet-based metal fuels such as tin, indium and gallium in the presence of different background gases and for different laser irradiances. These studies are relevant for alternative light sources that would be needed for future inspection applications. In addition, the experimental results help to determine the Out-Of-Band (OOB) radiation emission of the EUV source. By tuning the type of fuel, the laser energies and the background gas, the LPP light source shows good capabilities to operate as tunable light source covering a spectral emission range from the EUV to sub-200 nm range.

9424-45, Session 10

Scatterometry-based defect detection for DSA in-line process control

Robin Hsin-Kuo Chao, Chi-Chun Liu, IBM Corp. (United States); Cornel Bozdog, Aron J. Cepler, Matthew J. Sendelbach, Oded Cohen, Shay Wolfling, Nova Measuring Instruments Ltd. (Israel); Todd C. Bailey, Nelson M. Felix, IBM Corp. (United States)

Directed self-assembly (DSA) of block copolymers (BCPs) has developed into a promising nanolithography technique that can potentially improve both resolution and pattern quality to complement conventional photolithography. Process feasibility was successfully demonstrated on high volume manufacturing (HVM) wafer processing equipment , ; however, in-line process control, especially defect detection, still remains a great challenge as the throughput and sensitivity of existing toolsets may not be sufficient for the new DSA-specific defects.

Conventional brightfield optical defect scan tool is the standard methodology but may be limited by its optical resolution. Some researchers utilize top-down CD-SEM for qualitative defect analysis. Although CD-SEM provides the highest resolution, neither the necessary throughput for sampling sufficient wafer area nor the capability for in-line real time defect quantification has been demonstrated so far. Scatterometry was proposed

for DSA pattern metrology , but its effectiveness and throughput for defect detection has not been well characterized yet. In short, researchers are still pursuing a fast, non-destructive defect quantitative technique for in-line DSA process control.

The DSA defect detection and quantification of three novel scatterometry techniques have been investigated in this work. Using a "model-less" approach, where the defectivity data is directly extracted from the standard spectrum without reference to physical models, we found that spectral differentials between optical channels can be used to detect defects. Next, in model-based scatterometry approach , , where we modify standard modeling to include model parameter(s) that uniquely and independently describe defectivity, we found that such modifications to model-based scatterometry can separate the defectivity from the pattern profile information and yields a good correlation to the defect area as quantified by a reference extracted from CD-SEM. This correlation deviates at lower defect density regime, which indicates the limit of defect detection in current reflectometry-based tool set. Finally, a novel scatterometry configuration, Darkfield Spectral Reflectometry was proposed and studied and the initial results indicate a defectivity signal that is consistent with the reference metrology. The results in this work suggests that the defect density in DSA process can be quantified and monitored with scatterometry. Discussion on defect detecting limit in scatterometry tool set with potential directions for further studies will be provided as well.

9424-46, Session 10

Simulation of AIMS measurements using rigorous mask 3D modeling

Hsu-Ting Huang, Ru-Gun Liu, Tsai-Sheng Gau, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

AIMSTM tools have been widely used for wafer level inspection of mask performance and defects. Reported inspection flows include die-to-die (D2D) and die-to-database (D2DB) methods. The D2D approach can only be applied to patterns which repeat in different dies. For patterns that do not repeat in another die, only the D2DB approach is applicable. The D2DB method requires accurate simulation of AIMS measurements for a bona fide mask extraction. An optical vectorial model is needed to depict the mask diffraction effect in this simulation. As the pattern dimension continues to shrink, the conventional Kirchhoff model (thin mask model) is insufficient to describe the electro-magnetic field (EMF) scattering from the mask surface. To accurately simulate the imaging results, a rigorous EMF model is essential to correctly take account of the EMF scattering induced by the mask topography, which is usually called the mask 3D effect.

In this study, the mask 3D model we use is rigorous coupled-wave analysis (RCWA), which calculates the diffraction fields from a single plane wave incidence. Total mask diffraction fields from the partially coherent illumination source in optical lithography can be accurately computed using an Abbe model together with RCWA. However, the Abbe model is known for its high cost of computation time. A Hopkins model that simulates the EMF at a single angle of incidence (AOI) has errors when approximating the diffraction of light incident from a variety of spacial angles. A hybrid Hopkins model with RCWA can be used to calculate the EMF diffraction at a desired accuracy level while keeping the computation time practical. We will compare the accuracy and speed of the hybrid Hopkins model to the Abbe model. Results from the conventional vectorial Kirchhoff approach will also be calculated and used as a reference.

Since AIMS measurements provide full images on the wafer plane, these measurements contain more information than the conventional CD-SEM measurements, which only provide critical dimensions (CDs) or resist contours in some occasions. The CDs or contours merely convey the intensity information near the threshold level. The matching between simulation and experiment is therefore more challenging for AIMS because its measurements provide full intensity information. Parameters in the Mask 3D model such as pattern sidewall angle, film stack thickness, film optical properties, or pattern distortions, need to be adjusted during the fitting process. We will report the fitting results of AIMS images for structures with simple geometric shapes. By accurately simulating the AIMS measurements, one is capable of performing the mask inspection using the D2DB approach and accurately predicting the mask performance and defects.

9424-47, Session 11

A new paradigm for in-line detection and control of patterning defects

Stefan Hunsche, ASML Brion (United States); Marinus Jochemsen, ASML Netherlands B.V. (Netherlands); Vivek Jain, Xinjian Zhou, ASML Brion (United States)

With continuously shrinking design rules and corresponding low-k1 lithography, defectivity and yield are increasingly dominated by systematic patterning defects. The size of these yield-limiting defects is shrinking along with feature size, making their detection more difficult. Established distinctions between defects and CD control and also between inspection and metrology are beginning to disappear, requiring a new, holistic approach.

In this paper we discuss a novel approach to pattern defect detection and control, which integrates 1) full chip layout analysis and characterization by computational lithography, 2) utilization of wafer data from the scanner and inline wafer metrology such as Diffraction Based Focus (DBF) measurements on ASML YieldStar, 3) prediction of wafer locations with highest probability for defect occurrence, 4) defect verification by targeted SEM data acquisition and analysis at these specific locations, and 5) layout aware scanner corrections to reduce the overall defect probabilities.

We assess the various components of this flow by an experimental study on a 10 nm BEOL process at IMEC, using state-of the art negative tone development (NTD) and triple litho-etch patterning (LELELE) process. Most of the experiments are done using a half-field test layout of logic patterns that are constructed from a set of product-like standard cells.

We analyze the spatial distribution of process-window-limiting features in the layout, in the context of pattern-related best focus shifts in combination with wafer focus maps. Using computational lithography models we determined pattern printing characteristics and process margin limits across the entire reticle layout. In addition we identified and tagged specific hotspot patterns by pattern type and by location within the exposure field. Defect prediction on product wafers is based on calculating defect probabilities from locally available process window and local process condition estimates, e.g. focus offset distributions derived from scanner and DBF data.

We also established the capability to direct SEM image acquisition using an E-Beam Inspection tool, CD-SEM or Defect Review SEM to the predicted defect locations. A comparison of predicted resist contours at the hotspot patterns against simulations based on computational lithography models shows very good agreement of all predicted failure mechanisms, as well as good agreement between predicted and measured depth of focus limits, leading to the conclusion that for this process and set of patterns all defect types are in fact correctly captured.

9424-48, Session 11

Predictability and impact of product layout induced-topology on across-field focus control for 28 and 14nm FDSOI technologies

Jean-Gabriel Simiz, Bertrand Le-Gratiet, Pascal Gilgenkrantz, Alexandre Villaret, François Pasqualini, STMicroelectronics (France); Wim Tel, ASML Netherlands B.V. (Netherlands); Christopher Hugh Angus Prentice, ASML SARL (France)

With the dimension shrinkage, the depth of focus is reaching the scanner capabilities. Focus budget breakdown shows that intrafield contribution is

getting more and more significant and needs to be addressed.

Process induced topography as well as reduced Process Window can lead to yield limitation or killer defects on the wafer. The levelling capability of last generation scanners is getting improved but on the spatial scale of product layout still some significant levelling non correctable errors can be seen.

In the scope of improving the focus margin, understanding the correlations between scanner levelling performance, product layout and topography built-up brings very relevant information. Indeed, both topography and levelling intrafield fingerprints show a large part of systematics that is product related. In particular, scanner levelling Non-Correctable Errors maps present a lot of similarities with the layout of the product.

The present paper investigates the possibility to model the response of the level sensor as a function of layer design densities or perimeters data of the product. As the major part of this systematics is process induced topography due to previous deposition, etching and CMP, several layer density parameters were extracted from GDS. Those were combined through a multiple variable analysis (PLS: Partial Least Square regression) to determine the weighing of each layer and each parameter. Current work shows very promising results using this methodology.

In addition novel methods are shown on how to verify the impacts of topography on focus errors in resist and on product, as well as solutions to the impact of topography on FEM accuracy.

9424-49, Session 11

The analysis method of the DRAM Cell Pattern Hotspot

Kyusun Lee, KweonJae Lee, Jinman Chang, Tae Heon Kim, DaeHan Han, Ae-Ran Hong, Yonghyeon Kim, Jinyoung Kang, Bumjin Choi, Joo-Sung Lee, Hyeongsun Hong, Kyupil Lee, Joosun Choi, Gyoyoung Jin, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

It is increasingly difficult to determine degree of completion of the Pattering and the distribution at the DRAM Cell Patterns measured by CD-SEM is what effect on the device.

When we research DRAM Device Cell Pattern, there are three biggest problems currently, it is as follows. Firstly, it is difficult to predict the potential defect due to etch loading. Secondly, it is not possible to demonstrate the influence of the hotspot due to under Layer topology. Finally, it is not easy to predict final ACI pattern by the photo simulation, because photo pattern is completely different from final etch pattern. (because of Double Patterning Technology process) So, if the Hotspot occurs in any part of WF, it is very difficult to find it.

Among the instruments that are used in FAB, we are using CD-SEM mostly. CD-SEM is used to accurately measure small region of WF Pattern primarily. Therefore, there is no possibility of finding places where unpredictable defect occurs. Also, the other one, “Defect detector” is used to measure a wide area, but if there are same bridge pattern defects in the all chips, detector cannot detect critical hotspots like these patterns have difference between target layout and real wafer image. And this instrument is not distinguished the difference of distribution about 1nm~3nm. So, “Defect detector” is difficult to handle the data for potential weak point far lower than target CD.

NGR is used in order to measure accurately a small area such as CD-SEM and to inspect a wide range such as Defect detector simultaneously. This machine is used to compare WF Pattern with GDS directly, so it is possible to know WF Pattern’s errors immediately.

It is important to classify behavior of abnormal DRAM Cell Block Edge pattern. So, we have developed a new analysis method. Firstly, we modified the GDS by using the in-house tool, and then we have implemented the DPT ACI Final pattern. And, we have employed our new measuring method by our own technology, it is much more accurate than the normally method provided by the equipment company. Through this technology, we have studied DCGB(DRAM Cell-unit Genetic Blueprint) about Cell Block by using correctly extracted massive measured Data. It is possible to investigate accurately Hotspot occurrence coordinates within Cell Block Edge. (Figure 1. DCGB) Secondly, we have measured the multiple Chips & Blocks, and get a Mass-Data. And then we analyze Mass-Data by new analysis method that is a “Cell-unit-Block Composite Technology”. These methods can be used to avoid a misjudgment with data due to the wrong measurement of the specific WF area & Chip area. Finally, we could find out root cause of hotspots in Cell-unit-Block. Result of the iterative solution process, we could demonstrate the effects of the under layer by comparing the coordinates Hotspot and under layer Layout. In addition, by measuring the several location of WF and then By using this methods of analysis, it is possible to know the positional WF CD trends and a Shot CD trends. This means that we could predict yield results in advance without having to wait for full processed wafer.

In this study, using this innovative methodology, we have improved the potential weak points of 2Xnm DRAM Cell patterns currently in mass production. And, it has become to use as a criterion for yield enhancement through PWQ margin that was enlarged. These analysis methods give a high degree of completion of the Cell Pattering and the Distribution in sub-20nm product. And we are certain that it help also in the development of advanced process and Cell Layout.

9424-65, Session PSWed

Metrology of 50 HP wire-grid polarizer: a SEM-scatterometry comparison

Ruichao Zhu, The Univ. of New Mexico (United States); Sharwan Singhan, The Univ. of Texas at Austin (United States); Alexander R. Munoz, Arizona State Univ. (United States); Srinivasan Sreenivasan, The Univ. of Texas at Austin (United States); Steven R. J. Brueck, The Univ. of New Mexico (United States)

Scatterometry is used widely by the semiconductor industry as a fast, non-contact, non-destructive in-line measurement tool. Relatively few reports have discussed the extension of scatterometry to the extreme sub-wavelength scales that will be necessary for future nodes. As a start towards this goal, we have carried out scatterometry studies of a 50 nm half-pitch Al grating on top of fused silica substrate (a visible wire grid polarizer) fabricated by nanoimprint lithography and anisotropic etching. Measurements are reported at wavelengths of 244 nm and 405 nm. The reflection (0-order diffraction) is measured for incident angles of 8°-80° for all non-conical combinations of incident polarization and grating orientation. Simulation of the optical signature is by rigorous coupled wave analysis (RCWA). The grating profile is characterized by seven parameters (pitch, line width, sidewall angle, fused silica undercut depth, Al thickness, and horizontal and vertical extent of the top rounding). The simulation results show that the scatterometry signatures are very sensitive to grating parameter changes. The simulations act as a baseline library for the scatterometry measurements by fitting the experimental curves with the corresponding simulation parameters thus resulting in a grating profile. As expected, the signature from the 244 nm laser source is more sensitive to the details of the grating structure than the longer wavelength, 405 nm, measurements. For scatterometry, a cw wave laser is usually desirable as it eliminates pulse-to-pulse variations and provides a higher signal-to-noise. Our results show the 244nm laser is a good laser source to measure the structure around 100 nm pitch. The 405 nm results lose some information (especially on the fused silica undercut) and is not as accurate as the 244nm result, but it still reflects parts of the grating profile. Longer wavelength measurements (633 nm) will also be reported. These mimic the decreasing HP/Wavelength parameter that will be required at coming CD nodes. We also compare the results of scatterometry with the scanning electron microscope (SEM) images. They show the similar structure of the grating profile. There are also some discrepancies between the scatterometry grating profile and the scanning electron microscope (SEM) image which can be explained in terms of excess scattering from metallic structures and the finite beam size of the SEM.

This work is based upon work supported primarily by the National Science Foundation under Cooperative Agreement No. EEC-1160494. Any opinions,

findings and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the National Science Foundation.

9424-66, Session PSWed

High-throughput automatic defect review for 300mm blank wafers with atomic force microscope

Ardavan Zandiatashbar, Byong Kim, Young-kook Yoo, Park Systems Inc. (United States); Sang-il Park, Park Systems Corp. (Korea, Republic of)

While feature size in lithography process continuously becomes smaller, defect sizes on blank wafers become more comparable to device sizes. Therefore defect classification becomes more and more important for yield management and control. Defects on a blank wafer are inspected, reviewed, and repaired by different means. Defects with characteristic size comparable to light and electron beam wavelengths could be unclassified or misclassified by automated optical inspection (AOI) and require post-processing for proper classification.

As post-inspection metrology tools, electron microscopes are used for effectively classifying defects located by AOI. Although electron microscopy provides high resolution two-dimensional images, it could be a destructive method and lack enough accuracy in the measurements along Z axis for defects of nm-scale. On the other hand, atomic force microscope (AFM) is known to provide high lateral and the highest vertical resolution by mechanical probing among all techniques. [1] However its low throughput and tip life in addition to the laborious efforts for finding the defects have been the major limitations of this technique. In this paper we introduce automatic defect review (ADR) AFM as a post-inspection metrology tool for defect study and classification for 300 mm blank wafers and to overcome the limitations stated above. [2] In this AFM configuration, the Z and XY scanners are decoupled, made it able to obtain large scan images with nm-scale out of plane motion over full stroke. To minimize the stage errors and mismatch between AFM and AOI coordinates, the geometry of the wafer is used for coarse alignment. In addition, fine alignment of the coordinates is performed using enhanced vision on few optically visible defects. Locating of the defects, imaging, and defect classification are performed using the ADR automation software and at the throughput of several defects per hour. All of the images are collected using non-contact mode to preserve tip life and maintain data accuracy during the automation. The ADR AFM provides high throughput, high resolution, and non-destructive means for obtaining 3D information for nm-scale defect review and classification. Therefore this technology can be used for in-line defect review and classification.

[1] G. T. Smith, “Surface Microscopy,” in Industrial Metrology: Surfaces and Roundness, London, UK, Springer, 2002, ch. 3, sec. 1, pp. 103-105.

[2] “Automated AFM significantly boosts throughput in automatic defect review”, Nanoscientific, vol. Sep-2014, pp. 7-9, 2014, (www.nano-scientific.org).

9424-67, Session PSWed

High-order overlay modeling and APC simulation with Zernike-Legendre polynomials

Jae-Wuk Ju, Min-Gyu Kim, Ju-Han Lee, SK Hynix, Inc. (Korea, Republic of); Stuart Sherwin, KLA-Tencor Corp. (United States); Choon Hong G. Hoo, KLA-Tencor Texas (United States); Dong-Sub Choi, Do-Hwa Lee, Sanghuck Jeon, Kangsan Lee, KLA-Tencor Korea (Korea, Republic of); David C. Tien, KLA-Tencor Corp. (United States); Bill Pierson, John C. Robinson, Mark D. Smith, KLA-Tencor Texas (United States); Ady Levy, KLA-Tencor Corp. (United States)

Feedback control of overlay errors to the scanner is a well-established technique in semiconductor manufacturing. Typically, overlay errors are measured, and then modeled by least-squares fitting to an overlay model. Overlay models are typically Cartesian polynomial functions of position within the wafer (Xw, Yw), and of position within the field (Xf, Yf). The coefficients from the data fit can then be fed back to the scanner to reduce overlay errors in future wafer exposures, usually via an historically weighted moving average. In this study, rather than use the standard Cartesian formulation, we examine overlay models using Zernike polynomials to represent the wafer-level terms, and Legendre polynomials to represent the field-level terms. Zernike and Legendre polynomials can be selected to have the same fitting capability as standard polynomials (e.g., second order in X and Y, or third order in X and Y). However, Zernike polynomials have the additional property of being orthogonal over the unit disk, which makes them appropriate for the wafer-level model, and Legendre polynomials are orthogonal over the unit square, which makes them appropriate for the field-level model. We show several benefits of Zernike/Legendre-based models in this investigation in an Advanced Process Control (APC) simulation using highly-sampled fab data. First, the orthogonality property leads to less interaction between the terms, which makes the lot-to-lot variation in the fitted coefficients smaller than when standard polynomials are used. Second, the fitting process itself is less coupled – fitting to a lower-order model, and then fitting the residuals to a higher order model gives very similar results as fitting all of the terms at once. This property makes fitting techniques such as dual pass or cascading2 unnecessary, and greatly simplifies the options available for the model recipe. The Zernike/Legendre basis gives overlay performance (mean plus 3 sigma of the residuals) that is the same as standard Cartesian polynomials, but with stability similar to the dual-pass recipe. Finally, we show that these properties are intimately tied to the sample plan on the wafer, and that the model type and sampling must be considered at the same time to demonstrate the benefits of an orthogonal set of functions. Our results show opportunity for improved on product overlay (OPO) as compared with less optimal methods.

9424-68, Session PSWed

Continuous tool monitoring by means of product stream data analytics

Allan Minns, IBM Microelectronics (United States)

The primary means of monitoring microprocessor manufacturing equipment (tools) is often the use of dedicated wafers, specialized hardware contained within the tools themselves, or limited statistical process controls. While extremely useful, these techniques suffer from significant drawbacks. Dedicated monitoring wafers typically cannot be cycled very frequently, leaving open the possibility for extended periods of erroneous tool functionality. Specialized tool hardware, such as stage embedded resolution targets for critical dimension scanning electron microscopes (CDSEMs), suffer from a lack of diagnostic versatility. However, in cases where a tool processes a large number of parts per hour, metrological data analytics can be carefully deployed to both monitor for tool excursions in near real-time and discern the nature of the excursion.

The technique discussed here was modelled on engineering decision making and combines data from a plurality of tools, products, and databases to determine parameters indicative of acceptable processing. CDSEMs are uniquely capable in this regard because numerous attributes of the actual measurement are available. These attributes include (among many others) image intensity, edge entropy, and derived dimensions. While wafer processing may vary from time to time, once the process stabilizes and the measurement attributes take on predictable values, one can automatically assign probabilities to these reported attributes. In this way, excursions readily stand out as events whose attributes have very low cumulative probabilities. This is especially important in situations where unreported tool malfunctions (or even sub optimal operations) may result in out of spec parts appearing in spec.

A continuous stream of various products flowing from multiple process tools

into multiple measurement tools provides the foundation for powerful data analytics. This data flow can be harnessed to greatly reduce the mean time to detect excursions and rapidly answer basic questions such as whether or not a process or measurement tool malfunctioning, or a product simply out of spec. This technique has been successfully applied to monitoring CDSEMs and lithographic tools.

9424-69, Session PSWed

Overlay improvement using Legendre/ Zernike model-based overlay corrections and monitoring with interpolated metric

Md Zakir Ullah, Alan Lim, Rajanish Javvaji, Micron Semiconductor Asia Pte. Ltd. (Singapore); Boris Habets, Stefan Buhl, Georg Erley, Steven Tottewitz, Enrico Bellmann, Qoniac GmbH (Germany)

In leading-edge semiconductor manufacturing, the usage of higher-order grid corrections and higher-order intra-field corrections for overlay control has become a common practice. However, one of the drawbacks is that the higher-order parameters of the typically used polynomial models are not independent (orthogonal) from the common linear parameters or from themselves. Switching from a linear to a higher-order correction model impacts the linear parameters due to non-orthogonal model behavior. This occurs due to the higher-order parameters, which are typically noisier than the linear parameters and destabilize the linear parameters. Automatic process control (APC) feedback from noisy registration cannot react appropriately to model parameter drifts and jumps. On the other hand, chip sizes are often very large in high-volume manufacturing (HVM) memory production. Usually it is not possible to place intra-die overlay targets within the regular product structures of memory devices. Therefore, there is some concern about unseen overcorrection using higher-order intra-field corrections.

In this study we enabled orthogonal model corrections where model parameters do not influence each other as long as the measurement layout is sufficiently symmetric. For the grid correction we used Zernike polynomials, and for the intra-field correction we used a two-dimensional set of Legendre polynomials. We enabled these corrections by developing a transformation matrix because a scanner is incapable of correcting such orthogonal polynomials. Simulation with OVALiS software showed that the linear parameters were stabilized 200% when we used Legendre/Zernike modeling instead of standard polynomial models. The correlation between linear and higher-order parameters disappeared with combined Zernike/ Legendre polynomials. Overlay mean plus three sigma showed a significant improvement of up to 15~35% when run-to-run controller settings were optimized. We observed similar improvement on experimental wafers.

Additionally, we introduced an interpolated metric that probes the field with a dense grid. This interpolated metric showed that the Zernike/Legendre model-based correction does not cause the same overcorrection seen on the standard polynomial model. The interpolated metric agrees well with experimental and electrical data. We have tested higher-order process corrections comprehensively by enabling an orthogonal model and by making use of an interpolated metric to monitor the overlay performance. The orthogonal models can be implemented in the production line based on inline overlay data, where the interpolated metric will ensure that there is no overcorrection and no negative impact on product.

9424-70, Session PSWed

2D and 3D isolation mounts scatterometry with RCWA and PML

Hirokimi Shirasaki, Tamagawa Univ. (Japan)

Scatterometry is capable of measuring the critical dimension and profile measurements of grating structure. It is possible to get down to approximately 8nm with high precision in semiconductor manufacturing process control. The quality of measurement results depends on the setting groove model parameters, and on algorithms used by the analysis software. So, we develop the simulator to test the efficient parameter settings to raise the scatterometry's performance. In the papers on Microlithography in 2004-2008, we completed the 3D-FDTD analysis of the arbitrary shapes for isotropic and anisotropic mediums. In Microlithography 2010-2012, we developed the scatterometry simulation software that has the spectroscopy calculation and optimization algorithm systems. We calculated the spectroscopy using the Rigorous Coupled Wave Analysis that provides a method for calculating the diffraction of electromagnetic waves by periodic grating structures. The Conjugate Gradient and the Binary-Coded Genetic Algorithm methods were used to automatically search data that matches the given spectrum. In 2013, we sped up the scatterometry simulation for the 3D RCWA by using GPU and CUda LApack. The 2D scatterometry simulator was improved using a Real-Coded GA. In Microlithography 2014, we examined the sensitivity of scatterometry for the 2D isolation mounts on the substrate by applying the Perfectly Matching Layer in the RCWA. The RCWA is usually used for the period grooves and the scatterometry is now used for measuring the period groove shapes. We used the PML to absorb the outgoing waves from the interior of a period computational region for RCWA. Then, we showed it was possible to view the scatterometry for the isolation mounts on the substrate in several decade microns beam widths. In this paper, we continue to examine the scatterometry's sensitivity for the 2D isolation mounts. Then we examine the scatterometry for the 3D isolation mounts because the 3D metrologies will become important for 3D transistors. We examine the reflectance on the silicon and resist single mount and the silicon double mounts on the silicon substrate. First, we examine the mode convergences and the beam width dependences of reflectance. Second, we examine the wavelength properties of reflectance calculated by changing the beam width, the mount width and the mount height for single mount, and the mount positions for the double mounts. We also show the propagation properties of the electromagnetic fields propagating for the isolation mounts on the substrate. Next, the scatterometry simulator is developed for the isolation mounts using the Real-Coded GA. We use the RCGA to increase the population, to make a more sensitive solution and to get better fitting mount figures. The scatterometry characteristic is examined by choosing the n-th power cosine type mounts and approximating the smoothly changing mount shape with three or more trapezoids. Finally, we calculate the optical scattering property from the isolation mounts by the 2D and 3D FDTD analysis. We use Gaussian beams as incident waves. Then, we compare the scattering property results obtained from RCWA and FDTD method.

9424-71, Session PSWed

Novel self-calibration mark for overlay measurement

Teng-Chin Kuo, United Microelectronics Corp. (Taiwan)

Overlay measurement accuracy is important for 14nm beyond in order to meet rigid process requirement. Process induced overlay measurement error is noticeable since advanced process flow like metal gate, double-patterning and FinFET is more complicated than before. To minimize this measurement uncertainty, a novel Self-Calibration Mark (SCM) is designed for image-base overlay measurement to check and screen overlay measurement recipes. Different process steps like film deposition, thermal annealing and CMP cause overlay error could also be real-time monitored via SCM.

This calibration mark is designed and measured at 14nm gate layer and afterwards. 2 to 4nm process induced measurement error are detected at M0 layer by different measurement Recipes on current UMC 14nm FinFET process. The optimum overlay measurement recipe selected by SCM also matched with our electrical-test result. By SCM implement, a shorter cycle time for optimum overlay recipe selection compared to previous electrical-test method. This approach not only ranks overlay measurement recipes but also offers dynamic monitor of process variation. Furthermore, by site SCM to calibrate raw data error from within wafer process variation is our next step to study.

9424-72, Session PSWed

Novel self-calibration mark for overlay accuracy improvement

Nuriel Amir, KLA-Tencor Israel (Israel); Gary C. H. Wang, Simon C. C. Hsu, En Chuan Lio, Yuan Chi Pai, Sho Shen Lee, Chun Chi Yu, United Microelectronics Corp. (Taiwan); Henry Hsing, KLA-Tencor Taiwan (Taiwan); Tal Itzkovich, KLA-Tencor Israel (Israel)

Accuracy is the most critical element for overlay measurements for 14nm node and beyond, due to the stringent process requirement allowing only a few nanometers for the entire overlay budget. Overlay accuracy measurement error induced by the process is significant in advanced processes exhibiting multiple complex processing elements such as metal gate and FinFET on top of double patterning.

In this paper we present a novel Self Calibration Mark (SCM) and the real time measurement methodology for improving overlay accuracy. Improved accuracy is achieved through reducing the impact of process induced overlay errors from multiple steps such as: polish, etch, thin film deposition and thermal annealing. The contribution of each process element to the overlay error can be monitored in real time. Since measurement accuracy depends strongly on the right selection of the overlay measurement recipe conditions, we can improve accuracy by verifying that the measurement conditions accurately describe the SCM Overlay value.

This Self Calibration Mark was designed at the 14nm Gate layer with zero-offset of overlay between inner and outer AIM marks. We measured overlay data starting with the photo resist at Gate layer and on etched film pattern in the following process steps. Process induced overlay error at different steps was extracted by comparing the overlay data for each step with the overlay data at the resist level. Measurements results indicate up to 2 to 4nm of process induced overlay error at interconnect layers by different measurement conditions. The NIR filter was selected as the optimum wavelength for the overlay measurement recipe with the smallest process induced error on the current UMC 14nm FinFET process. This optimum overlay measurement recipe selected by SCM also matched with electrical-test results.

With SCM and the corresponding measurement methodology, a significantly shorter time to accurate measurement was achieved, especially when compared to the traditional use of electrical test as the calibration tool.

The next steps are the design of SCM with different overlay offsets and the calibration by site of raw data error from within wafer process variation.

9424-73, Session PSWed

Overlay target selection for 20nm process on A500 LCM

Vidya Ramanathan, KLA-Tencor Corp. (United States); Lokesh Subramany, GLOBALFOUNDRIES Inc. (United States); Tal Itzkovich, KLA-Tencor Israel (Israel); Chanseob Cho, GLOBALFOUNDRIES Inc. (United States); Lipkong Yap, KLA-Tencor Corp. (United States); Bill Pierson, KLA-Tencor Corp (United States); Patrick W. Snow, Karsten Gutjhar, GLOBALFOUNDRIES Inc. (United States)

Persistently shrinking design rules and increasing process complexity require tight overlay (OVL) control thereby making it imperative to choose the most suitable overlay measurement method technique and complementary target design. The different optical overlay methods which are currently used, imaging based OVL and scatterometry based OVL, may show exhibit different measurement performance for each layer. This arises primarily due to the, which is due to the fundamental technical differences between the two methodologies in the physics of the measurement and the design of the target. In this paper we compare explore these two methodologiess for several layers with different stacks and thereby optical properties.

In this paper we describe an assessment of various target designs from FEOL to BEOL on 20-nm process. Both scatterometry and imaging measurement method techniques were reviewed for several key layers on KLA-Tencor A500 LCM tool, which enables the use of both imaging and scatterometry methodsplatforms. Different sets of SCOL (Scatterrometry based overlay) and AIM targets were carefully designed and printed while taking into consideration the process and optical properties of each layer. Once targets were printed, performance comparison was done between different target types: SCOL 4 cell targets, measured by scatterometry, and Blossom, AIM and TripleAIM, measured by the imaging technique. For each target the optimal measurement settings was selected based on Total Measurement Uncertainty (TMU) performance and OVL performance (raw OVL values and modeled linear OVL residuals). TMU was calculated as below:

TMU=√(〖TIS3SIG〗^2+〖Precision〗^2)

The optimal overlay target for a given layer was then chosen based on its measurement performance on the tool and correlation to reference OVL Blossom or AIM imaging targets (Blossom or AIM). For some certain layers, a comparison was done between measured OVL and reference metrology will be explored as well. Preliminary rResults show indicate that for some certain layers imaging based OVL using AIM target is the optimal method choice, while for some certain other layers scatterometry based OVL using SCOL 4 cell target is the optimal methodtarget. Additional imaging target type, TripleAIM, which enables OVL measurement between across 3 layers, was evaluated as well.

9424-74, Session PSWed

Qmerit-calibrated overlay to improve overlay accuracy and device performance

Md Zakir Ullah, Mohamed Fazly Mohamed Jazim, Stella Sim, Alan Lim, Liew Chia Chuen, Biow Hiem, Liew Chia Chuen, Micron Semiconductor Asia Pte. Ltd. (Singapore); Jesline Ang, Ek Chow Lim, KLA-Tencor Singapore (Singapore); Dana Klein, Eran Amit, KLA-Tencor Israel (Israel); Roie Volkovitch, David Tien, KLA-Tencor Corp. (United States); DongSub Choi, KLA-Tencor Korea (Korea, Republic of)

In advanced semiconductor industries, the overlay error budget is getting tighter due to shrinkage in technology. To fulfill the tighter overlay requirements, gaining every nanometer of improved overlay is very critical in order for devices to function properly during technology development and in order to accelerate yield in high-volume manufacturing (HVM) fabs. To achieve meet the stringent overlay requirements, fabs often use higher-order grid and field corrections, correction per exposure (CPE) and other techniques which require sufficiently accurate measurement data to prevent unexpected instability in the production line and to prevent yield loss. To meet the stringent overlay requirements and to overcome other unforeseen situations, it is becoming critical to eliminate the smallest imperfections in the metrology targets used for overlay metrology. For standard cases, the overlay metrology recipe is selected based on total measurement uncertainty (TMU). However, under certain circumstances, inaccuracy due to target imperfections can become the dominant contributor to the metrology uncertainty and cannot be detected and quantified by the standard TMU. For optical-based overlay (OBO) metrology targets, mark asymmetry is a common issue which can cause measurement inaccuracy, and it is not captured by standard TMU.

In this paper, we established a new calibration method, Archer Self Calibration (ASC), to improve overlay accuracy on image-based overlay (IBO) metrology targets to accelerate device yield. This method makes the overlay measurement robust to target imperfections without deteriorating its sensitivity to the target overlay and without causing any throughput penalty. ASC uses a quality merit, Qmerit, to estimate quantitative inaccuracy and calibrate measured data. Qmerit quantifies the target asymmetry based on the discrepancy between two algorithms applied on the same target. However, it requires an inaccuracy function that

needs to be calculated based on multiple conditions in order to calculate actual inaccuracy per measurement point. Once this inaccuracy function is generated, a new recipe is produced to provide inaccuracy calibrated overlay data.

In this study, we developed a new color selection methodology for the overlay metrology recipe. We used Qmerit-calibrated data for linear process corrections and fine process corrections (CPE) at multiple process layers, with multiple devices. This study shows that color filter can be chosen more precisely with the help of Qmerit data. Overlay stability improved by 10~20% with best color selection, without causing any negative impact to the device. Post-CPE residual error, as well as overlay mean plus three sigma, showed an improvement of up to 20% when Qmerit-calibrated data was used. We observed up to 30% improvement in certain electrical failures associated with tested process layers.

9424-76, Session PSWed

A difractometer for quality control in nanofabrication processing based on subwavelength diffraction

Martin Kreuzer, Jordi Gomis-Bresco, Institut Català de Nanociència i Nanotecnologia (ICN2) (Spain); Marianna Sledzinska, ICN2 (Spain); Clivia M. Sotomayor-Torres, Institut Català de Nanociència i Nanotecnologia (ICN2) (Spain) and ICREA-Institucio Catalana de Recerca i Estudis Avançats (Spain)

Optical techniques can control nanometer scale dimensions, like scatterometry controls thin films thickness, by monitoring the changes of a particular optical property. The link between the nanometer scale critical dimension (CD) and the optical property can be done by tracing back the optical property change or by comparing with a previously acquired/ calculated library.

In the last years, we have developed a methodology for controlling the fidelity of nanoimprinting lithography: subwavelength diffraction (SWD) .It's well known that in a diffraction grating by changing the shape of the motive (the cell that repeats) one can select the light intensity distribution. In particular, to maximize the light filtered out by a monocromator, blazed grating are designed to distribute most of the light in the +1 diffraction order, reducing the losses (light diffracted in the other diffraction orders).

The CD of that repeated cell lay in the nanometer scale, and if repeated with fidelity in all of the periods determine the intensity distribution of the light diffracted by the grating. In the same way that scatterometry and ellipsometry relay on libraries to detect critical dimension changes, we can establish a univocal relation between the diffraction pattern of a grating (the intensity versus collected angle measurement) and the nanometer scale CD of the repeated cell. Using this concept, in periodic structures (diffraction gratings) dimensional sub-wavelength features can be detected from the diffraction pattern (or diffractogram), given that enough orders of diffraction are measured and that the accuracy of the measurement allows distinguishing deviations from a reference. Most of the mass production nanofabrication processes, like nanoimprinting lithography, consist on reproducing a cell with nanometer scale features at least hundreds of times in a repetitive continuous way. The results of such approaches are periodic arrays of cells with well-defined nanometer scale CD. The periodicities are normally in the micrometer range, and because of that, the periodic arrays constitute themselves good diffraction gratings for optical light.

Once we defined the magnitude to measure (diffractogram) we focused in making the metrology compatible with the fabrication process. Diffractograms are normally collected by repositioning the wave source and the detector (what determines the diffraction angle) in a sequential way. Standard X ray machines are a good example. Sequential acquisition is slow by nature and does not allow monitoring more than one order of diffraction at a time. We have developed a diffractometer that allows implementing inline SWD as a metrology tool for inline nano fabrication. The optical design allows measuring at once (milisecond acquisition times) the diffraction pattern of an optical diffraction grating without movable parts and with high accuracy. The illuminated zone can be made as small as few 10ths of microns, improving the contrast for local defectivity, or arbitrarily big.

9424-77, Session PSWed

High-sensitivity tracking of CD-SEM performance

Sergey Babin, Peter Yushmanov, Igor Gudich, abeam Technologies, Inc. (United States)

The performance of CD-SEMs and any other e-beam system changes with time due to system instability, column contamination, cathode degradation, sample charging, and environmental changes. The measured values of critical dimensions (CDs) directly depend on the performance of the system. When measured CDs are out of spec in manufacturing, it is crucial to determine whether this is due to process variation or due to the metrology tool. Multiple methods have been employed so far, such as measuring CDs on "golden" wafer and image sharpness monitors. However, as technology progresses, these methods suffer from linewidth variations on the wafer, as well as from variations of line edge and linewidth roughness.

The developed method utilizes advanced algorithms that are capable of quantitative extraction of SEM performance. The method is independent of linewidth, LER, or LWR, and has high sensitivity. This software, QSEM, was developed to automatically evaluate image quality and assign a value to that quality. The image quality value is based on multiple factors such as noise, sharpness, analysis of histograms, and charging.

Images of production wafers, as well as test images, were input into the software. Multiple microscopes have been evaluated. The results produced by QSEM are discussed. The estimated sensitivity to image sharpness is from 0.05 to 0.1 image pixels, which is about 0.04 nm. One of the series of images included images taken when the beam was variably defocused: the QSEM software determined that autofocusing of the CD-SEM was not set up at the optimal value. Using QSEM daily for SEM images allows the performance of CD-SEMs to be tracked for proper calibration and preventive maintenance, as well as resolves the dispute between the process or metrology failures.

In addition, the BEAMETR product automatically measures the beam size, which is one of the main characteristics of any e-beam system. The measurement is based on the known parameters of the test sample and the spectral frequency analysis of the SEM image of the sample. The extension of this method, the extraction of the modulation transfer function for SEMs, is discussed briefly.

9424-79, Session PSWed

Improvement of depth of focus control using wafer geometry

Jaydeep K. Sinha, KLA-Tencor Corp. (United States); Honggoo Lee, Jongsu Lee, Sangjun Han, Changhwan Lee, Myoung Soo Kim, Sangmin Kim, Wontaik Kwon, Sung-ki Park, SK Hynix, Inc. (Korea, Republic of); Sathish Veeraraghavan, J. H. Kim, Pradeep Vukkadala, KLA-Tencor Corp. (United States); Jungho Byeon, KLA-Tencor Corp. (Korea, Republic of); Dieter Meuller, KLA-Tencor Corp. (United States)

For several decades, semiconductor industry has been controlling the site flatness and edge flatness of the starting wafer material by defining tight specs that scales with technology nodes on industry standard site flatness metrics such as SFQR and ESFQR. The need for controlling site flatness of the starting material stems from previous research that shows site flatness metrics directly impacts lithography defocus. Though controlling starting material flatness is a good start towards improved yield the geometry of the wafer changes significantly by processes downstream such as CMP,

bevel etch, and film dep. Hence, for 2x and smaller technology nodes with very stringent focus process window it is critical to control wafer flatness variations caused by processes downstream.

In this paper, the capability of an interferometer based patterned wafer metrology tool to predict lithography defocus is validated by comparing the measured site flatness with scanner leveling data at a FEOL litho-step with large edge defocus issues. The full wafer flatness variation map measured by the metrology tool shows that there is significant edge roll-off which is quantified by the ESFQR metric to be 1.3 microns. This is an order of magnitude larger than the typical ESFQR values of approximately 125 nm observed for starting wafer and might be the root cause of large defocus issues near the edge. The good correlation observed between site flatness measured by the metrology tool with scanner leveling data validates the capability of the patterned wafer metrology tool to predict lithography defocus.

The other goal of this work was to identify FEOL processes including CMP and bevel etch that changes wafer flatness and eventually non-correctable defocus issues at the critical litho-steps. Wafer geometry parameters were monitored to understand the impact of process conditions such as deposition chambers, stations, and thermal conditions. By tuning different knobs on deposition and other process tools a process window concept was created to control wafer geometry specification in order to meet the depth of focus requirements.

9424-80, Session PSWed

Through pitch monitoring by optical scatterometry

Robert Melzer, GLOBALFOUNDRIES Dresden Module One LLC & Co. KG (Germany); Carsten Hartig, GLOBALFOUNDRIES Dresden Module Two, GmbH & Co. KG (Germany); Gunter Grasshof, Bjoern Sass, Fernando Koch, GLOBALFOUNDRIES Dresden Module One LLC & Co. KG (Germany); Jan Engelmann, KLA-Tencor Germany (Germany); Zhi Qing Xu, Zhenkui Shen, KLA-Tencor China (China)

Optical critical dimension (OCD) scatterometry in state of the art semiconductor manufacturing is a well-accepted and powerful technique to determine profile properties such as critical dimensions, sidewall angles, trench depths as well as layer thicknesses of microelectronic structures. The amount and combination of information receivable via OCD measurements makes it, as long as interpreted correctly and incoming process variations especially incoming material variations are well understood, superior to other measurement techniques such as critical dimension scanning electron microscopy (CDSEM), transmission electron microscopy (TEM) or atomic force microscopy (AFM). For high throughput inline process monitoring and feedback OCD models are usually generated for uniform gratings having fixed pitches representing dense areas of the microelectronic chip design. However, for purposes such as improvement in process tool matching, wafer uniformity or optical proximity correction (OPC) it is of great value if the measured test patterns do have different layout properties being representative for other design elements and styles as well.

In this paper a through pitch OCD measurement within the shallow trench isolation (STI) layer on the 28nm node is presented. This approach allows to interpret, to tune and to monitor process tool behavior for different pattern densities using only one single specially designed lithography mask. Two different use cases are shown. For varying pitch sizes either the designed line CD or the designed space CD kept constant.

General OCD modelling approaches and examples to illustrate the key idea and practical use will be provided.

9424-81, Session PSWed

Understanding CD-SEM artifacts by comparing experiment with simulation

Alessandro Vaglio Pret, KLA-Tencor/ ICOS Belgium (Belgium); Chao Fang, KLA-Tencor Texas (United States); Joost P. Bekaert, IMEC (Belgium); Stewart A. Robertson, John J. Biafore, Mark D. Smith, KLA-Tencor Texas (United States)

Most of the characterizations and the analysis of features after lithography and etch is based on top-down CD-SEM measurements. These tools are used throughout the semiconductor industry for process R&D, process monitoring during production, and for Optical Proximity Correction (OPC) and verification. The most common outputs of CD-SEM metrology are critical dimension (CD), roughness (LWR, LER for lines, CER contacts) and evaluation of printing uniformity for dense and sparse features. Despite the high accuracy and reproducibility, all these outputs suffer from metrology mismatch, artifacts due to top-down 2D reconstructions of 3D features, charging and damaging. Unwanted or unknown offsets related to metrology represent critical issues that jeopardize OPC, processing, and production yield.

In this work we present a study that compares simulated and experimental SEM images of an OPC dataset for Process Windows (PW) band verification, where top-down SEM metrology causes a severe CD offset between dense and isolated trenches. Trenches across pitch were exposed on the ASML NXT:1900i at imec in focus-exposure matrices using a commercial positive-tone resist. CD and LWR after exposure were collected using the same metrology settings through pitch and used to calibrate a stochastic resist model in PROLITHTM via simulated SEM images. LWR was also matched to Power-Spectral Density (PSD) analysis for the dense and the isolated cases. A global root-mean square model error of less than 2nm was achieved after calibration (Table 1). When comparing simulated dense trenches with isolated trenches, we found that a fixed metrology plane through aerial image or simulated resist polygons produced a severe CD offset, as can be experimentally noted in Figure 1 (top). In this particular case, due to resist thickness loss and profile differences between the dense and isolated trenches, an equal threshold-to-height metrology in the middle of the resist would have resulted in a CD overestimation of roughly 30nm on isolated trenches. Comparing experimental top-down SEM and cross-section images with simulations, we can see how this CD offset caused by metrology is captured “for free” by calibrating top-down SEM images and resist profiles.

Enabling synthetic SEM images during resist calibration allows metrology-aware lithography simulations and OPC.

9424-82, Session PSWed

Overlay measurement accuracy enhancement by design and algorithm

Hong-Goo Lee, Byongseog Lee, Sangjun Han, Myoung Soo Kim, Won-Taik Kwon, Sung-Ki Park, SK Hynix, Inc. (Korea, Republic of); Tal Itzkovich, Yuri Paskover, KLA-Tencor Israel (Israel); Dong-Sub Choi, Do-Hwa Lee, Sanghuck Jeon, Kangsan Lee, KLA-Tencor Korea (Korea, Republic of); Amnon Manassen, KLA-Tencor Israel (Israel); David C. Tien, KLA-Tencor Corp. (United States); Negri Daria, David Gready, Eitan Herzel, KLA-Tencor Israel (Israel)

Overlay is one of major challenges in lithography, considering the difficulty to meet the required overlay performance for the advanced device. This is because the required overlay performance is very close to the accumulated best performance of overlay components like scanner, mask, process and metrology.

Optimal overlay design would be cheapest solution for overlay improvement comparing with other hardware related solution. But it doesn’t mean it

is also easy to find the optimal design. In this study, we will show the methodology to find optimal overlay mark design to achieve better overlay performance.

Optimal target design requires two prerequisites. One is process robustness and the other is metrology-friendly. If the design is not robust enough, profile of overlay mark will be damaged by process, since device process is being optimized to guarantee the device pattern, not overlay mark. If the overlay mark is being damaged, measurement result will be very sensitive over measurement conditions like wavelength and worst case, it will report inaccurate overlay results and also noisy measurement results which ends up with high residual. The other prerequisite is metrology-friendly and this is often contradicting with process robustness in terms of strength of signal. For example, one of the ways to be robust over the process is staying within the design guide which requires segmentation for the bars of overlay target. But, segmentation will reduce the contrast loss for the measurement. In this study, we showed the procedure and investigation result.

Target design will help to enhance the process robustness. But, enhancing measurement algorithm to overcome process induced measurement inaccuracy is another way to improve measurement accuracy. We developed the new algorithm to minimize the inaccuracy. In this study, we will show the new algorithm result comparing with current algorithm.

9424-84, Session PSWed

Lithography process controllers and photo-resistance monitoring by signal response metrology (SRM)

WeiYuan Chu, KLA-Tencor Corp. (United States); Wei-Jhe Tzai, United Microelectronics Corp. (Taiwan)

For advanced lithography metrology, SCD (Scatterometryl Critical Dimension) tool is a common mean applied to the control process. SCD tool has the capability to report accurate data information (Critical Dimensions), PR SWA (Side Wall Angle) and PR HT (Height). The items of PR profile correlates with the inline process controllers which are mainly referring to focus and energy dose. SCD is a model based metrology tool; to decode the process controllers, it is requires the computation through a model. Once the model extracts the information of PR CD, PR SWA and PR HT from spectrum, one can further correlate the geometry items with the process controllers further and monitor of the controllers. However, information loss is a major concern. During the data transformation, noise and model can distort the signals. It is said, the interested degree, focus and dose, might not be true to the original.

Foundry therefore seeks a methodology to monitor focus and dose with the least amount of steps requiring information transformation. SRM (Signal Response Metrology) is to be demonstrated in this paper. SRM is a new technique that obviates the need for geometric modeling by directly correlating focus, dose, and CD variation to spectral response of a scatterometry tool.

9424-85, Session PSWed

Lithography process related electrostatic discharge effect mechanism study

Xiaosong Yang, Semiconductor Manufacturing International Corp. (China)

Electrostatic discharge (ESD) problem resulting from charges on wafers is a serious concern in IC manufacturing. In the photolithography process, ESD charge effect is mainly considered during the mask making and reticle maintenance but seldom be noticed in the lithography process flow itself. As is discovered in our paper, 3 types of defect , AA (active area) damage, gate oxide break through and IMD (Inter Metal Dielectric) oxide crack that are confirmed to be induced by lithography process induced ESD charging effect. We carefully studied the mechanism of these ESD charging effect by systematic DOE splits and succeeded to dig out that these electric charges comes from the spin process during PR coating and developing. In the lithography coating and developing wafer process, the wafer will be at high spin speed at many of the steps which will easy help to store the electric charge on the wafer. In our study, the rinse step in developing process is the most key factor to store the electric charge on wafer. In generally, the higher rinse speed, the higher positive electric charge. Furthermore, we also discovered that the different step in develop rinse process have different impact on charge level, in which the acceleration and deceleration step has the highest charge voltage.

In fab process real situation, there are 3 major types of ESD charge effect was discovered. The 1st type ESD charge effect is discovered in the thin oxide layer such as DG (dual gate) and LDD (light doped drain) layer , this type ESD charge is detected as pin hole or poly/gate oxide/AA(active area) burn out, and tightened KLA scan recipe help us to catch this type of ESD charge in-line; The 2nd type ESD charge effect is discovered in the IMD layer during Via photo process , this type of ESD charge is reported as IMD crack with worse wafer center defect map which can be easy detected by in-line defect scan; While, the last type of ESD damage discovered in Al BEOL metal layer process is the hardest to be detected and identified, this type of ESD charge has no any defect signal in Litho in-line process detection methodology , but it will finally neutralize the metal etch O2 plasma which may have influence on Al etch galvanic corrosion effect with early fail from wafer edge. Of these 3 different type of ESD charge effect, no matter what is the different defect type and failure mechanism in different process step, the most key process factor to dominate ESD charge in photo process is just the develop rinse step. As is in our study, with the wafer surface condition change, different process will have different optimized develops rinse speed range.

As to minimize and eliminate the ESD damage in lithography process, we finally carry out the simplified recipe optimization solution which only need optimize for the develop rinse speed with different in-coming surface charge level and process application, so that can be easy implemented in the worldwide fabs.

9424-86, Session PSWed

Scanner focus metrology for advanced node scanner monitoring and control

Jimyung Kim, Youngsik Park, Taehwa Jeong, Su Hyun Kim, Kwang-Sub Yoon, Byoung-il Choi, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Vladimir B. Levinski, Daniel Kandel, Yoel Feler, Nadav Gutman, Eltsafon Island-Ashwal, Moshe Cooper, DongSub Choi, Eitan Herzel, Tien David, JungWook Kim, KLA-Tencor Israel (Israel)

Scanner Focus window of the lithographic process becomes much smaller due to the shrink of the device node and multi-patterning approach. Consequently, the specification of scanner focus becomes tighter and more complicated focus control/monitoring methods such as field-by-field focus control or intra-field focus control is a necessity.

Moreover, the tight scanner focus specification starts to raise another fundamental question, accuracy of the reported scanner focus. The insufficient accuracy of the reported scanner focus using the existing methods is coming from two main origins: 1) focus measurement quality, which is due to low sensitivity of measured targets; 2) the scanner focus is estimated using special targets, e.g. large pitch target and not using the device-like structures. Both these factors are eliminated using KLA-Tencor proprietary “Focus Offset” technology.

We investigated the followings for scanner focus measurement

- Empirical target design.
- Recipe settings, including measurement algorithm.
- Accuracy: correlation of the reported correctable with the offset between the scanner focus and the best focus position of the device.

Optimization was performed for advanced node and for optimal target design using the KLA-Tencor proprietary Focus Offset Targets technology which provides printability and sensitivity in a sufficiently large process

window, while maintaining small target sizes.

This investigation involves also recipe optimizations which decide the measurement conditions like wavelength, polarization, algorithm ...etc.

In this investigation, we used measurements comparison to validate the quality of the reported correctable focus values along with the theoretical (theory/simulation) and empirical investigation of the accuracy of the reported focus, measured using KLA-Tencor proprietary "Focus Offset" metrology technology.

9424-87, Session PSWed

The use of eDR-7100 for DSA defect review and automated classification

Hari Pathangi, Hareen Bayana, Dieter Van Den Heuvel, IMEC (Belgium); Loemba Bouckou, KLA-Tencor France (United States); Jim Brown, KLA-Tencor Corp. (United States); Paolo Parisi, KLA-Tencor Italy SRL (Italy); Roel Gronheid, IMEC (Belgium)

Directed self-assembly (DSA) plays a promising role as an alternative patterning candidate in future fabrication flows. One of the main challenges for DSA processes is to understand the possible root cause(s) of the different kinds defects and to reduce the total defect density to a production-relevant number [1]. In this direction, it is of utmost importance to be able to locate and identify the DSA defects, some of which are rather unique in terms of their size, structure and morphology compared to the defects seen in more conventional process flows [2].

This paper summarizes the work completed as part of the equipment validation for the KLA-Tencor's eDR-7100, a scanning electron microscope (SEM)-based 300 mm wafer defect review and classification system, at imec, Belgium. The main objective of this manuscript is to demonstrate the efficiency of eDR-7100 in automated defect classification for the 14 nm half-pitch chemo-epitaxy line/space DSA flow implemented at imec. Creating an automated defect classification scheme for a process flow in R&D phase is quite challenging due to the overwhelming number of defects, the new types of defects and their variability that come with the different process steps and materials.

Setting up an automatic defect classification with the eDR-7100 is a two-step process. Initially, an optimized recipe is created to capture the SEM images of defect locations identified by the broadband optical defect inspection tool (KLA2835) and by tuning-in offset values to account for the stage offset between the two tools. The image capture rate of the eDR-7100 with a typical review recipe of a DSA wafer after pattern transfer is about 1700-1900 images/hour, including the automatic defect location (ADL) and the automatic defect classification (ADC) images.

An iDOTM (inline Defect Organizer) is then created that uses a list of parameters from the raw ADC images to create an automated defect classification algorithm. A set of manually pre-classified images are then fed into the offline analysis software from KLA-Tencor for completing the iDOTM using a tree structure. This iDOTM, when linked to the review recipe, carries out the automated defect classification during the image capture and bins the different images under different class codes. This manuscript will present quantitatively the efficiency of this automated classification compared to manual classification and a case study showing a reduction in the tool-time for image capture and time needed for manual defect classification at least by a factor of 2.

References

[1] R. Gronheid et al., Proc. SPIE (2014), Vol. 9049, 904905-1.

[2] C. Ito et al., Proc. SPIE (2014), Vol. 9049, 90492D-1.

9424-88, Session PSWed

Real-time decision-based multiple mode SEM review imaging solution

Harsh Sinha, Huina Xu, KLA-Tencor Corp. (United States); Garry Chen, White Pai, United Microelectronics Corp. (Taiwan)

Embedded defect types continue to be a challenge for scanning electron microscopes (SEM) review solutions. Though high energy beams can be used to image these defect types, they cause damage to the reviewed sites. Also, imaging all review sites at higher electron energy has often resulted in low topography surface defects to be non-visible due to high penetration depth. In this work we present a method in which defects are reviewed at non-destructive lower electron energies and only the non-visual review sites are reviewed at higher electron energies to image any potential additional defect types. The non-visual defects are identified inline during review using automatic defect classification attributes.

In this specific case, we reviewed a poly removal step wafer. Using a low electron energy beam, residues and patterning errors were identified. However, they represented only 47% of the total defects with the remaining53% identified as SEM NonVisual (SNV). These SNV locations were determined in real-time using an automatic defect classifier, allowing the sites to be sub-sampled with higher electron energy review. This higher electron energy review revealed that the SNV defects were actually real buried void defects.

Figure 1 (a) shows an example of residue which can be seen using low electron energy beam. Though no high electron energy beam image was captured for that defect in auto review, a manual review image, shown in figure 1 (b), shows that higher landing energy limits from the imaging of these residue defects. Alternatively, a buried void defect is determined to be SNV when reviewed with low electron energy beam, as shown in figure 1(c). When this site was auto-classified and then auto-reviewed with high electron energy beam in the same job a buried void was identified. This can be seen in figure 1 (d).

The next best alternative to the proposed method has been to review all defects with different imaging conditions leading to >2x review time and greater SEM imaging induced damage. To conclude, this method provides an effective method to produce an accurate defect Pareto while optimizing review time and review induced damage.

9424-89, Session PSWed

SEM critical point imaging (CPI) technology using high-resolution SEM images at pre-defined locations on the die and on the wafer for newest technology nodes

Dominique Sanchez, STMicroelectronics (France); Loemba Bouckou, KLA-Tencor France (France); Remi Le Tiec, Benôit Hinschberger, STMicroelectronics (France); Olivier Moreau, KLA-Tencor Corp. (United States); Paolo Parisi, KLA-Tencor Italy SRL (Italy)

In order to optimize the time to market of the newest technology nodes and maximize their profitability, advanced semiconductor manufacturers need to adapt their yield enhancement strategies to their current development stage. During very early development, gross defectivity at some critical process steps often makes it impractical to use broadband plasma or laser scanning micro-defect patterned wafer inspection technique such sensitive defect inspections capture a large number of defects, producing wafer defect maps so heavily populated that even wafer level signature are difficult to visualize. I.

INTRODUCTION

A scanning electron microscope (SEM) can be a powerful alternative for providing engineers with an understanding of critical defects during the very early development stage. Rather than inspecting an entire wafer, a SEM equipped with Critical Point Inspection (CPI) technology captures high-resolution SEM images at pre-defined locations on the die and on the wafer.

In order to yield useful information the CPI image capture needs to fulfill the following requirements:

1/ use the best resolution possible – 1.5nm

2/ provide a high signal-to-noise image in order to visualize elusive defects such as subtle line pinching, pattern deformations, systematic bottom bridging in high aspect ratio structures, etc.

3/ be extremely accurate in its location in order to be able to get the critical points in a field of view 100% of the time

4/ be fast enough to capture hundreds of locations on a wafer while avoiding bottlenecks on the review tool.

In this study, the utilization of CPI for the early development of 14nm design rule technologies is described. CPI allowed the monitoring of known "hot spots" – locations where the chip design is less robust to process variation. By evaluating split lots experiments with the CPI technique, R&D engineers obtained faster time-to-information from the ease of use and output data quality of the technique.

METHODOLOGY

A-Presentation

Introduced in KLA-Tencor system eDR-5210 Series*, Critical Inspection Point (CPI) is a SEM technique used to inspect hot spots-locations*. The methodology of CPI consist of collecting SEM images at a wafer site location, which has been predefined by users.

To perform a CPI test, users have to setup an eDR-xxx recipe which requires to :

1/ Set up die dimensions by loading KLARF* file from an inspection tool

2/ Perform an optic alignment

3/ Setup and check SEM images and focus conditions

The CPI* process flow is quite simple in such way that eDR-xxx* system moves the stage to a defined wafer site location (hot spot), performs site focus, grabs a SEM* image of hot spot location, and moves the stage to the next wafer hot spot site location. The process described previously is repeated until all site location predefined are visited. The die dimensions allows eDR-xxx* system to move across wafer site locations.

Beam conditions and focus parameters defined in recipe, ensure the quality of SEM image collected. The hot-spot locations on a die, defines a site location of interest where IC process requires a special monitoring. The system stage accuracy is critical in positioning the SEM* beam close enough to hot-spot location to be visited during CPI process flow. Wafer mapping or die sampling complete the following steps.

4/ Select hot-spot location on a die

5/ Define wafer mapping or die sampling

defines the position of die to be visited during CPI process flow.

Different type of CPI techniques have been developed among the eDR-xxx series development. We can distinguish two main CPI type: CPI DDL* and CPI Align. In CPI DDL technique, system provides SEM images of hot spot site location predefined by user, rather in CPI Align technique, eDR-xxx system provides perfectly aligned SEM image of hot spot location predefined by user.

9424-90, Session PSWed

Study on ADI CD bias correlating ABC function

Guogui Deng, Jingan Hao, Bin Xing, Yuntao Jiang, Gaorong Li, Qiang Zhang, Liwan Yue, Yanlei Zu, Hua-Yong Hu, Winnie Liu, Manhua Shen, Skin Zhang, Haichao Huang, Wei-Ming He, Deping Kong, Kaiting He, Nannan Zhang, Yi-Shih Lin, Qiang Wu, Xuelong Shi, Semiconductor Manufacturing International Corp. (China)

As the technology node of semiconductor industry is being driven into more advanced 28nm and beyond, the ADI (After Development Inspection) CD (Critical Dimension) budget and control is more and more important. 1nm even 0.5nm CD difference is critical for process control. In this paper, we studied one function in CD SEM (Scan Electronic Microscope) measurement, i.e. ABC (Adjust of Brightness and Contrast). We revealed how addressing focus and even the choice of addressing pattern may bring in a systematic error into the CD measurement result. This provides a more comprehensive overlook of CD measurement and the measurement consistency of TP (Through-Pitch) pattern and inline pattern.

ABC is a basic function of CD-SEM measurement. It provides the basic parameter of brightness and contrast of the measured pattern under very high pattern magnification (usually 200K ~300K). Therefore, ABC is always carried out under the same pattern magnification for the parameters are magnification-correlated. There are two ways of doing ABC: in-situ ABC (ABC carried out exactly on the measured pattern) and off-site ABC (ABC carried out on patterns next to the measured pattern). Each way has its pros and cons. The in-situ ABC could provide more applicable parameters but induce certain damage to the PR (Photo Resist) which enlarges CD. Each way has its own niche for different measurement request, as long as the induced impact is predictable.

9424-91, Session PSWed

CD uniformity imporvement of dense contact array in negative tone development process

Fengnien Tsai, Teng-Hao Yeh, Chin-Cheng Yang, Elvis Yang, Ta-Hung Yang, K. C. Chen, Macronix International Co., Ltd. (Taiwan)

Layout pattern density impacts mask critical dimension uniformity (MCDU) as well as wafer critical dimension uniformity (WCDU) performance in some respects. In the mask making process, layout pattern density influences the MCDU through electron-beam scattering over a local region, development loading and etch loading effects. In wafer lithographic process, apart from the MCDU directly affecting the WCDU, the other possible factors associated with the layout pattern density to influence WCDU include optical proximity, optical flare, chemical flare and development loading effects.

In patterning the 86nm-pitch dense contact array with negative tone development (NTD) process, the abrupt pattern density change around the array edge of a NTD mask arises as a very challenging issue for achieving satisfactory WCDU. The wafer-level critical dimension of contact holes in the preliminary stage can gradually vary ~5nm from array corner to array center, with around 160um extension along diagonal direction of array. In figuring out the causes of uneven post-developed contact dimension around the array boundary, development recipe optimization, soft-bake/post-exposure-bake temperature splits and layout pattern density splits through extending the sub-resolution assist features (SRAF) coverage around array boundary were explored to differentiate the dominant factors. Through the understanding of critical factors affecting the WCDU, the suitable solutions on improving WCDU for patterning dense contact array with NTD process was proposed.

9424-92, Session PSWed

Real-time and large-field FF-OCT

Yue Zhu, Nanjing Univ. of Science and Technology (China)

Full-field optical coherence tomography (FF-OCT) capable of in vivo cellular-level imaging is demonstrated for non-scanning horizontal cross-sectional imaging in this paper. The system is based on a white light

interference microscope illuminated by a tungsten halogen lamps. A pair of identical high NA microscope objectives are used for imaging. We developed a single chip which generating two signals, one for PZT and the other for CCD, as a result, the entire system is synchronous conveniently. It takes 60 seconds to get high quality en face images or only 10s to normal en face images with lower quality. Using an ultra-broad bandwidth illumination incorporated with relatively high NA (0.5 NA) objectives, our experimental setup achieves an axial and lateral resolution in tissue of 1.3 μm and 0.89 μm respectively. A field of view of 228 μmx171 μm is covered by the 640x480 pixel CCD cameras. We present images of onion cells taken by old and new system for comparison. In vivo images of human finger skin which reveal cellular-level structures are also given in this paper. Our system is characterized by its high resolution, low cost and simple arrangement for adjustment, providing a practical and quicker method of performing FFOCT in vivo imaging, it is definitely significant for assisting physicians in clinical diagnosis.

9424-93, Session PSWed

Improvement of ArF immersion lithography by filtration technology

Tung-Chang Kuo, Met Yeh, Yeh Sheng Lin, Lian Cong Liu, Wen Liang Huang, Chun Chi Yu, Isaac Chao, Chun-Chung Chuang, Yi Nan Cheng, Will Tseng, United Microelectronics Corp. (Taiwan)

The scaling down of features sizes on leading-edge semiconductor manufacturing applications has employed various advanced lithography techniques to enable further technology progression. Among available technologies, the most effective way to shrink feature size is the improvement of optical imaging through the introduction of shorter wavelengths at exposure and an increase of numerical aperture. However, EUV lithography featuring an exposure wavelength of 13.5nm has been repeatedly delayed. In response to these delays, device manufacturers have widely adopted multiple patterning technologies. This poses a challenge to a semiconductor fab as multiple patterning techniques increase both the complexity and number of lithography process steps. Following this technical trend, the need for new yield enhancement technologies are getting increasingly vital to the effective manufacturing of today's semiconductor devices. One such yield enhancement technology is photochemical filtration to remove defect-causing particles and gels before they contact the wafer. As the sensitivity of defect inspection tools increases, the cleanliness of the filter itself has also compounded the challenge.

In this paper, we evaluate the performance of several types of filter cleaning technologies and their effect on photolithographic performance. Nylon and poly-ethylene membrane based filters were mainly used in this evaluation. And filters with different cleanliness characteristics are also evaluated to confirm the importance of filter cleanliness. The chemicals used for this evaluation is ArF immersion resist with positive tone imaging. The defectivity performance was validated with a wafer defect inspection tool. These evaluation results show that filters with higher cleanliness characteristics are effective in reducing on-wafer defectivity. We also evaluated the influence of the filter kind on lithographic performance. Finally, we will also show that newly developed filters have the performance necessary to be further enable advancements in leading-edge semiconductor device manufacturing.

9424-94, Session PSWed

Study on immersion lithography defectivity improvement in memory device manufacturing

Wei-Ming He, Hua-Yong Hu, Qiang Wu, Semiconductor Manufacturing International Corp. (China)

As semiconductor integrated circuit industry steps into immersion lithography's era, defectivity in photolithography becomes more complex which requires more efforts in the analysis and solution finding when compared to traditional dry lithographic process. In this paper, we focus on one type of immersion defect from memory or flash memory devices with typical mask layouts. Since the use of self-aligned double patterning (SADP) or other double patterning techniques, the original single pattern layer has to be split into 2 mask layers: logic area vs cell area. One characteristic of such split process is that the total mask transmission rate (TR) is above 70%, with both big open areas and a cell area with a transmission rate close to 50%. This indicates that it may have special defect mechanism and type compared to logic devices. We have found that one type of defect is a "blob" defect with center ring-like map. We have studied this defect with different development recipes and analyzed their underlying mechanisms. We have also studied the effect of different mask layouts and different photo-resists including types with topcoating and without topcoating, as well as the effect of BARC substrate (organic-BARC/Si-BARC). The results of our study will be presented and discussed.

9424-96, Session PSWed

Carbon dioxide gas purification and analytical measurement for leading edge 193nm lithography

Sarah Riddle Vogt, Chuck H. Applegarth, Matt Browning, SAES Pure Gas, Inc. (United States); Cristian Landoni, Marco Succi, SAES Getters, S.p.A. (Italy); Simona Pirola, Giorgio Macchi, SAES Getters S.p.A. (Italy)

The use of purified carbon dioxide (CO2) has now become a reality for leading edge 193 nm immersion lithography scanners. Traditionally both dry and immersion 193 nm lithographic processes have constantly purged the optics stack with ultra-high purity compressed dry air (UHPCDA). This constant purge flow is intended to protect the lenses from the detrimental effects of Airborne Molecular Contaminants (AMCs). AMCs can be in the form of acids, bases, organics, and/or refractory compounds. These contaminants are known to create a wide range of lens contamination issues. These effects become more pronounced when the presence of AMCs is combined with high energy laser radiation (typical for lithography processes). Sources of AMCs are everywhere in the Semiconductor plant and can come not only from impurities in the lens purge gases but from outgassing of plant materials, people, and chemicals used in the fab. The presence of AMCs at extremely low levels, such as single digit part-per trillion volume (pptV), has proven to be harmful when they are present in UHPCDA.

Carbon dioxide has been utilized for a similar purpose as UHPCDA. AMC purification technologies and analytical measurement methods have been extensively developed to support the Lithography Tool Manufacturers purity requirements. For Extreme-Ultraviolet (EUV) lithography, CO2 is also utilized with even tighter purification requirements also removing moisture, oxygen, hydrogen, and methane. While UHPCDA is generally produced from on-site gas compressors and subsequent purification; carbon dioxide sources can vary significantly from region to region, even for the same purity grade.

This paper covers the analytical tests and characterizations carried out to asses impurity removal from 3.0N CO2 (beverage grade) for its final utilization in 193 nm and EUV scanners. Over 200 efficiency and capacity tests have been carried out in 100% CO2 utilizing 3.0N gas from several different gas companies. Results will be presented for the following impurities O2, H2O, CO, H2, Toluene, Butane, Xylenes, IPA, Benzene, Hexane, HMDSO, H2S, COS, CS2, SO2, NOx, NH3, and CH4.

9424-98, Session PSWed

EUV tools: hydrogen gas purification and recovery strategies

Sarah Riddle Vogt, Charles H. Applegarth, SAES Pure Gas,

Inc. (United States); Cristian Landoni, Marco Succi, SAES Getters S.p.A. (Italy)

The technological challenges that have been overcome to make EUV (Extreme ultraviolet lithography) a reality have been enormous. This vacuum driven technology poses also significant purity challenges for the gases utilized for purging and cleaning the scanner EUV chamber and source. Hydrogen, nitrogen, argon, and ultra-high purity compressed dry air (UHPCDA) are the most common gases utilized at the scanner and source level. Purity requirements are tighter than for previous technology nodes tools. This paper will review the types of purification technologies that are currently available to generate high purity hydrogen starting from an already clean source that is at least 99.99% pure. Other technologies also widely used in gas purification, like pressure swing absorption (PSA) and membrane separation, that are more suitable to handle a lower degree of hydrogen purity will not be discussed. The advantages and disadvantages of adsorbers, getters, cryogenic and palladium purification technologies with guidelines on how to select the most appropriate technology depending on the application and the experimental conditions will be discussed. In addition, specifically for hydrogen, EUV tool users are facing not only gas purity challenges but also the need for safe disposal of the hydrogen at tool outlet. Recover, reuse, and/or recycling strategies could mitigate the disposal process and tool cost of operation. This paper presents the most common approaches utilized at the facility level to operate EUV tools along with hydrogen recovery strategies.

9424-99, Session PSWed

Silicon fin line edge roughness determination and sensitivity analysis by Mueller matrix spectroscopic ellipsometry based scatterometry

Dhairya J. Dixit, Samuel O'Mullane, SUNY College of Nanoscale Science and Engineering (United States); Erik R. Hosler, Vimal K. Kamineni, Moshe E. Preil, GLOBALFOUNDRIES Inc. (United States); Kevin Heidrich, Nick Keller, Joseph Race, Nanometrics Inc. (United States); Gangadhara Raja Muthinti, IBM Semiconductor Research and Development Ctr. (United States); Alain C. Diebold, SUNY College of Nanoscale Science and Engineering (United States)

Line edge roughness (LER) represents one of the current challenges of semiconductor technology process control. As the critical dimensions (CD) of patterned structures decreases, LER of a few nanometers becomes crucial as it negatively affects the performance characteristics of the fabricated device. Application of Mueller matrix spectroscopic ellipsometry (MMSE) based scatterometry to determine LER in periodic line-space structures is demonstrated utilizing 28 nm pitch Si fin samples fabricated by directed self-assembly (DSA) patterning. Mueller matrix (MM) elements' optical response within the model is influenced by structural parameters like pitch, CD, height and side-wall angle (SWA), as well as their associated effective optical properties. Evaluation and decoupling MM element response to LER from other structural parameters requires sensitivity analysis, carried out with the help of a forward problem approach to scatterometry and optical model simulations. Here, an approach is developed to quantify Si fin LER by comparing the optical responses generated by systematically varying the grating shape and measurement conditions. Finally, the validity of this approach is established by comparing the obtained result to the extracted Si fin structural profile retrieved from the inverse problem approach and top down scanning electron microscope (SEM) images.

9424-100, Session PSWed

Transient tip-sample interactions in high-speed AFM imaging of 3D nanostructures

Aliasghar Keyvani, Hamed Sadeghian, Technische Univ. Delft (Netherlands) and TNO (Netherlands); Hans F. L. Goosen, Fred van Keulen, Technische Univ. Delft (Netherlands)

Scanning probe microscopy has been suggested as an alternative technology for metrology and inspection of nanostructures for future semiconductor applications. However, scanning probe technologies suffer from lack of throughput. Thus, fast and parallel operation has been proposed to meet the inspection requirements of the industry. One important issue in high speed imaging is that the probability of damaging the tip or the sample will be increased.

In the high speed operation, changes in topography, which occur in time intervals shorter than the response time of the cantilever, result in a transient motion of the cantilever that increases the probability of damage. Especially in the case of sharp steps in topography (such as FinFET) the applied forces are much higher than what is expected for steady state conditions.

In this paper the tip-sample interactions in transient conditions have been investigated and it will be demonstrated that the forces in transient conditions scale with the apparent mass of the tip as well as its stiffness, while in steady conditions they only scale with the spring constant. As a show case, the effect of transient interaction on scanning a 14 nm FinFET has been studied. Results from this study are used in designing a cantilever (patent pending) that exerts lower forces in transient conditions in compared to a normal probe with the same spring constant by reducing the apparent mass.

9424-51, Session 12

Intra-field patterning control using high-speed and small-target optical metrology of CD and focus

Hugo Cramer, Stefan Petra, Bastiaan Onne Fagginger Auer, Henk-Jan Smilde, Steven Welch, Baukje Wisse, Stefan Kruijswijk, Frank Staals, Christian Leewis, Paul Hinnen, Stuart Young, Mark Maslow, Michael Kubis, Arie den Boef, ASML Netherlands B.V. (Netherlands)

Today's CD-uniformity (CDU) requirements ask for a tight control of all processing-induced patterning variations. This drives improvements in measuring tools and correction capabilities of the involved production tools. The state-of-the-art scanner offers higher-order interfield and intrafield correction potential of CD, through dose and focus corrections. This requires metrology schemes with dense spatial (interfield and intrafield) and high temporal (lot-2-lot and wafer-2-wafer) sampling densities which can be supported by integrated scatterometry[1].

In practice post-litho processing (e.g. etch) is a major contributor to variations in final CD. State-of-the-art etchers offer higher-order correction potential, through multi-zone temperature control among other added control possibilities. In addition the scanner can be used to correct remaining CD variations, in particular intrafield variations. Using these full correction capabilities in a tight control loop also drives the sampling density of after-etch CD metrology towards multiple fields and multiple points per field.

For this application we have evaluated a high-NA full-azimuth angle-resolved scatterometry solution with the capability to measure on small areas (below 15x15μm2). The high NA enables the spatial resolution, and the combination with a high-brightness source also leads to sub-second Move-Acquire-Measure (MAM) times. Finally, the selectable wavelength(s) of this tool helps to maximize the process-robustness of the CD measurement recipe.

We will present densely sampled metrology data measured with this tool on small targets on product wafers. Analysis demonstrates the small target capability of the measurement tool by comparison with standard target size reference metrology. The analysis of intrafield and wafer-2-wafer variations will reveal the potential value of the high-speed, high-sampling-density metrology in controlling after-etch CD variations.

9424-52, Session 12

Comprehensive BEOL control using scatterometry and APC

Padraig R. Timoney, Sudhir Baral, Laertis Economikos, Jamie Tsai, Alok Vaid, GLOBALFOUNDRIES Inc. (United States); Haibo Lu, Byungcheol Kang, Paul K. Isbester, Prasad Dasari, Naren Yellai, Nova Measuring Instruments Inc. (United States)

Copper interconnects have been adopted in advanced semiconductor manufacturing due to benefits of reduced RC delay, cross talk and power consumption. With each technology node, interconnects reduce in size resulting in increased line resistivity, a critical metric in determining the device performance. Reactive Ion Etching (RIE) and Copper Chemical Mechanical Processing (Cu CMP) are two of the key back end of the line (BEOL) processes that affect the interconnect performance. Due to the underlying topography and nature of these processes, reduced incoming trench depth and subsequent metal line height that can potentially result from these processes have direct impact to RC delay.

Traditional inline metrology methods used are time consuming and do not provide the needed wafer level metrics. In addition, measurement of remaining dielectric thickness on solid pads is not a good representative of the actual device structures and has been shown insufficient for process monitoring especially with decreasing thickness of copper pads. Efficient control of BEOL processes requires measurement of metal line thickness and other critical profile parameters from which resistance can be extracted. In order to relate BEOL process steps and understand their interactions, it is necessary to have a directly comparable measurement methodology on a similar measurement structure.

Over the past several years, scatterometry has been proven as the only metrology method to provide the full profile information of the Cu lines. Scatterometry is a diffraction based optical measurement technique using Rigorous Coupled Wave Analysis (RCWA), where light diffracted from a periodic structure is used to characterize the details of profile. Unique algorithms, such as Holistic Metrology can be used to make the scatterometry development process faster.

In this paper, we will present how scatterometry can be used to measure copper line height on 3D structures and how feed forward from RIE can be applied for control of Cu CMP process for 20nm technology node. Figure 1 demonstrates the need for CMP to understanding incoming trench depth variations in order to stabilize the copper line height. Validation data is presented for different scatterometry models including accuracy, repeatability and DoE tracking. The paper will demonstrate the capability for reducing copper line height variation and the correlation of the reducing trench height variation to improved stabilization of electrical resistance.

9424-53, Session 12

Hybrid metrology implementation: server approach

Alok Vaid, Carmen Osorio, Givantha Iddawela, Jamie Tsai, Florence Nelson, GLOBALFOUNDRIES Inc. (United States); Eyal Grubner, Nova Measuring Instruments Ltd. (Israel); Byungcheol Kang, Paul K. Isbester, Matthew J. Sendelbach, Cornel Bozdog, Nova Measuring Instruments Inc. (United States)

Hybrid Metrology (HM) is the practice to combine measurements from multiple toolset types in order to enable or improve the measurement of one or more critical parameters required for process control of advanced devices, materials and architectures. Continuing our previous work, here we report on advances in integration of multiple toolsets with respect to software (data analysis algorithms, combined usage of different toolset data) as well as hardware (methodologies to transfer data from one toolset to the other in the fab environment).

Implementation of Hybrid Metrology in the Fab can be split into two phases. Phase 1 includes the readiness of infrastructural setup to ensure that the processed data from first metrology toolset (e.g secondary tool) is made available to the second metrology tool (primary tool) before the actual measurement, thereby allowing the primary tool to yield hybridized output. Phase-2 incorporates the infrastructure that would allow sharing and parallel interpretation of of raw data between toolsets such as spectra for OCD/ Film Thickness, images for CDSEM, trace data for AFM, etc (universal hybrid engine – co-optimization). Phase 2 is currently viewed as the all-inclusive final goal of Hybrid Metrology approach.

In previous report we discussed the first-in-industry implementation of HM Phase 1 in High Volume Manufacturing, where communication of processed data between toolsets takes place through host and presented preparations for Phase 2 (offline hybrid co-optimization of data from multiple toolsets). Here we discuss extension of Phase 1 to include direct high-bandwidth communication between toolsets via dedicated Hybrid Server, enabling seamless deployment into HVM without added complexity of host protocol changes, and further lay down the framework for Phase-2 HVM implementation. We will demonstrate qualification and production implementation of 20 & 14nm complex applications.

9424-54, Session 12

Machine learning and predictive data analytics enabling metrology and process control in IC fabrication

Narender Rana, Yunlin Zhang, Todd C. Bailey, IBM Corp. (United States)

Processor technology is going through multiple changes in terms of patterning techniques (multipatterning, EUV and DSA), device architectures (FinFET, nanowire, graphene) and patterning scale (few nanometers). These changes require tighter controls on processes and measurements to achieve the required device performance, and challenge the metrology and process control in terms of capability and quality. Multivariate data with complex trends and correlations generally cannot be described well by mathematical models but can be relatively easily learned by computing machines and used to predict or extrapolate. We have studied the use of machine learning and analytics to accurately predict dimensions of EUV resist patterns down to 18 nm half pitch leveraging resist shrinkage patterns. These patterns could not be directly and accurately measured due to metrology tool limitations. Machine learning models are also used in process control where, for example, the electrical test results are predicted early in the processing flow invoking appropriate actions. We have developed insights in the multivariate data correlations using the data mining and analytics tool developed by IBM for semiconductor applications. We report results from various cases and experiments on metrology enhancements and process control. Figure 1 shows improved correlation of predicted resistance values to the measured ones through a neural network as compared to the linear multivariate regression model that is typically used in process control. This paper provides other similar insights and a general overview of machine learning and advanced analytics in the advanced semiconductor development and manufacturing.

9424-55, Session 12

Optimizing hybrid metrology: rigorous implementation of Bayesian and parallel regression

Mark-Alexander Henn, Richard M. Silver, John S. Villarrubia, Nien-Fan Zhang, Hui Zhou, Bryan M. Barnes, Bin Ming, András E. Vladár, National Institute of Standards and Technology (United States)

Hybrid metrology, i.e. the combination of several measurement techniques to determine critical dimensions is an important approach to meet the needs of semiconductor industry. A proper use of hybrid metrology may not only yield more reliable estimates for the quantitative characterization of 3-D structures but also a more realistic estimation of the corresponding uncertainties. Recent developments at NIST feature the combination of optical critical dimension (OCD) measurements and scanning electron microscope (SEM) results. The hybrid methodology offers the potential to make measurements of essential 3-D attributes that may not be otherwise available. However, combining techniques gives rise to essential challenges in the error analysis and combined model function spaces.

Critical dimensions in this setting are determined by fitting the model data which is supposed to be a function of the critical dimensions f(x) to the measurement data y. This is equivalent to minimizing the difference measure or chi square function (f(x)-y)^T V(f(x)-y), with V denoting a weight matrix, which in most cases is supposed to be a diagonal matrix.

One of the key challenges here is the question how well the involved model functions, namely the models for the OCD and the SEM, can be approximated by linear functions. This is important since a highly non-linear behavior affects the solution in many ways. It might not only increase the time needed to determine the critical dimensions but can also lead to the presence of many local minima of the chi square function. Furthermore it can yield erroneous uncertainty estimates. We give examples for non-linear behavior and show alternative approaches to the minimization and the error estimation in those cases.

The second challenge lies in the fact that the critical dimensions are determined by minimizing the weighted chi square function that measures the goodness of fit between the model(s) and the measurement data. Usually the weights are chosen to account for the errors that are present in the measurement, making an accurate modelling of those errors vital for a reliable determination of the critical dimensions and also for reasonable uncertainty estimates. We demonstrate how not only the magnitude of those errors but also correlations due to systematic effects might impact the solution.

Finally we compare the Bayesian approach to the approach using parallel optimization. Remember that the Bayesian approach uses the result of one measurement method as an input to the other, while the parallelization deals with the minimization of a chi square function that is the sum of the individual chi square functions. An important question that will be investigated in this presentation is under which circumstances the solutions obtained by those two different methods coincide.

Possible solutions to each of the challenges are illustrated by means of both hypothetical examples and measurement data.

9424-83, Session 12

Holistic approach using accuracy of diffraction-based integrated metrology to improve on-product performance, reduce cycle time, and cost at litho

Kaustuve Bhattacharyya, ASML Netherlands B.V. (Netherlands); Chih-Ming Ke, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

The high-end semiconductor lithography requirements for CD, focus and overlay control drove the need for diffraction-based metrology and integrated metrology (IM). Both diffraction-based overlay (DBO) and IM are now successfully deployed in high-volume manufacturing at 2-x and 1-x production nodes.

One of the most critical enablers in this deployment is the upfront prediction (well before a wafer measurement to take place) of overlay metrology accuracy via target design simulation called “design for control” or D4C. Traditional metrology-precision (“TMU”), matching and speed are of course important and good performances for those are maintained (tool matching overlay data will be included from over 100 YieldStar system in production), but additional attention is paid towards “accuracy” as this has a direct impact to on-product performance.

The other most critical enabler is IM allowing a faster feedback of the litho cluster performance trend while reducing litho-metro cycle time and cost.

Going forward in 1-x development node, more complex lithography techniques (such as multiple patterning), advanced device designs (such as advanced FinFET), as well as advanced materials (like hardmasks) are introduced. These pose new challenges for metrology accuracy, litho-metro cycle time and process control. In this publication several systematic steps are taken to face these challenges (figure 2 in attached).

First is to address the increase of metrology sampling to support multi-patterning. It is a fact (figure 1 attached) that multi-patterning creates an significant increase in litho-metro cycle time (doubling or even tripling metro-sampling). Integrated metrology becomes extremely necessary to control this cycle time jump. A faster “integrated” YieldStar metrology system (T250D) is introduced to enable the measurement speed. Multi-layer overlay targets are introduced to enable multiple measurements in a single acquisition and a fully automated track-buffer logistics using IM is deployed to address cycle time reduction. Focus metrology is also used in integrated mode in addition to overlay and this combination helps cycle time even further.

Then an advanced version of the predictive target design (D4C) is deployed. This not only ensures precision and speed but also addresses accuracy and robustness of metrology measurements to process variation beyond HVM conditions to support process development phase (where a high degree of process variations expected).

Finally, to achieve desired process window control, the above accurate measurement data is captured in integrated metrology mode using an advanced sampling and the data is fed back to scanner using a novel control-mechanism (containing the highest order of correction possible today using a sophisticated interfaces on the scanner).

The above holistic approach for process window control using on-product metrology (overlay, focus) data will be discussed in details in this publication.

9424-56, Session 13

Intra-field on-product overlay improvement by application of RegC® and TWINSCANTM corrections

Ofir Sharoni, Carl Zeiss SMS Ltd. (Israel)

The on product overlay specification and Advanced Process Control (APC) is getting extremely challenging particularly after the introduction of multi-patterning applications like Spacer Assisted Double Patterning (SADP) and multi-patterning techniques like N-repetitive Litho-Etch steps (LE, N ≥ 2). When the latter is considered, most of the intra-field overlay contributors drop out of the overlay budget. This is a direct consequence of the fact that the scanner settings (like dose, illumination settings, etc.) as well as the subsequent processing steps can be made very similar for consecutive Litho-Etch layers. The major overlay contributor that may requires additional attention is the Reticle Image Placement Error (IPE). When the inter-layer overlay is considered, controlling the intra-field overlay contribution gets more complicated. In addition to the IPE contribution, the TWINSCANTM lens fingerprint in combination with the exposure settings is going to play a role as well. Generally speaking, two subsequent functional layers have different exposure settings. This results in a (non-reticle) additional overlay contribution.

In this paper, we have studied the wafer overlay correction capability by RegC® in combination with TWINSCANTM intra-field corrections to improve the on product overlay performance. RegC® is a reticle intra-volume laser writing technique that causes a predictable deformation element (RegC® deformation element) inside the quartz (Qz) material of a reticle. This technique enables to post-process an existing reticle to correct, for instance, for IPE. Alternatively, a pre-determined intra-field fingerprint can be added to the reticle such that it results in a straight field after exposure. This second application might be very powerful to correct for instance for (cold) lens fingerprints that cannot be corrected by the scanner itself. Another possible application is the intra-field processing fingerprint. One should realize that a RegC® treatment of a reticle generally results in global distortion of the reticle. This is not a problem as long as these global distortions can be corrected by the TWINSCANTM system (currently up to the third order). It is anticipated that the combination of the RegC® and the TWINSCANTM corrections act as complementary solutions. These solutions perfectly fit into the ASML LithoInsight product in which feedforward and feedback corrections based on YieldStar overlay measurements are used to improve the on product overlay.

9424-57, Session 13

Pattern recognition and data mining techniques to identify factors in wafer processing and control determining overlay error

Auguste Lam, STMicroelectronics (France); Alexander Ypma, ASML Netherlands B.V. (Netherlands); Maxime Gatefait, STMicroelectronics (France); David Deckers, Arne Koopman, Richard J. F. van Haren, Jan Beltman, ASML Netherlands B.V. (Netherlands)

On-product overlay can be improved through the use of context data from the fab and the scanner. Continuous improvements in lithography and processing performance over the past years have resulted in consequent overlay performance improvement for critical layers. Identifying the remaining factors causing systematic disturbances and inefficiencies will further reduce the overlay numbers. The starting point of our work is a novel analysis method that relates fab context (listing the steps from various processing tools that have been applied to a wafer) to the principal fingerprints present in aligned position deviation measurements from the scanner wafer alignment system (referred to as Principal Fingerprint Analysis). The processing tools causing these principal fingerprints can be found by using a contextual analysis on fab data from the Manufacturing Execution System.

STMicroelectronics and ASML are working together on further applying the context pattern mining method. Fab context data, overlay & alignment measurements and relevant loggings from the ASML scanner are being gathered. Mappings between context, fingerprints and alignment & overlay metrology are learned by using techniques from pattern recognition and data mining. We relate structure ('patterns') in the metrology data to relevant contextual factors. These factors can then be moved to the known effects (e.g. the presence of systematic fingerprints from reticle writing error or lens and reticle heating). Hence, we build up a knowledge base of known effects based on data. Outcomes from such an integral ('holistic') approach to litho data analysis may be exploited in a model-based predictive overlay controller that combines feedback and feedforward control (EMLC 2014, B. Le Gratiet).

A first large dataset (~ 0.5 TB) was collected and analyzed. A decision tree analysis revealed the top factors that determine high-order ('non-correctable') overlay error between two layers of 6 different products. A principal fingerprint analysis of overlay metrology of two BEOL (metal) layers showed dominant rotation and dual swirl patterns. In addition, an indicator for the presence of reticle or lens heating was proposed based on measurements collected during scanner reticle alignment. Calculation of the indicator ran on a large number of lots from several layers and products. Relating it to context parameters like illumination mode, dose, reticle transmission factor and lot exposure history helps to identify the layers for which a dedicated lens or reticle heating correction may pay off. Finally, a cluster analysis of overlay parameters and throughput logs may pinpoint additional variations, which can be used to further optimize the process control strategy.

Hence, the available measurements from scanner, fab and metrology equipment are combined to reveal opportunities for further overlay improvement which would otherwise go unnoticed.

9424-58, Session 14

Hybridization of XRF XPS and scatterometry for in-line FinFET process control beyond 10nm

Benoit L'Herron, STMicroelectronics (United States); Robin Hsin-Kuo Chao, IBM Corp. (United States); Kwanghoon Kim, Samsung (France); Bartlet Deprospo, Muthumanickam Sankarapandian, IBM Corp. (United States); Wei Ti Lee, ReVera, Inc. (United States)

The manufacturing process of logic devices from 14nm node and beyond utilizes innovative techniques to satisfy the design rules. The aggressive design and pitch poses unique challenges to in-line metrology methods. The conventional metrology workhorse, CDSEM and CDAFM, has faced increasing difficulties to provide accurate and consistent measurements due to the small half-pitch and the structure complexity, especially with 3D FinFET. Optical metrology technologies, however, are not limited to the small pitches, and can provide complex measurements for patterns and films. Thus an inclination of measurement steps in the process control flow has been observed in recent years.

X-ray Fluorescence (XRF) and X-ray photoelectron spectroscopy (XPS) are two X-ray techniques that are recently being commonly adopted in microelectronics manufacturing. The X-ray techniques makes direct elemental measurements based on emission of electromagnetic waves during shell electron position change in reaction to external radiation. These optical metrology techniques only sensitive to crystalline materials and has no modeling issues, such as parameter correlation, to affect the accuracy and precision of the measurements. However, XRF/XPS are currently not able to extract any profile information directly without post process. Scatterometry, on the other hand, is able to extract full profile information as long as the broad band light penetrates. Due to its inversely problem solving nature, the solution accuracy and precision sometimes suffer from parameter correlation and probing depths when dealing with materials with high extinctive coefficients. Since these two classes of techniques are fast, non-destructive in-line metrology techniques, they are complementary to each other to provide a metrology solution to a complex structure by hybridizing the data.

This paper focused on the synergy between the X-ray and scatterometry, and the benefits to combine the data to improve the accuracy and precision for in-line metrology. Particular examples were given to show that the hybridization addresses the challenge of aggressive patterning. In 10nm node back-end-of-line (BEOL) integration, we show that the hybridized data between the XRF/XPS/OCD provided the closest dimension correlations to TEM results, compared to individual techniques and CDSEM. The other example of the usage is from SiGe channel formation, that the SiGe lost by wet etch process can be measured by XPS, and linked back to fix scatterometry models to break correlations and extract accurate profile information. This work will discuss the X-ray and scatterometry hybrid metrology strategy in both FEOL and BEOL process control in next technology nodes.

This work was performed by the Research and Development Alliance at various IBM Research and Development Facilities

9424-59, Session 14

Grazing-incidence small angle x-ray scattering studies of nanoscale polymer gratings

Manolis Doxastakis, Hyo Seon Suh, Argonne National Lab. (United States) and The Univ. of Chicago (United States); Xuanxuan Chen, The Univ. of Chicago (United States); Paulina A. Rincon Delgadillo, The Univ. of Chicago (United States) and IMEC (Belgium); Lingshu Wan, The Univ. of Chicago (United States); Lance D. Williamson, The Univ. of Chicago (United States) and IMEC (Belgium); Zhang Jiang, Joseph Strzalka, Jin Wang, Argonne National Lab. (United States); Wei Chen, Nicola Ferrier, Abelardo Ramirez-Hernandez, Argonne National Lab. (United States) and The Univ. of Chicago (United States); Juan J. de Pablo, The Univ. of Chicago (United States) and Argonne National Lab. (United States); Roel Gronheid, IMEC (Belgium); Paul F. Nealey, The Univ. of Chicago (United States) and Argonne National Lab. (United States)

Grazing-Incidence Small Angle X-ray Scattering (GISAXS) is emerging as an efficient and accurate structural characterization technique at the nanoscale. GISAXS offers the ability to probe large sample areas, offering three-dimensional information at high detail in a thin film geometry. Furthermore, the potential to probe samples in different environments provides for an attractive technique with unique advantages. This departs significantly from other available methods which are often limited to small areas and/or two-dimensions. In this study we exploit the application of GISAXS to determine the structures formed at each step of LiNe (Liu-Nealey) flow using chemical patterns for directed self-assembly (DSA) of block copolymer (BCP) films.. Experiments conducted at the Advanced Photon Source, Argonne National Laboratory provided characteristic scattering patterns at low incident angles that probed film characteristics at both parallel and normal directions to the surface.

Quantitative analysis of GISAXS scattering patterns at low incident angles allows the interrogation of film structure as the beam penetrates the film and is reflected at the substrate interface. The depth probed is controlled by changes in the incident angle while scattering measured by a two-dimensional detector provides information on the underlying three dimensional structures. Despite the clear advantages that GISAXS offers, accurate models for scattering at nanoscale lengths are needed to extract detailed information of sample characteristics. The assembly of such models requires experiments with precise, high quality samples that will promote further development of both theoretical and computational tools. This is even more important for polymers which present with lower contrast and higher diffusive components. Previous studies support the application of the Distorted Wave Born approximation to model multiple scattering effects in grazing geometry. In addition, in contrast to hard gratings, polymer structures made of crosslinked polystyrene (serving as chemical guiding stripes for DSA of BCP films) present characteristic diffusive components that follow the shape of the patterns. We discuss herein, the application of a numerical approach which allowed us to extract information on the mean shape of the polymer gratings as well as a quantitative description of variations present in the samples. Such detailed information is of paramount importance to our directed self-assembly process which depends on the quality of the underlying chemical patterns. Furthermore, we will present a strategy to couple our approach with molecular simulations providing detailed information of density variations throughout directed assembled diblock copolymer films. Such a combined experimental and simulation effort holds significant promise to advance our ability to characterize patterns at the nanoscale.

9424-60, Session 14

Evaluation of laboratory x-ray sources for high-throughput CD-SAXS

Daniel F. Sunday, Donald Windover, Wen-li Wu, R. Joseph Kline, National Institute of Standards and Technology (United States)

The ITRS roadmap states that there is an unmet need for high throughput dimensional metrology of next generation devices. These devices will have critical dimensions less than 10 nm and contain multiple components with complex three dimensional shapes. This combination presents considerable challenges to conventional process metrology methods. We will discuss an in-depth study of CD-SAXS and its potential for high throughput dimensional metrology using industry-relevant samples. We will compare results obtained with ultra-low noise detectors to conventional detectors. We have used a single-photon counting detector to conduct a detailed statistical study to determine how fast CD-SAXS measurements can be made with current x-ray sources and to make absolute intensity measurements to determine the number of photons required for a given measurement accuracy. We have also conducted a study to determine the minimum number of incidence angles required to obtain three-dimensional profile fits to complex line patterns and will present the results of a modeling study of the relationship between uncertainty and amount of data collected. We will conclude with a discussion of new, higher brightness X-ray sources and the potential near term improvements in CD-SAXS measurement time.

9424-61, Session 14

Signal response metrology (SRM): a new approach for lithography metrology

Stilian Pandev, KLA-Tencor Corp. (United States); Fang Fang, Young Ki Kim, Jamie Tsai, Alok Vaid, Lokesh Subramany, Chen Li, GLOBALFOUNDRIES Inc. (United States); Dimitry Sanko, Vidya Ramanathan, Ren Zhou, Kartik Venkataraman, KLA-Tencor Corp. (United States); Ronny Haupt, KLA-Tencor Germany (Germany); Lester Wang, GLOBALFOUNDRIES (United States)

Critical Dimension uniformity (CDU) requirements at 20nm and newer nodes have challenged the precision limits of CD-SEM metrology conventionally used for scanner qualification and in-line focus/dose monitoring on product wafers. Optical CD metrology has consequently gained adoption for these applications because of its superior precision, but has faced hurdles of long time-to-results and limited robustness to process variation. Both of these hurdles are due to the limitations imposed by geometric modeling of the photoresist (PR) profile as required by conventional RCWA-based (rigorous coupled wave analysis) scatterometry. Signal Response Metrology (SRM) is a new technique that obviates the need for geometric modeling by directly correlating focus, dose, and CD variation to spectral response of a scatterometry tool. Consequently, it offers superior robustness to process variation for focus/dose monitoring while shrinking the time to set up a new measurement recipe from days to hours. This work describes the fundamental concepts of SRM and the results of its application to lithography metrology and control. These results include lead time to results and performance data on focus, dose and CD measurements performed on real devices and on design rule metrology targets.

SRM uses one or more focus/exposure matrix (FEM) wafers that cover a wide process range to train a model to correlate scatterometry spectral response to scanner focus and dose variations. The only inputs required are the programmed scanner focus/dose values and CD-SEM data—no information of the grating and film stack are required. This trained model can then be used to measure focus, dose, and CD on product wafers at the same process step. We have developed a methodology to parse spectral response to focus and dose into “signal components” that can be plotted in a fashion similar to Bossung plots using CD data (see Figure 1). From these

"signal Bossung plots", we can determine best focus on FEM wafers.

Since layers beneath the PR grating also contribute to the spectral response, variations in these underlayers also need to be accounted for. In conventional scatterometry, the correlations from underlayers are removed by using multiple signal acquisition pathways and/or feed forward of information from previous process steps. However, using multiple subsystems adds to the modeling complexity and feed forward is subject to error propagation. SRM deals with underlayer variations by using a differential method rather than an additive one. Spectra acquired from multiple adjacent targets that have identical underlayers but different grating pitches/CD are compared to determine the spectral response to grating vs underlayers. The spectral response to underlayers is filtered out, thus enhancing sensitivity to focus and dose, while also mitigating the impact of non-scanner related process variation on focus/dose metrology. An example of the benefits of the differential technique is shown in Table 1. Another example of the benefit of SRM is shown in Figure 2, wherein a comparison between PR CD of a device SRAM feature measured by CD-SEM vs SRM is shown. Normally, PR pattern for actual device SRAM is too complex to be modeled by RCWA, and therefore has not been measured by scatterometry. This example shows that using SRM, modeling complexity is no longer a limitation for optical metrology of litho layers.

9424-62, Session 14

A parametric study of TSOM method

Ravikiran Attota, HyeongGon Kang, National Institute of Standards and Technology (United States)

Through-focus scanning optical microscopy (TSOM) method shows ability to identify three-dimensional shape variations of nanoscale targets with nanometer scale measurement resolution using ubiquitous conventional optical microscopes [1]. Innovative non-mechanical scanning methods have also been developed increasing the stability of the system [2]. Since it is a differential method, aberrations (or imperfect optical conditions) usually do not have significant effect on the measurement process (and hence robust). An imperfect optical microscope is generally adequate for analyzing nanoscale 3-D shape variations, especially as a process or quality control method in an industrial setup. For the same reason the TSOM method does not rely on optical simulations making the measurement process less cumbersome. A practical process evaluation method for truly-3D shaped high-aspect-ratio (HAR) targets of about 1100 nm deep trenches was demonstrated at the 2014 SPIE Advanced Lithography conference [3] by making use of an experimentally developed TSOM image library (without using optical simulations).

However, it is important to optimize the conditions to get the best out of the TSOM method. The TSOM image pattern and sensitivity of the method depend on measurement conditions. The current paper studies the parameters using measurements and simulations. The effect of parameters such as illumination numerical aperture (NA), collection NA, wavelength, focus step height, and camera pixel size will be presented. Effect of optical and illumination aberrations on the sensitivity will be presented. Optimization of the parameters and some practical tips for successful TSOM analysis will also be presented.

1. Ravikiran Attota and Ronald Dixson, "Resolving three-dimensional shape of sub-50 nm wide lines with nanometer-scale sensitivity using conventional optical microscopes," Applied Physics Letters, 105, 043101. http://dx.doi.org/10.1063/1.4891676

2. Maxim Ryabko, Sergey Koptyaev, Alexander Shcherbakov, Alexey Lantsov, and S. Y. Oh, "Motion-free all optical inspection system for nanoscale topology control," Optics Express, 22, pp. 14958-14963 (2014), http://dx.doi.org/10.1364/OE.22.014958

3. Ravikiran Attota, Mike Kang, Keana Scott, Richard Allen, Andras Vladar, Bin Ming and John Kramar, "3D Shape Analysis of HAR Targets Using TSOM: A Correlation Study Using FIB Cross-sections ," SPIE Adv. Litho. Feb 2014, San Jose.

9424-63, Session 15

The development and advantages of helium ion microscopy for the study of block copolymer nanopatterns

Alan P. Bell, Trinity College Dublin (Ireland); Ramsankar Senthamaraikannan, Tandra Ghoshal, Atul B. Chaudhari, Michael A. Morris, Univ. College Cork (Ireland)

Helium ion microscopy (HIM) has been used to study the nanopatterns formed in block copolymer (BCP) thin films. Owing to its' small spot size, minimal forward scattering of the incident ion and reduced velocity compared to electrons of comparable energy, HIM provides pattern information and resolution not attainable with other commercial microscopic techniques.

In order to realise the full potential of BCPs and the resultant formation of high density ultra-small features, the dimensions and geometry of these BCP materials will need to be accurately characterised throughout all stages of pattern formation, development and ultimately pattern transfer. The preferred BCP pattern inspection techniques of choice to date have been AFM and SEM. AFM suffers from poor lateral resolution and resolving individual polymer blocks using SEM is difficult. SEM suffers from reduced resolution when a more surface sensitive low accelerating voltage is used and low surface signal when a high accelerating voltage is used. In addition to these drawbacks, SEM typically requires the use of a conductive coating on a lot of insulating specimens. This coating reduces surface detail as well as increasing the dimensions of coated features. AFM is limited by the dimensions of the probe tip and a skewing of lateral dimension results. This can be eliminated through basic geometry for large sparse features, but when dense small features need to be characterised AFM is not a reliable technique. With this in mind, BCP inspection by HIM can offer greater insight into block ordering, critical dimensions and line edge roughness(LER) (LER is a critical parameter in the semiconductor industry and much is known about enhanced edge contrast in HIM allowing quantifiable characterization) compared to both AFM and SEM.

In this work we will demonstrate the resolution capabilities of HIM using various BCP systems where lamella and cylinder features are realised. Imaging of BCP of low MW will be presented challenging the attainable resolution of the technique. Further, studies of BCPs with blocks of similar chemistry will be presented demonstrating the superior chemical contrast compared to SEM. HIM excels as a BCP inspection tool in four distinct areas. Firstly, HIM offers higher resolution at standard imaging conditions than SEM. This increased resolution is important for edge definition in CD measurement. Secondly, the signal generated from He+ is more surface sensitive and enables visualisation of features that cannot be resolved using SEM. Thirdly, superior chemical contrast enables the imaging of unetched samples with almost identical chemical composition. Finally dimensional measurement accuracy improvements and trade-offs with HIM for lithographic materials.

9424-64, Session 15

Potential Application of Tip-Enhanced Raman Spectroscopy (TERS) in Semiconductor Manufacturing

P.Y. Hung, Sematech (United States); Thomas O'Loughlin, Texas A&M Univ. (United States); Aaron Lewis,, Rimma Dechter, Nanonics Imaging Ltd. (Israel); Martin Samayoa, Sematech (United States); Sarbajit Banerjee, Texas A& M University (United States); Erin Wood, Angela R. Hight Walker, NIST (United States)

This work discusses the potential metrology application of TERS in semiconductor manufacturing and it also addresses approaches to bridge challenging gap areas such as the lack of reproducible tips and a traceable standard. Two potential areas for TERS application will be presented:

process/ integration development and defect metrology. The former is likely to focus on the R&D stage, and the latter has potential for high volume manufacturing applications. Strained Si monitoring is one of the well-studied applications of Raman spectroscopy for process or integration development. Strained silicon in the channel area to enhance carrier mobility has been of great interest for the semiconductor industry for the past decade. Micro Raman has been employed to map and monitor the strain profile and TERS has been shown to image strain with a much improved 50 nm resolution. In contrast, the application of Raman and TERS for defect metrology is relatively underexplored. Since TERS allows for strong signal amplification and therefore has a lower detection limits and coupled with chemical identification. As CMOS scaling continues, there is an imminent need to monitor and identify defects down to sub 30 nm dimensions. Currently, defect characterization routinely done by energy dispersive X-ray spectroscopy (EDS) is inefficient for monitoring sub 30 nm defects. Furthermore EDS only provides elemental information, and thus cannot provide precise identification of carbonaceous species such as photo-resists or air borne contamination. To evaluate this application, we used commercial polystyrene/ latex nanoparticle to mimic sub 30 nm defect. Our result shows micro Raman does not collect a discernible signal, however the surface-enhanced Raman has a clear spectra.

Further development is needed to develop TERS as a metrology tool. The primary concern is the lack of reliable and reproducible tips. In addition, the absence of a traceable standard for equipment and measurement verification needs to be addressed. Johnson et al. has proposed a scheme for constructing highly reproducible tips. The scheme is compatible with large scale manufacturing. This work shows progress from our team, which includes optimization in the hard-mask removal step using electro-chemical etch. For a traceable standard, FINFET manufacturing process was used to produce arrays of strained SiGe lines with a targeted line-width of 33 nm and pitch of 288 nm. Our Raman mapping data from the traceable standard demonstrates the superior spatial resolution of TERS as compared to micro Raman.

9424-75, Session 15

Virtual overlay metrology for fault detection supported with inline metrology and machine learning

Hong-Goo Lee, SK Hynix, Inc. (Korea, Republic of); Emil Schmitt-Weaver, ASML Netherlands B.V. (Netherlands); Min-Suk Kim, Sang-Jun Han, Myoung Soo Kim, Won-Taik Kwon, Sung-Ki Park, SK Hynix, Inc. (Korea, Republic of); Kevin Ryan, Thomas Theeuwes, Kyu-Tae Sun, Young-Wan Lim, Daan Slotboom, Michael Kubis, Jens Staecker, ASML Netherlands B.V. (Netherlands)

While semiconductor manufacturing moves toward the 7nm node, an increased emphasis has been placed on reducing the influence known contributors have toward the on product overlay budget. With a machine learning technique known as function approximation, we use a neural network to gain insight to how known contributors, such as those collected with scanner metrology, influence the on product overlay budget. The result is a sufficiently trained function that can approximate overlay for all wafers exposed with the lithography system. As a real world application, inline metrology can be used to measure overlay for a few wafers while using the trained function to approximate overlay vector maps for the entire lot of wafers. With the approximated overlay vector maps for all wafers coming off the track, a process engineer can redirect wafers or lots with overlay signatures outside the standard population to offline metrology for excursion validation. With this added flexibility, engineers will be given more opportunities to catch wafers that need to be reworked, resulting in improved yield. The quality of the derived corrections from measured overlay metrology feedback can be improved using the approximated overlay to trigger, which wafers should or shouldn't be, measured inline. As a development or integration engineer the approximated overlay can be used to gain insight into lots and wafers used for design of experiments (DOE) troubleshooting. In this paper we will present the results of a case study that follows the machine learning function approximation approach to data analysis, with production overlay measured on an inline metrology system at SK hynix.

9424-101, Session 15

Further advancing the throughput of a multibeam SEM

Dirk Zeidler, Carl Zeiss Microscopy GmbH (Germany)

Multiple electron beam SEMs enable detecting structures of few nanometer in diameter at much higher throughputs than possible with single beam electron microscopes at comparable electron probe parameters. Although recent multiple beam SEM development has already demonstrated a large speed increase, higher throughputs are still required to match the needs of many semiconductor applications. We demonstrate the next step in the development of multi-beam SEMs by increasing the number of beams and the current per beam. The modularity of the multi-beam concept ensures that design changes in the multi-beam SEM are minimized.

Conference 9425: Advances in Patterning Materials and Processes XXXII

Monday - Thursday 23–26 February 2015

Part of Proceedings of SPIE Vol. 9425 Advances in Patterning Materials and Processes XXXII

9425-1, Session 1

Recent progress on multipatterning *(Keynote Presentation)*

Hidetami Yaegashi, Tokyo Electron Ltd. (Japan); Kenichi Oyama, Shohei Yamauchi, Arisa Hara, Sakurako Natori, Masatoshi Yamato, Noriaki Okabe, Tokyo Electron AT Ltd. (Japan)

Fine-patterning for Semiconductor manufacturing has been driven by optical lithographic technique historically. Although the delay of EUV tool for HVM has been concerned, continuous down scaling is going on steadily beyond the resolution limitation of 193nm-immersion technique. Double patterning process has been firstly adopted in 30nm node device of memory device, and evolved step by step from SADP, SAQP to SAOP. Self-Aligned Multiple-Patterning (SAMP) with 193-immersion is getting most promising technology for further downwards scaling at the present. On the other hand, paradigm in design area changed to highly regular layout style using Gridded Design Rules (GDR). For the fabrication of Single directional layout, any related process tools, such as Lithography, Etching, Deposition and Cleaning have to be harmonized smartly, and patterning capability also will be needed to observe from lithographic viewpoints. Especially, pattern fidelity on mandrel pattern in SAMP might be controlled precisely. One of important process step to maintain pattern fidelity is LER suppression on resist pattern and improvement pattern transfer fidelity through RIE, because any pattern performance transfer to pitch split secondary spacer pattern.

9425-2, Session 1

Continued CMOS scaling through exploratory materials research *(Keynote Presentation)*

Todd R. Younkin, Intel Corp. (United States)

The continued scaling of complex device geometries is driving the need for novel lithographic techniques, self-alignment strategies, and thin film deposition and etch strategies with atomic-layer precision. In this context, novel materials play a key and enabling role. Bringing novel materials to high-volume manufacturing requires a highly coordinated research and development pipeline.

With the realization that overlay management will limit scaling long before devices and interconnects fail to perform intrinsically, the talk will first outline how extreme UV lithography (EUV) and directed self-assembly (DSA) can simplify patterning by reducing the number of masks and overlay steps. Novel EUV resist materials require amplification mechanisms that overcome acid blur and new strategies to improve shot noise limitations and mechanical stability. For DSA, novel block co-polymers are needed with a higher chi parameter to yield tighter pitch and improved roughness.

Thin film deposition with atomic-layer precision is derived from the chemical nature of the precursors and co-reactants. A wide variety of materials can be accessed through judicious choice of precursor and co-reactants and the ability of these molecules to recognize complementary chemical functionality on a surface to enable self-alignment of thin films.

9425-3, Session 2

Towards 11nm half-pitch resolution for a negative-tone chemically-amplified molecular resist platform for extreme-ultraviolet lithography

Alex P. Robinson, Andreas Frommhold, The Univ. of Birmingham (United Kingdom); Alexandra L. McClelland, Irresistible Materials Ltd. (United Kingdom); Dong Xu Yang, The Univ. of Birmingham (United Kingdom); John Roth, Nano-C, Inc. (United States); Richard E. Palmer, The Univ. of Birmingham (United Kingdom); Yasin Ekinci, Paul Scherrer Institut (Switzerland)

In order to enable continued steady progress in semiconductor device shrinkage, new lithography technologies have become necessary. According to the International Technology Roadmap of Semiconductors (ITRS) EUV lithography is one of the leading candidates to replace current manufacturing processes. However, unresolved issues still remain - such as low available source power. The move to a much shorter wavelength for patterning has also made the development of new photoresist platforms necessary, a challenging task in itself.

While significant research into to new materials has been undertaken, to date no suitable resist has emerged that meets all the requirements as laid out in the semiconductor roadmap for 2016, when EUVL is scheduled to be introduced into high volume manufacture. In addition to fulfilling the target for 2016, new material platforms should also have the promise to meet the outlined specifications beyond 2016 to ensure a useful lifespan for next generation lithography.

We are developing a molecular resist platform for EUV application. We've previously demonstrated that the system holds promising properties that put it close to the RLS targets for 2016 [1]. Here we report on recent progress in improving the resolution and reducing the line edge roughness (LER) of our material through materials synthesis and resist formulation improvement, and via process optimization. We show patterning at the Paul Scherrer Institute (PSI) interference lithography tool down to 11 nm half-pitch (hp) and examples of exposures that yielded LER values as low as 1.5 nm at 25 nm hp. In addition we report initial exposures of the resist system at the Berkeley Micro Exposure Tool (BMET), with resist modulation seen at 14 nm hp, and identify some performance differences for our resist system between the different EUV exposure platforms together with discussing potential strategies to mitigate the differences.

[1] A. Frommhold, D.X. Yang, A. McClelland, X. Xiang, Y. Ekinci, R.E. Palmer, A.P.G. Robinson, Journal of Micro-Nanolithography MEMS and MOEMS 12 (2013) 033010.

9425-4, Session 2

Recent progress of negative-tone imaging with EUV exposure

Toru Fujimori, EUVL Infrastructure Development Ctr., Inc. (Japan)

Photo resist material researchers have been studied Chemical Amplified Resist (CAR) for a long time, and CAR is still one of the strongest candidates for EUV lithography realization for sub-10 nm generation. Recently, some researchers concern about the limitation of CAR's performance, which mean, resolution, sensitivity and line width roughness (LWR) trade off. New chemistry and new resist materials will be strongly required, but CAR still

has the potential of the performance. CAR is usually developed by water based developer, like 2.38% tetramethylammonium hydroxide (TMAH), called positive-tone development (PTD). It is very useful for semiconductor industry, because TMAH is a standard developer for every lithography process. However, the issue of water based developer is to cause resist film swelling, which leads to poor LWR performance and pattern collapse. It is very difficult to resolve these issues by using water based developer system. The other hand, negative-tone imaging (NTI, using organic solvent based developer) provided low swelling and smooth dissolving behavior. So, negative tone imaging with EUV exposure (EUV-NTI) has huge advantages for the performance, especially for improving LWR, which will be expected to resolve RLS trade off. Also, NTI system has been already introduced to manufacturing with ArF exposure. So, it seems not so difficult to use EUV-NTI for manufacturing.

This paper describes the recent progress of negative-tone imaging with EUV exposure comparing with positive-tone development. Novel chemical amplified resist materials for EUV-NTI have been studied to improve LWR and sensitivity. Some of the results with NXE3100 scanner will be shown. Basically, NTI has better performance than PTD, and one of the impact results was 60% higher sensitivity in comparison with PTD to be "single mJ/cm2" with keeping LWR performance. Also, process conditions of EUV-NTI, like pre applied bake (PAB) temperature, post exposure bake (PEB) temperature, development procedure and rinse procedure, are very effective for improving lithographic performance. By using "Mild developer", less solubility solvent, provided around 30% higher sensitivity with keeping LWR performance, also pattern collapse margins were improved with after development rinse by using organic solvent based rinse. Lithographic performance with NXE3100 scanner will be reported.

9425-5, Session 3

The effect of resist dissolution process on pattern formation variability: an in situ analysis using high-speed atomic force microscopy

Julius Joseph S. Santillan, Motoharu Shichiri, Toshiro Itani, EUVL Infrastructure Development Ctr., Inc. (Japan)

Extreme ultraviolet (EUV) resist lithography targets on resolution, line width roughness / line width roughness or LWR/LER and sensitivity (RLS) are being pushed towards fine patterning of sub-10 nm half-pitch (hp) lines and spaces (L/S) and beyond. Patterning materials / processes play a significant role in obtaining such targets. To meet this challenge, a number of groups have focused on breaking the often-reported RLS trade-off relationship through new-concept materials and optimization of present material platforms are being proposed. The application of alternative processes is also being considered. [1]

The authors have focused on a more fundamental approach through further understanding of the development or dissolution process where the first instance of physical formation of such fine patterns occurs. Specifically, the authors proposed the use of an in-liquid high-speed atomic force microscope (HS-AFM) which allows the in situ analysis of pattern formation during dissolution. [2]

Recent research activities involving this original technique have focused on analysis possibilities from the enormous amounts of data obtained. An intensive review of acquired results up to present, point to the possibility of analyzing; "swelling"[3] change of exposed resist film (during dissolution), pattern critical dimension variation (at "through-process": dissolution, rinse, dry), sidewall (LWR/LER) and pattern top surface roughness variation (at "through-process"), particle size analysis of resist dissolution units, etc. Among these, the formation of LWR/LER during dissolution will be the focus of this paper.

For these experiments, the EIDEC standard resist (ESR1), a positive-tone EUV resist composed of a hybrid polyhydroxystyrene(PHS)-methacryl polymer, onium salt type photoacid generator (PAG) and acid quencher was utilized at 50nm film thicknesses. Patterning was done using the in-house 0.3NA EUV small field exposure tool (SFET). Optimized post application and post exposure bake conditions were applied and development was carried out using a typical aq. 2.38wt% TMAH developer. The HS-AFM was used at a scanning area of 1000x1000 nm (at 400x400 pixels) with a speed of 2 s/image.

Figure 1 shows HS-AFM obtained images used in the in situ pattern LWR/LER formation analysis for a 32nm L/S pattern on the ESR1 resist at a Zthreshold 50% of the pattern height, which is ~25nm from the wafer surface. It is noteworthy that the exposed areas of the ESR1 resist (spaces between lines) exhibit swelling in the first 10s of dissolution. At 20s since the start of dissolution, the dissolved area does not reach the set Zthreshold, thus no values are obtained. At around 44s, the dissolved spaces reach the set Zthreshold. Measured results suggest a trend of decreasing LWR as dissolution time advances. However, as further extending this dissolution time may result in line cuts as seen at the top left side of the image (at 58 s), a possible increase in LWR is expected. During the conference, the formation of LWR (from the beginning until end of the dissolution process) will be presented in detail. Discussions will also be made on how this formation mechanism changes with EUV resists of relatively improved LWR values.

9425-6, Session 3

XAS photoresists electron/quantum yields study with synchrotron light

Alessandro Vaglio Pret, KLA-Tencor/ ICOS Belgium (Belgium); Peter de Schepper, Terje Hansen, IMEC (Belgium); Angelo Giglia, Istituto Officina dei Materiali (Italy); Kenji Hoshiko, JSR Micro N.V. (Belgium); John J. Biafore, KLA-Tencor Texas (United States)

The main roadblock for EUV lithography to be successfully adopted by industries for high-volume manufacturing is severe lack of power. Actinic source power has increasing, but much slower when compared to Moore's law. One way to help mitigate this problem is to optimize the photoresist by increasing both absorbance and quantum yield. The latter represents the ratio between generated acids and absorbed photons. In EUV, the quantum yield is mainly limited by the number of ionized electrons, or electron yield, which can be generated after a photo absorption event.

While absorbance is relatively easy to measure or calculate, yields are extremely difficult to quantify, and the debate on upper limits is far from settled. In this paper, we present how, using synchrotron light with tunable energy, we directly measured the number of generated electrons per incident photon for ArF, KrF and EUV photoresists using X-ray Absorption Spectroscopy (XAS, figure 1). Spectra were collected at the Elettra synchrotron, at the BEAR beamline. As can be seen from the graph, the EUV material (dark-blue line) scores much higher compared to the ArF (green line) and the KrF (red line) materials, with a visible peak around 13.5nm. It is also evident from the plot that the majority of electrons are generated by the backbone polymer itself (EUV pol., light-blue curve), and not by the additives. Interesting to notice a second electron peak around 60nm wavelength, mainly related to K, L2 and L3 peaks of EUV PAGs and quenchers (H, C and O compounds), completely absent in the KrF, ArF material, and in the EUV backbone polymer.

Convolving the spectra with the expected radiation band at wafer level for the NXE:3100 EUV scanner installed at IMEC (figure 2) it is possible to estimate the number of generated electrons per absorbed photons – or electron yield – as function of wavelength. Knowing the electron yield allowed us to better model quantum yields for the materials we analyzed using stochastic simulation methods.

9425-7, Session 3

Inhomogeneity of PAGs in hybrid-type EUV resist system studied by molecular-dynamics simulations for EUV lithography

Minoru Toriumi, Toshiro Itani, EUVL Infrastructure Development Ctr., Inc. (Japan)

As feature sizes on semiconductor devices continue to get smaller, resist materials are required to meet the challenging requirements for patterning sub-20 nm features, sizing dose of less than 20 mJ/cm2 and line width roughness (LWR) below 2 nm. It is very difficult to break through this RLS tradeoff. We consider the inhomogeneity of resist components in resist films influences these resist properties and that the information on the inhomogeneity should be valuable to control it and to break through the tradeoff. However there are no experimental studies to measure directly the inhomogeneity in the resist film and identify its physical and chemical properties. Therefore we have started to study the inhomogeneity of resist components in resist films using molecular-dynamics (MD) simulation.[1] The inhomogeneity of locations and motions of PAGs in the resist film was shown and was affected by the physical and chemical properties of PAGs, and free volumes of polymers.

In this paper, a hybrid-type resist film was studied using MD simulation and the effects of polymer were also analyzed to study the inhomogeneity. To simulate the resist film, 3-dimensional periodic boundary condition was applied to construct the amorphous models consisting of two hybrid-type polymers and seven PAGs in a basic cell of ca. 3.5 nm. Evaluated polymer was a hybrid-type polymer composed of phenolic and methacrylic monomer units with the molecular weight of 10,000. Evaluated PAG was triphenylsulfonium nonaflate and its composition was 20 wt% to 100 % polymer weight. MD simulations of the amorphous models were performed for several nanoseconds under the one atm and 300 K conditions of isothermal-isobaric ensemble (NPT) where numbers (N), pressure (P) and temperature (T) were constantly conserved after relaxation procedures such as canonical ensemble (NVT) where N, volume (V) and T were conserved and minimization of total energy. Configurations were simulated from the 10 initial conditions larger than two or three of conventional MD procedures in order to understand clearly its effect of creating initial conformations.

The simulated results shows directly the inhomogeneity of PAGs located in resist films. The average distance of PAG pairs is 0.64 nm and is larger than the distance of pure PAGs (without polymer), 0.37 nm, which was determined from radial distribution of pure PAGs only obtained by the simulation of PAGs only exist in a basic cell.

PAG shows inhomogeneity of not only the localizations but also the motions of PAGs. After the analysis on seventy PAGs of the simulations, the average trajectory volume of PAG anions is 1.7 times larger than that of PAG cations. It can be elucidated by the physical and chemical properties of PAG ions and the interactions between the neighboring PAGs and polymers.

In the conference, interactions between PAGs and polymers will be discussed in details using 3D-graphics by Mathematica.

9425-8, Session 4

Advanced patterning approaches based on negative-tone development (NTD) process for further extension of 193nm immersion lithography

Michihiro Shirakawa, Naoki Inoue, Hajime Furutani, Kei Yamamoto, Akiyoshi Goto, Mitsuhiro Fujita, FUJIFILM Corp. (Japan)

With the delay of extreme ultraviolet lithography (EUVL) application to high volume manufacturing (HVM), several attempts for the extension of 193 nm immersion lithography have been widely studied.

Among the numerous candidates, NTD (Negative Tone Development) process now occupies an important position for HVM of the 20 nm and 14 nm nodes devices. NTD process is a method for obtaining a negative-tone reversal pattern by developing with an organic solvent. NTD process allows a good lithography performance at specific patterns such as narrow trenches and contact holes because of the high optical contrast with bright mask. Lower risk of defects due to the fact that NTD process does not use any cross-linking reaction is also one of the factors that it has been applied to HVM.

Given the situation that EUVL is facing difficulties towards the HVM yet, further extension of NTD process is desired for below 14 nm nodes devices.

In this paper, we will introduce two techniques for the further evolution of NTD process. One is ACCEL (Advanced Chemical Contrast Enhancement Layer) process that can improve the lithographic performance and the other is DTD (Dual Tone Development) process that can shrink patterning pitch.

ACCEL is an additionally provided layer which is coated on a surface of NTD resist film before exposure and removed by NTD developer. ACCEL is a technique that enhances the acid distribution contrast. In fact, lithographic performances such as exposure latitude and DOF improved by about 20% by applying ACCEL to a conventional NTD resist. We estimate that material transfer between the resist layer and the ACCEL layer is the cause of the contrast improvement. Detail mechanism will be discussed in the presentation.

DTD process is one of the simplest pitch shrink method which is achieved by repeating PTD and NTD process. Feasibility study of 28nm half-pitch contact hole patterning has been demonstrated so far. However, Exposure latitude margin and CDU performance were not sufficient for applying DTD to HVM. In this paper, we will show the investigation of DTD pattern formation mechanism and efforts for performance improvement by additional processes.

9425-9, Session 4

Optimizing performance in cross-linking negative-tone molecular resists

Richard A. Lawson, Hannah Narcross, Brandon Sharp, Georgia Institute of Technology (United States); Jun Sung Chun, SEMATECH Inc. (United States) and SUNY College of Nanoscale Science and Engineering (United States); Mark Neisser, SEMATECH Inc. (United States); Laren M. Tolbert, Clifford L. Henderson, Georgia Institute of Technology (United States)

Negative tone resists have generally received less attention than positive tone resists for high volume manufacturing lithography. This is due to a number of reasons including significant swelling in many early negative tone resists and difficulty in controlling the extent of reaction. Continued reduction in feature sizes has increased interest in negative tone resists because of the potential for higher optical image contrast in bright field imaging and the need for higher resist mechanical strength to prevent pattern collapse during development and drying. At the 2014 SPIE Advanced Lithography conference, we reported on sub-20 nm EUV imaging using a negative tone epoxide functionalized molecular resist.1 In less than a year, we improved the EUV resolution of a single resist molecule (4Ep in Figure 1) from greater than 30 nm to 18 nm while also improving the LER simply through the development and addition of novel polymerization control additives which control the extent of cross-linking and modify the resist contrast. Since then, we have focused on optimizing performance in this class of materials by further development of control additives and by the synthesis of a series of new resist molecules beyond 4Ep, some of which are shown in Figure 1. These new compounds allow for a variety of comparisons which provide further insight into controlling and improving patterning performance. Some of these comparisons include: the effect of the number of functional groups on the molecule, the effect of the glass transition temperature of the resist, and the effect of multiple different cross-linking mechanisms such as epoxide-phenol cross-linking compared to epoxide homopolymerization. Certain structural moieties appear to significantly modify properties such as film quality, film adhesion, glass transition temperature, and EUV sensitivity. We have also synthesized some resist molecules that have aqueous base solubility, and these allow for direct comparison of the effect of organic solvent versus aqueous alkaline solution development. The effect of the polymerization control additives are similar in each resist, but the magnitude of the effect can vary significantly. Figure 2 shows initial EUV patterning performance for some of these resists. This paper will provide an overview of some of our efforts into optimizing performance in these systems and share the insights gained thus far into which material properties have the biggest effect on patterning performance and why.

9425-10, Session 4

Process variation challenges and resolution in the negative-tone develop double patterning for 20nm and below technology node

Sohan S. Mehta, Lakshmi K. Ganta, Craig D. Higgins, Vikrant K. Chauhan, Burcin Erenturk, Lokesh Subramany, Chien-Hsien S. Lee, Hui Peng Koh, Paramkit Singh, David R. Cho, GLOBALFOUNDRIES Inc. (United States)

Immersion based 20nm technology node and below becoming very challenging to chip designers, process and integration due to multiple patterning to integrate one design layer . Negative tone development (NTD) processes have been well accepted by industry experts for enabling technologies 20 nm and below. 193i double patterning is the technology solution for pitch down to 80 nm. This imposes tight control in CD variation in double patterning where design patterns are decomposed in two different masks such as in litho-etch-litho etch (LELE). CD bimodality has been widely studied in LELE double patterning [1]. A portion of CD tolerance budget is significantly consumed by variations in CD in double patterning.

The objective of this work is to study the process variation challenges and resolution in the Negative Tone Develop Process for 20 nm and Below Technology Node. This paper describes the effect of dose slope on CD variation in negative tone develop LELE process. This effect becomes even more challenging with standalone NTD developer process due to q-time driven CD variation .We studied impact of different stacks with combination of binary and attenuated phase shift mask and estimated dose slope contribution individually from stack and mask type.

In order to meet the minimum insulator requirement for the worst case on wafer the overlay and CDU budget margins have slimmed. Besides the litho process and tool control using enhanced metrology feedback, the CD variation has other dependencies too. Color balancing between the two masks in LELE is helpful in countering effects such as iso-dense bias, and pattern shifting. Dummy insertion and the improved decomposition techniques [2], for example, using multiple lower priority soft constraints can help address color balancing. Innovative color aware routing techniques [3] can also help with achieving more uniform density and color balanced layouts. In this work we also explore the CDU correlation with layout decomposition and color balancing. Detail simulation and resist modeling study will be carried out to understand theoretical aspect. Direct correlation with normalized yield, reliability impact and future needs for LELE specific process control will be discussed

9425-12, Session 4

Effect of molecular resist structure on glass transition temperature and lithographic performance in epoxide functionalized negative-tone resists

Hannah Narcross, Richard A. Lawson, Brandon Sharp, Georgia Institute of Technology (United States); Jun Sung Chun, SEMATECH Inc. (United States) and SUNY College of Nanoscale Science and Engineering (United States); Mark Neisser, SEMATECH Inc. (United States); Laren M. Tolbert, Clifford L. Henderson, Georgia Institute of Technology (United States)

Although high volume manufacturing is dominated by positive tone resists, negative tone resists have received more interest recently as the performance requirements for EUV resists continue to become more challenging. Some of the best performance in negative tone EUV resists has been obtained using small molecules (i.e. molecular resists) for the base resist resin as opposed to polymers. Our group has shown sub-20 nm resolution with good sensitivity in a four-functional molecular resist with novel polymerization control additives.1 To improve performance even further, a fundamental understanding of the relationships between the physical properties of resist materials and their lithographic performance is critical for the rational design and optimization of negative tone molecular resists. One advantage of using small molecules as the base resist is the opportunity to create a series of molecules with equivalent functionality but with systematically varying structural moieties. This can allow for direct comparison of the effect of such moieties on performance. It also allows for the creation of a series of compounds possessing different glass transition temperatures (Tg). The effect of Tg on patterning performance can then be studied. We have synthesized an analogous series of di-functionalized epoxide resists differing in their molecular glass cores in order to investigate the effect of the differing structural moieties and resist Tg on imaging performance. Some of the molecules in this series are shown in Figure 1. Initial studies have shown the resist structure can modify the Tg of the un-crosslinked resist by well over 30 °C. The materials all show similar deep-ultraviolet (DUV) imaging doses, but have very different contrast ratios from very high to very low. Some variations in the series show very different EUV sensitivities than might be expected from DUV patterning data due apparently to the effect some structural groups on electron capture during EUV exposure. Initial EUV patterning for one of the resists is shown in Figure 2 which shows 20 nm 1:1 line:space patterns. Physical properties, lithographic metrics, and imaging data will be compared this series of resists so that conclusions regarding the effect of different structural groups and the effect of resist Tg relative to thermal processing conditions can be made in terms of negative tone molecular resist EUV performance.

9425-81, Session 4

Point-of-use filtration strategy for negative-tone developer in extended immersion and extreme-ultraviolet (EUV) lithography

Lucia D'Urzo, Entegris GmbH (Germany); Philippe Foubert, IMEC (Belgium); Harold Stokes, Dainippon Screen Deutschland GmbH (Germany); Yan Thouroude, Dainippon Screen Deutschland GmbH (Belgium); Annie Xia, Entegris, Inc. (United States)

Negative tone development (NTD) has drammatically gained popularity in 193nm dry and immersion lithography, due to superior imaging performance.

Several comparative research works between positive tone development and negative tone development have been carried out for both memory and logic devices and have been showing superiority of NTD in terms of imaging quality [1, 2 and 3].

The introduction of NTD, appealing for extending 193nm lithography capability, is becoming a strong requirement for extreme ultraviolet (EUV) lithography.

Popular negative tone developers are organic solvents such as n- butyl acetate (n-BA), aliphatic ketones, or high-density alcohols such as Methyl Isobutyl Carbinol (MIBC).Their leaching behavior on common polymeric membranes calls for improvements on traditional point-of-use (POU) filtration strategy. In this work, a comparative study between ultra-high molecular weight polyethylene (UPE) and polytetrafluoroethylene (PTFE) POU filtration has been carried out. Results correlate with the occurrence or the mitigation of micro bridges in a 45nm dense line pattern created through immersion lithography as function of POU membrane.

9425-13, Session 5

Total fidelity management in self-aligned multiple patterning process

Masatoshi Yamato, Noriaki Okabe, Arisa Hara, Sakurako

Natori, Shouhei Yamauchi, Kenichi Oyama, Tokyo Electron AT Ltd. (Japan); Hidetami Yaegashi, Tokyo Electron Ltd. (Japan)

Through the continuous scaling with extension of 193-immersion lithography, the multi-patterning process with the grid-based design has become nominal process for fine fabrication to relax tight pitch designs. In self-aligned type multiple patterning, 7 nm node gate pattern was reported and it was become a focal point LER on core-pattern is essential category to control pattern placement variations. Though CD uniformity (CDU) on line pattern in self-aligned double patterning (SADP) is relatively stable caused in high thickness controllability of spacer deposition films, the variations of CDU and LER on first core pattern impinge the CDU on space and pitch pattern. In previous study, pattern fidelity of single exposure patterning was improved through photoresist smoothing process using direct-current superposition technique.

In this paper, we will report that photoresist smoothing work in an efficient way to pattern fidelity control in self-aligned type multiple patterning and cut-hole pattern.

9425-14, Session 5

Tailored molecular glass resists for Scanning Probe Lithography

Christian Neuber, Hans-Werner Schmidt, Peter Strohriegl, Andreas Ringk, Tristan Kolb, Andreas Schedl, Univ. Bayreuth (Germany); Vincent Fokkema, Marijn G. A. van Veghel, VSL Dutch Metrology Institute (Netherlands); Mike Cooke, Oxford Instruments (United Kingdom); Colin Rawlings, Urs Dürig, Armin W. Knoll, IBM Research – Zürich (Switzerland); Jean- François G. N. de Marneffe, Ziad el Otell, IMEC (Belgium); Marcus Kaestner, Yana Krivoshapkina, Matthias Budden, Ivo W. Rangelow, Technische Univ. Ilmenau (Germany)

A molecular glass is a super-cooled highly viscous liquid or solid material that didn't have sufficient time to equilibrate and thus shows a stable or metastable amorphous state. The amorphous state results in advantageous properties such as good transparency, processability, high homogeneity and isotropic properties.1 Most notable in comparison to high molecular polymers, molecular glass materials have a well-defined structure and typically a small molecular size. Consequently, they do not undergo chain entanglement and show higher vapor pressure and lower viscosities above their glass transition temperatures. In summary, these materials are ideal candidates for future nanolithography as the patterning resolution can theoretically reach the building block size, which means for molecular glasses the size of utilized small molecules.2 The tailoring of utilized resist materials towards required properties is one of the key factors to control the resolution of future lithography and nanomanufacturing.

The achievable lithographic resolution is mainly determined by the confinement of the lithographic reaction, defined by the applied patterning technique and patterning parameters, as well as by the resist material itself, which includes the size and its distribution of the individual molecules in the thin resist films, the glass transition temperatures (Tg), additives, solubility, etch resistance, adhesion, resist preparation method, etc.3 However, for Scanning Probe Lithography (SPL), only a few resist investigations dealing with commercial available molecular glass resists have been published. In general, closed-loop electric field SPL has already demonstrated high-resolution patterning capability by utilizing the molecular glass resist calix[4]resorcinarene, as well as benefits of combining SPL with electron beam lithography in a mix and match type patterning process.4-6 In addition, the application of molecular glass resists in thermal SPL allowed the realization of complex high-resolution patterns and even the realization of three dimensional shapes.7

In this work solvent-free film preparation from tailored synthesized molecular glass resists, their thermal analysis, the characterization of etch resistance for plasma etching transfer processes, and the evaluation of the patterning performance using SPL tools, in particular electric field and thermal based SPL, is demonstrated. Therefore, a series of: (i) Twisted fully aromatic dicarbazole-biphenyl materials, (ii) fully aromatic spiro-based, and (iii) tris-substituted twisted resist materials were systematically investigated. The materials feature very high glass transition temperatures of up to 173 °C, which allows solvent-free thin film preparation by physical vapor deposition (PVD) due to their high thermal stability. In pattern transfer a sufficient plasma etching resistance was observed, which enables a etch selectivity to silicon of more than 6:1. This allows an efficient pattern transfer even by utilizing only 10 nm thin resist films. Their lithographic resolution potential is demonstrated by positive and negative tone patterning using electric field and thermal SPL.

References

[1] Shirota, Y., "Photo- and electroactive amorphous molecular materials - molecular design, syntheses, reactions, properties, and applications", Journal of Materials Chemistry 15, 75 (2005).

[2] De Silva, A., Felix, N. M. and Ober, C. K., "Molecular glass resists as high-resolution patterning materials", Advanced Materials 20, 3355-61 (2008).

[3] Reichmanis, E., Nalamasu, O. & Houlihan, F. M., "Polymers for microlithographic applications: new directions and challenges", Macromolecular Symposia 175, 185-196 (2001).

[4] Kaestner, M., and Rangelow, I. W., "Scanning proximal probe lithography for sub-10nm resolution on calix[4]resorcinarene", J. Vac. Sci. Technol. B 29, 06FD02 (2011).

[5] Kaestner, M., and Rangelow, I. W., "Scanning Probe Lithography on Calixarene," Microelectron. Eng. 97, 96–99 (2012).

[6] Kaestner, M., Hofer, M., and Rangelow, I. W., "Nanolithography by scanning probes on calixarene molecular glass resist using mix-and-match lithography", J. Micro/Nanolith. MEMS MOEMS 12(3), 031111 (2013).

[7] Pires, D., Hedrick, J. L., De Silva, A., Frommer, J., Gotsmann, B., Wolf, H., Despont, M., Duerig, U. and Knoll, A. W., "Nanoscale Three-Dimensional Patterning of Molecular Resists by Scanning Probes", Science 328, 732-735 (2010).

Acknowledgement: The research leading to these results has received funding from the European Union's Seventh Framework Programme FP7/2007-2013 under Grant Agreement No. 318804 (Single Nanometer Manufacturing for beyond CMOS devices – acronym: SNM).

9425-15, Session 5

Effects of the statistical fluctuation of PAG and quencher on LWR of ArF resists

Mitsuhiro Fujita, Michihiro Shirakawa, Shuhei Yamaguchi, FUJIFILM Corp. (Japan)

As the minimum feature size of state-of-the-art semiconductor devices has been reduced to below 20 nm, reduction in the line width roughness (LWR) or the line edge roughness (LER) of resist patterns has become even more crucial. So far, a number of researches have been conducted on the LWR of chemically amplified resists (CAR). It has been reported that LWR is influenced by various factors, such as the shot noise of exposed photons or electrons, the quality of aerial images, the molecular structure of polymers, the diffusion length of acid during post exposure bake (PEB), and so on. Although the details of LWR are getting clear, it is still not established how to design resist material to reduce LWR without the deterioration of other lithographic performances.

We report herein our understanding about the root cause of LWR and recent progress on improvement of LWR by theory-based material design. In this work, we discussed the relation between LWR and the non-uniformity of the sensitivity of ArF resists caused by the statistical fluctuation of the chemical composition at nm scale. Note that the fluctuation of chemical composition at nm scale cannot be avoided even if the materials in ArF resist are well miscible with each other and there is no apparent segregation, because the number of the molecules contained in extremely small volume is not large enough to ignore statistical fluctuation. Especially, we focused on the fluctuation of the concentration of photo acid generator (PAG) and

quencher because the influence of the concentration fluctuation of PAG and quencher to the sensitivity fluctuation was supposed to be much larger than that of the other components of resist material.

We investigated a statistical model of resists and derived a formula for LWR caused by the statistical non-uniformity of sensitivity. We compared experimental data of LWR obtained by ArF lithography and the theory and the experimental results showed good agreement with the theory. It indicated that, at least in case of ArF lithography, LWR was mainly caused by the statistical fluctuation of PAG and quencher.

Based on the theory, we developed new kinds of PAG and quencher that are expected to reduce the statistical nonuniformity of sensitivity. Using these new materials, we succeeded in improvement of LWR without the trade-offs between other lithographic performance (i.e., exposure latitude or sensitivity).

The results of this work provide not only new insight into the cause of LWR of CAR but also theoretical strategy for further LWR improvement. We believe that the theoretical design of resists based on the statistical model is useful for next generation lithography as well as ArF lithography.

9425-16, Session 5

Fundamental study of spin-coating using in-situ analysis and simulation

Masahiko Harumoto, Jun-ichi Yoshida, Dainippon Screen Manufacturing Co., Ltd. (Japan); Harold Stokes, Dainippon Screen Deutschland GmbH (Germany); Yuji Tanaka, Tadashi Miyagi, Koji Kaneyama, Charles Pieczulewski, Masaya Asai, Dainippon Screen Manufacturing Co., Ltd. (Japan)

Spin coating has been used as a photoresist application method for many years[1,2] and consequently certain defects have been recognized through each resist generation; i-line, KrF, ArF, ArF immersion and, most recently, EUV[3-7]. Last year we reported an in-situ analysis via high-speed video camera that proved to be useful for understanding defect formation such as non-uniformity spots within organic film coatings and post-develop water-mark defects.[8] In this study, fingerprints known as 'tiger stripes' around the wafer's edge were analyzed. This phenomenon, for example, is directly related to the wafer spin-speed and air-flow during coat-processing.

Utilizing a high-speed camera and 3D simulation we can reveal the mechanism of fingerprint generation for 'tiger stripe' phenomenon, confirm the mechanism with several different spin-speeds, and correlate these to defect inspection results. Furthermore, we will discuss the expansion to 450mm wafer.

9425-17, Session 5

Contact hole pitch scaling incorporating direct current superposition

Jeffrey T. Smith, Anton deVilliers, Nihar Mohanty, TEL Technology Ctr., America, LLC (United States); Yuichiro Miyata, Tokyo Electron Kyushu Ltd. (United States); Vinayak Rastogi, Sanjana Das, TEL Technology Ctr., America, LLC (United States)

Patterning methods for pitch scaling of contact hole and via structures generally require multiple lithography and etch passes or even more complicated cross-spacer processes, all of which require a number of deposition and etch steps.

The incorporation of direct current superposition (DCS) cure process enables memorization of small, complex contact hole and via patterns directly into photoresist films, greatly simplifying the complexity and cost compared to other contact pitch scaling techniques such as LELE and cross-self aligned multiple patterning.

The DCS cure process, utilizing ballistic electrons to create a finite modified layer within the resist pattern, effectively hardens the resist while depositing a sputtered SiO2 film over the initial pattern, rendering it impervious to any solvent attack from secondary film coatings and lithography passes Trench or contact type patterns can then be effectively memorized into a photoresist film which does not need to be removed prior to the coating of a second resist film which will be used for either pattern stitching or for cross-type pattern decompositions incorporating aspects of intersecting patterns contained in both films. The incorporation of DCS processes enables a wide selection of resist materials that can be used in the curing process, unlike previous methods of resist pattern memorization which required the use of exclusively PTD and even alcohol-based resists. This method enables the incorporation of NTD resists, with their superior contact and small trench imaging capability, to be used in the patterning process.

In this paper we present a cost-effective method utilizing memorization directly in photoresist films for generating memory and logic type contact patterns with two exposure passes which would normally require more complex LELELE (or greater) decompositions. We have demonstrated that this process can be used to generate. We will also present work looking at incorporating interlaced periodic structures through the DCS-enabled resist memorization process to create dense contact / via arrays.

Figure1shows a very simple demonstration of this process where 28nm slot contacts with tip-to-tip spacing of 30nm are created through the DCS-enables resist memorization process.1 Semi-dense lines are imaged and then processed through DCS cure to both harden the resist and deposit a thin SiO2 film over the pattern which memorizes it directly in the photoresist. Additional photoresist is then coated directly overtop the pattern (no transfer etch to a hardmask, no stripping of the resist or antireflective films are required) and processed through a second exposure made of 28nm trenches @ 80nm pitch. The final pattern which can be transferred to a hardmask contains the overlapping open areas of both photoresist patterns which produce a 28nm slot contact with 30nm tip-to-tip spacing.

The additional benefit of this process is that it enables other track-based technology to slim the images in each resist film in order to create even smaller final patterns such as NTD-compatible trimming materials, and anti-spacer materials.

9425-18, Session 5

Revealing beam-induced chemistry using modulus mapping in negative-tone EUV/e-beam resists with and without cross-linker additives

Deidre L. Olynick, Prashant K. Kulshreshtha, Dominik Ziegler, Lawrence Berkeley National Lab. (United States); Scott Dhuey, The Molecular Foundry (United States); Ken Maruyama, JSR Micro, Inc. (United States); Paul D. Ashby, Lawrence Berkeley National Lab. (United States)

Understanding fundamental resist chemistry in candidate systems is crucial for the success of next generation lithographies. Previously, we studied Noria-MAd (methyl-admantane) molecular resist in negative tone (Noria-MAd) with varying amounts (0-20% by weight) of oxetane functionalized Noria. The oxetane addition induced cross-linking towards higher material modulus and better patterning in negative tone development. Although we measured an increase in modulus with increasing cross-linker additive, the best pattern quality was not at the highest cross-linker amount.1,2,3 We found that best pattern quality is at lower amounts of cross-linker additive (5%) in part because the lower amount of cross-linker balanced the benefits of cross-linking against the swelling that can occur when hydrophobic material (molecules that are only partially deprotected) is trapped within the cross-linked matrix.

Here we investigate deprotection chemistry and modulus as a function of exposure dose and cross-linker additives using PeakForceTM Tapping AFM analysis. In the Noria-MAd, modulus should increase with dose because more deprotection leads to stronger hydrogen bonding. Cross-linker additives can increase the modulus further. We compare the measured

modulus in Noria-MAd with 0, 5, and 20% cross-linker addition over a large dose range. Resists were exposed in a 100 keV electron beam and modulus measurements were taken for both post-exposure and post-development. We find distinct changes in modulus throughout dose and far beyond the dose to reach full thickness. This indicates chemical changes extend far past the point where the material becomes insoluble. Hence, the modulus mapping technique provides insight into the dose induced chemical changes, even on patterned features where other techniques, such as FTIR, would be insensitive.

To understand how modulus through dose correlates to pattern quality, we looked at patterned features as a function of dose and bias (writing the feature smaller than the printed size). By biasing e-beam features, we increase the dose within a written line without changing line size. We find that pattern collapse is reduced with bias even in the base-line resist (no cross-linking). The result can be understood by combining aerial image simulations with the measured modulus as function of line size. Unbiased 25 nm half-pitch lines do not reach the dose where the modulus measurement is saturated. Biasing the lines to 12 nm increases the measured modulus and indicates further deprotection. This will reduce swelling as well as mechanically strengthen the lines.

[1] P.K. Kulshreshtha, K. Maruyama, S. Kiani, D. Ziegler, J. Blackwell, D. Olynick, P.D. Ashby, in: SPIE Advanced Lithography, International Society for Optics and Photonics, 2013, pp. 86810O-86810O-86811.

[2] P.K. Kulshreshtha, K. Maruyama, S. Kiani, S. Dhuey, P. Perera, J. Blackwell, D. Olynick, P.D. Ashby, in: SPIE Advanced Lithography, International Society for Optics and Photonics, 2013, pp. 86820N-86820N-86810.

[3] P.K. Kulshreshtha, K. Maruyama, S. Kiani, S. Dhuey, P. Perera, J. Blackwell, D. Olynick, P.D. Ashby 2014 Nanotechnology 25 315301

9425-19, Session 6

Understanding the efficacy of linewidth roughness post processing *(Invited Paper)*

Chris A. Mack, Lithoguru.com (United States)

Line-edge roughness (LER) and linewidth roughness (LWR) are becoming increasingly important sources of error in lithographic processing since feature sizes have been shrinking faster than the magnitude of the LWR. For extreme ultraviolet (EUV) lithography in particular, reducing LWR has been a vexing problem, with resist LWR on the order of 5 nm (3?) but requirements less than 2 nm. One potential solution is the use of post-processing, such as electron beam or ultraviolet light exposure, annealing in a hydrogen environment, HBr plasma treatment, or the etch process itself. Such processes have been shown to reduce the high-frequency roughness and the overall 3? of the roughness. There is some debate, however, about whether smoothing only the high-frequency roughness has any significant impact on the detrimental effects of LWR on critical dimension uniformity (CDU).

This paper will attempt to understand the efficacy of post-processing for the improvement of CDU. First, the impact of post-processing on the power spectral density (PSD) of the roughness will be modeled as a low-pass filter, turning a pre-processing PSD into a post-processing PSD. Then, the impact of the amount of smoothing on the CDU of the final feature will be determined using the recently derived expression [1]

where ?CDU is the variation of the mean linewidth from feature to feature for a line of length L, ?LWR is the LWR for an infinitely long line, ? is the correlation length of the roughness, and H is the roughness exponent (from the PSD post-processing).

Further, this paper will explore the impact of when the post-processing is done for the case of complimentary lithography. Does it matter whether the post-processing comes before or after the cut-lithography step?

[1] C. A. Mack, "Analytical Expression for Impact of Linewidth Roughness on Critical Dimension Uniformity", Journal of Micro/Nanolithography, MEMS, and MOEMS, Vol. 13, No. 2 (Apr-Jun, 2014) p. 020501.

9425-20, Session 7

Influence of etch process on contact hole local critical dimension uniformity in extreme-ultraviolet lithography

Gian F. Lorusso, Ming Mao, IMEC (Belgium); Liesbeth Reijnen, Katja Viatkina, Roel Knops, Timon F. Fliervoet, ASML Netherlands B.V. (Netherlands)

Contact Hole (CH) Local Critical Dimension Uniformity (LCDU) has a direct impact on device performance. As a consequence, being able to understand and quantifying the different LCDU contributors and the way they evolve during the various process steps is critical. In this work the impact of etch process on LCDU for different resists and stacks is investigated on ASML NXE:3100 and NXE:3300. LCDU is decomposed into resist, mask, and metrology components. The design of the experiment is optimized to minimize the decomposition error. CD and LCDU are monitored and found to be stable.

We observed that the net effect of the etch process is to improve LCDU, although the improvement is both stack- and resist-dependent. Different resists demonstrate the same LCDU improvement in absolute terms, so that the LCDU after etch will depend on the initial resist performance. Using a stack different from the one used to set up the etch process can undermine the LCDU improvement. A characterization of the effect through pitch indicated the worse the LCDU after litho is, the larger the absolute improvement will be.

The impact of the various etch steps is investigated in order to identify the physical mechanisms responsible for the LCDU improvement through etch. Both top-down and cross section Scanning Electron Microscopy (SEM) are used. The step-by-step analysis of the etch process showed that the main LCDU improvement is achieved during oxide etch, while the other process steps are either ineffective or detrimental in terms of LCDU. The main cause of the LCDU improvement is then attributed to the polymerization of the CH surface happening during the oxide etch.

Finally, the LCDU improvement caused by the etch process is investigated as a function of the initial LCDU after litho in a relatively broad range (2-15nm). In Figure 1, the ratio between LCDU after litho over LCDU after etch is plotted as a function of the initial LCDU after litho for two different resists. The results indicate that the impact of etch on LCDU is characterized with a single curve, specific to the etch process in use and independent of the resist type. In addition, we observe that the percentage LCDU improvement is constant above a certain threshold, in agreement with the through-pitch results.

9425-21, Session 7

Organic carbon hard masks utilizing fullerene derivatives

Alex P. Robinson, Andreas Frommhold, The Univ. of Birmingham (United Kingdom); Alan G. Brown, Irresistible Materials Ltd. (United Kingdom); Tom Lada, Nano-C, Inc. (United States)

Progress in lithographic resolution has made the adoption of extremely thin photoresist films necessary for the fabrication of '1x nm' structures to prevent issues such as resist collapse during development. While there are resists with high etch durability [1], ultimately etch depth is limited by resist thickness. A possible solution is the use of a multilayer etch stack. This allows for considerable increase in aspect ratio. For organic hard masks a carbon-rich material is preferred as carbon possesses a high etch resistance in silicon etch plasma processes. A thin silicon topcoat deposited on the carbon film can then be patterned with a thin photoresist film without feature collapse, and the pattern transferred to the underlying carbon film by etching. This produces high aspect ratio carbon structures suitable for substrate etching. In terms of manufacturability it is beneficial to spin coat the carbon layer instead of using chemical vapor deposition [2], but the

presence of carbon-hydrogen bonds in typical spin on carbon leads to line wiggling during the etch. We have previously introduced a fullerene based 'spin on carbon' (SoC) with high etch durability and reported on material characterization [3, 4]. Here recent advances in material development and work towards commercialization of the materials are presented. The low hydrogen level in the material allowed for high resolution etching without wiggling.

Materials were formulated in solution by mixing the fullerene derivatives with suitable crosslinkers, commonly in cyclohexanone or anisole. Spin coating produced homogenous carbon films with few defects and thicknesses up to 150 nm. After deposition the carbon layers were baked on a hotplate to crosslink the film at temperatures of 250 – 350°C. Crosslinkers typically employed were epoxies of either novolac or fluorene type. Fluorene's advantage is its lower Ohnishi number leading to improved etch durability. However the fluorene expoxy only successfully crosslinks the carbon film at an elevated bake temperature. We have thus developed a fullerene derivative, which enables the use of amine crosslinking with a fluorene dianiline. In this way it was possible to combine fluorene etch performance with a lower bake temperature

Use of the materials in etch stacks was demonstrated. A 20 nm thin silicon film was sputtered on top of the carbon layers. Resist patterns were written on the silicon topcoat by e-beam lithography and transferred to the silicon thin film using SF6/CHF3 ICP. The carbon layer was then etched by O2 plasma through the silicon mask and finally the pattern was transferred into the silicon substrate by the same process as the topcoat.

9425-22, Session 7

Hybrid materials: a bottom-up approach for micro- and nanolithography

Giovanna Brusatin, Univ. degli Studi di Padova (Italy)

Micro and nanostructuring surfaces by a direct lithographic process is uncommon. A functional organic or inorganic material is generally indirectly patterned, by patterning a sacrificial resist deposited on it first, and then by transferring the image of the sacrificial layer to the functional material, in a pattern-transfer step. This multi-step process often causes a deterioration of lithographic performance, is time-consuming, and makes the process complicated.

Engineered organic-inorganic hybrid materials, HyMat, emerging as an alternative to organic polymers for micro and nanolithography, offer new opportunities for the easy, fast and cheap development of micro- and nano- devices, and can be employed as final device materials in a direct lithographic process [1].

Integration of inorganic networks, organic functional groups and optically active molecules or nanoparticles allows to obtain combinations of properties and structures otherwise impossible with traditional material.

In particular, a simple and highly versatile synthesis platform is presented enabling preparation of HyMat [2], built up by a bottom-up sol-gel approach at low process temperatures. A few types of key building blocks constitute the way for accessing HyMat and make up their formulation, providing a means to synthetize innovative materials enabling to get:

- Optical active micro and nanostructures
- Miniaturized sensors for analytes in gaseous or liquid media
- Direct patternability with a range of lithographic techniques
- Variable inorganic and organic compositions and controlled porosity

The amount and type of these building blocks determine the key points of HyMat success: (1) direct patternability with different lithographic tools with high performance; (2) presence of both positive and negative tones, exploited thanks to a deep knowledge and control over material interactions with radiation or thermal/pressure-driven processes and developers, that contributes to reduce costs and steps of a lithographic process; (3) variety of compositions, from both organic-inorganic hybrid to totally inorganic, and chemical-physical properties as transparency, refractive index, stiffness, porosity, sensing functionality, offering a broad field of possible applications for HyMat as final device material.

Such spin-on materials with ceramic (i.e. GeO2, TiO2, ZrO2, HfO2, Al2O3) or silica based hybrid compositions has allowed a one-step development of plasmonic or fluorescent sensing devices [3, 4], high resolution patterns [5], dry-etching masks with outstanding resistance [6], optically active micro and nanostructured platforms.

1. G. Brusatin et al. Nanotechnology 2008
2. http://www.hymat.dii.unipd.it/
3. L Brigo et al. J. Mat. Chem. C 2013
4. L Brigo et al. Nanotechnology 2013
5. L Brigo et al. Nanotechnology 2012
6. E. Zanchetta et al. Adv. Mater. 2013

9425-23, Session 7

Enhancing etch selectivity in DSA block copolymer films with sequential infiltration synthesis on 300mm Si substrates

Arjun Singh, IMEC (Belgium) and Katholieke Univ. Leuven (Belgium); Safak Sayan, Intel Corp. (United States) and IMEC (Belgium); Ziad el Otell, IMEC (Belgium) and Katholieke Univ. Leuven (Belgium); Boon Teik Chan, Roel Gronheid, IMEC (Belgium)

Numerous block copolymer systems (BCP) can be used in directed self-assembly (DSA) processes to form patterns useful in lithography, especially line-space with lamellar phase systems and vias/pillars with cylindrical phase systems. However, a lot of these systems with attractive pattern formation capabilities have limited plasma etch contrast between the polymer domains. One potential solution to greatly enhance this etch contrast is a recently developed technique called sequential infiltration synthesis (SIS). SIS is a self-limiting synthesis technique, like atomic layer deposition, where organo-metallic (OM) precursor vapours and oxidants are introduced into self-assembled block copolymer systems in multiple cycles. In the first half of each cycle the OM precursor selectively reacts with one polymer domain, and in the second half of the cycle the oxidant reacts with the OM groups in the polymer film to selectively form metallic compounds in one of the polymer domains. Thus, the polymer pattern is transformed into a metallic mask with much enhanced plasma etch contrast. We report the effects of such a block-selective SIS process of metallic compounds on the feature sizes, roughness and profiles of patterns formed with BCP systems. Additionally, we investigate patterns transferred into substrate layers from metallic masks synthesised by such processes and evaluate SIS process compatibility with pre-existing DSA process flows on 300mm Si substrates.

9425-51, Session PS1

Studying the mechanism of hybrid nanoparticle EUV photoresists

Li Li, Jing Jiang, Ben Zhang, Cornell Univ. (United States); Mark Neisser, SEMATECH Inc. (United States); Jun Sung Chun, SEMATECH Inc. (United States) and SUNY College of Nanoscale Science and Engineering (United States); Christopher K. Ober, Emmanuel P. Giannelis, Cornell Univ. (United States)

With the development of nanofabrication and shrinkage of feature size for semiconductor devices, photolithography technology that can provide high-resolution patterning is required. Research in short wavelength lithography, especially for extreme ultraviolet lithography (EUV), is attracting considerable attention. The next generation EUV photoresists should combine high etch resistant, high imaging quality and appropriate light absorption. Previous results in our group showed that hybrid nanoparticles

composed of inorganic metal oxide core and organic ligands have excellent dual tone photo-patterning performance under EUV exposure. A record lowest dose of 4.2 mJ/cm2 for EUV photoresists with negative patterning has been achieved.

This presentation is focused on the investigation of dual tone patterning mechanism with hybrid inorganic/organic photoresists. It is hypothesized that the particle size change of nanoparticles leads to their solubility difference in the developers before and after exposure, and thus forms high sensitivity photo-patterning. Hafnium oxide (HfO2) modified with carboxylic acid groups were prepared and the influence of electrolyte solutions as well as pH on their particle size change was investigated. The average particle size and zeta potential of the nanoparticle in different electrolyte solutions were measured by dynamic light scattering (DLS). The results show that addition of different concentrations of electrolytes changed the hydrodynamic diameter of nanoparticles in the water. Increased concentration of tetramethyl ammonium hydroxide (TMAH) caused the zeta potential of nanoparticle to change from positive to negative and its hydrodynamic diameter to increase dramatically from 40 nm to 165 nm. In addition, increasing concentration of triflic acid led to the decrease of particle size and zeta potential. This work provides for the first time fundamental information about the inherent nature of hybrid nanoparticle photoresists, their behavior in solution, and a framework to start thinking about optimization under various development conditions.

9425-53, Session PS1

Strategies for enhancing the sensitivity of novel non-chemically amplified (n-CAR) negative tone resists for EUVL

Vikram Singh, V.S. V. Satyanarayana, Vishwanath Kalyani, Subrata Ghosh, Chullikkattil P. Pradeep, Satinder K. Sharma, Kenneth E. Gonsalves, Indian Institute of Technology Mandi (India)

EUV-Lithography (wavelength 13.5 nm), is being developed to realize high-volume production of semiconductor devices with sub-20 nm minimum feature size. Most commonly, the reduction in the line edge roughness (LER) is the most serious problem in the development of high-resolution EUV-resists due to RLS trade offs. However, the line edge roughness (LER) is still far from the required value of 1 nm as per ITRS-2013. Furthermore, the sensitivity should be reduced to 10 mJ/cm2. We recently developed non-chemically amplified resist materials, which showed potential in patterning down to 15 nm and below having low LER. This development involves strategic incorporation of radiation sensitive trifluoromethane sulfonate units in the monomer structure (MAPDST) which undergoes AIBN-initiated free radical polymerization to yield the desired photosensitive resist MAPDST homopolymer. Though the material is potent enough to pattern sub-20 NM HP lines pattern, the sensitivity is too low (~34.4mJ/cm2) to meet the target projected by ITRS-2011. Interestingly, incorporation of methyl methacrylate functionality as a dissolution inhibitor into the polymer backbone resulted in a significant increase in sensitivity (~10 mJ/cm2) along with improved LER. Though there could be several parameters that can play major roles in determining the sensitivity of MAPDST homopolymer, the above results showed us an avenue that the dissolution microstructure is one of the most critical parameters that helps in improving the sensitivity of base resist MAPDST homopolymer. The MAPDST-MMA copolymer can image down to 20 nm and below and as observed its sensitivity is molecular weight dependant (For MW-17,000 sensitivity is approx. 10 mJ/cm2 and for 30,000 obtained around 5 mJ/cm2). In this presentation, the effects of molecular weight, dissolution inhibitor and hybrid metal sensitizers in the microstructure of the non CAR resist backbone polymer and their cumulative effect on sensitivity and high resolution are discussed.

9425-54, Session PS1

Measurement of lateral diffusion coefficient of single-guest molecules toward evaluation of local inhomogeneity in polymeric materials

Syoji Ito, Osaka Univ. (Japan); Satoshi Takei, Toyama Prefectural Univ. (Japan); Hiroshi Miyasaka, Osaka Univ. (Japan)

Polymeric materials play crucial rolls in lithographic processing techniques that are diversely applied in fabricating fine structures at the laboratory level as well as in industrial processes. In spite of a wide range of significant application, it is still challenging to clarify precise molecular dynamics of reactions occurring in polymeric materials, including polymerization, crosslinking, and photodecomposition, because these reactions shows quite complex behaviors owing to intrinsic inhomogeneity in such condensed materials.

In recent several years we have been trying to investigate the dynamics of reactions at nanometer scale and to evaluate the microscopic inhomogeneity in polymeric materials in terms of the diffusive motion of single guest molecules precisely tracked at nanometer accuracy. In the present study we have applied the single-molecule tracking (SMT) for the characterization of microscopic property variations in a dextrin-based photo-curable material, PA08, provided from Nissan Chemical Industries, Ltd.

Thin films of PA08 including a small amount of a photoinitiator and a very tiny amount of fluorescent guest dyes were prepared on well-cleaned glass substrates by spin-casting. We employed a 325-nm He-Cd laser to induce crosslinking in the PA08 films. Before photoirradiation with the UV laser the guest dyes showed lateral diffusion in PA08 films without network formation. The diffusion coefficient of the guest dye varied according to their location, reflecting intrinsic microscopic inhomogeneity in the sample. UV irradiation induced network formation in the sample films, resulting in a decrease in the lateral diffusion coefficient of the guest dye depending on UV dose.

To characterize spatial inhomogeneity in the sample films during the network formation, we obtained relative standard deviations (RSD) of the lateral diffusion coefficient. The RSD of the lateral diffusion coefficient increased at the early stage of the network formation under small UV dose. With an increase in UV dose the RSD reached a peak, then decreased to a plateau. At the final stage of the reaction at the plateau, the RSD became smaller than the initial value.

By integrating the results obtained we can summarize the dynamics of the network formation. At the early stage of reaction the microscopic inhomogeneity of the PA08 films tentatively increase. After reaching a peak the inhomogeneity decrease in turn. Finally, at the last stage, the polymer films become more homogeneous than the initial state.

9425-55, Session PS1

Measurement of acid diffusion from PAG in photoresists by using TOF-SIMS with GCIB

Naoki Man, Toray Research Ctr., Inc. (Japan); Atsushi Sekiguchi, Litho Tech Japan Co., Ltd. (Japan)

Diffusion behavior of acid generated from PAG in resist films is a one of most effective factor which characterizes the performance of photoresists. The top coat method has been proposed as a method for measuring the distance of diffusion (diffusion length) of acid which was generated from PAG due to the exposure, during the PEB process and for calculating the diffusion coefficient. Top coat material (“TC” hereinafter) containing PAG (second layer) is coated on a PAG-free resist (first layer), then the exposure and PEB processes are performed. In this procedure, the acid generated in the TC (second layer) during the exposure diffuses into the resist (first layer) when the PEB was performed. The process of developing this sample

removed the TC and the parts of the first layer into which the acid has diffused. We can obtain the acid diffusion length based on the quantity of film removed by the development. However, this method does not provide the distribution of diffusing PAG in resist films, because the thickness of residual films after the developing process is measured.

In this work, we applied TOF-SIMS measurement with gas cluster ion beam (GCIB) etching to the top coat method, in order to obtain the distribution of diffusing PAG and residual protecting groups of the resin in the resist (first layer) after the exposure and PEB processes. TOF-SIMS with GCIB has been developed as a depth profiling method for polymers. It reveals the distribution of chemical structures in the depth direction. Fig. 1 shows depth profiles of C4F9SO3- corresponding to both of PAG anion and acid in TC containing PAG (second layer) / PAG-free resist (first layer) samples before / after exposure and after PEB. Distribution of C4F9SO3- before and after exposure is similar in the resist, though the intensity in TC after exposure is lower than that before exposure. Concentration of C4F9SO3- in TC after PEB is much lower than before PEB. Distributions of C4F9SO3- shifted into the resist according to the PEB temperature. We investigated the detail of the diffusion behavior of acid from PAG and compare with the original top coat method which uses the development.

9425-56, Session PS1

The effect of resist material composition on development behavior

Shinya Minegishi, Toshiro Itani, EUVL Infrastructure Development Ctr., Inc. (Japan)

Extreme ultraviolet (EUV) lithography which extends photolithography to extreme shorter wave length (13.5nm) is capable of achieving sub-20 nm half pitch resolution by single exposure. Therefore, EUV lithography is the leading candidate to succeed 193 nm immersion lithography. However, Resolution, Line Width Roughness (LWR) and Sensitivity (RLS) trade-off is still a significant issue for EUV resists. We have evaluated the EUV resist characteristics and lithographic performance using the several analysis tools and the small-field exposure tool (SFET) and EB exposure tool for fundamental study for breaking the deadlock of this trade-off.

There are several points for the better resist patterning, and “development” is one of the most important steps. In situ observation of development was investigated, for example by quartz crystal microbalance (QCM) method, and swelling behavior of resist was observed for better understanding of development [1]. One of the representative analyses at EIDEC is the direct observation of resist development behavior by high-speed AFM [2-5]. Recently various materials are tested as EUV resist component, therefore, the development behavior will be different from the conventional hydrocarbon type resist. However, the direct observation of development behavior has been investigated only for limited resist.

In this study, the relationship between resist composition and development behavior is evaluated. Systematic evaluation of hydrophobic unit ratio in resist and development behavior was investigated. The resist was exposed with EUV or EB exposure and the development behavior of the film was observed by high-speed AFM. In previous work, the swelling behaviors of exposed resist by tetramethyl ammonium tetramethylammonium hydroxide (TMAH) were; p-hydroxystyrene (PHS) type resist showed grain-formation and little swelling, methacryl type showed crater-like dissolution and little swelling, and PHS-methacrylate hybrid type resist showed huge swelling [2,3,4,5]. We will describe our recent experiments to compare the various resist composition and development behavior by high-speed AFM in this presentation. Introduction of hydrophobic unit into PHS-methacrylate hybrid type resist was examined, and the resist showed different development behavior. Grain-formation was observed and resist did not show swell or crater-like dissolution.

The detailed study will be reported on the presentation.

[1] M. Toriumi, SPIE Proc. 72732Y (2009).

[2] T. Itani, J. J. Santillan, SPIE Proc.79720H (2011).

[3] J. J. Santillan, T. Itani, SPIE Proc.83250P (2012).

[4] J. J. Santillan, T. Itani, SPIE Proc.86820I (2013).

[5] J. J. Santillan, M. Shichiri, T. Itani, SPIE Proc.90510O (2014).

9425-57, Session PS2

Hybrid nanoparticles for EUV lithography

Ben Zhang, Jing Jiang, Mufei Yu, Cornell Univ. (United States); Jun Sung Chun, SEMATECH Inc. (United States) and SUNY College of Nanoscale Science and Engineering (United States); Mark Neisser, SEMATECH Inc. (United States); Emmanuel P. Giannelis, Christopher K. Ober, Cornell Univ. (United States)

Extreme ultraviolet lithography (EUV-L) is considered the very important candidate for next generation patterning. One of its major issues is to design new photoresist materials with high resolution, etch resistance and sensitivity. Recently, Ober, Giannelis and coworkers have developed hybrid nanoparticles composed of an inorganic core and an organic ligand showing excellent lithographic performance under EUV exposure. Experimental results demonstrate that to date zirconium methacrylate (ZrO2-MAA) nanoparticles could give a critical dimension (CD) down to 21.5 nm, and a sensitivity of 4.2 mJ/cm2.

The present work describes new hybrid photoresist nanoparticles and explores the influence of ligand on their EUV patterning capacity. It is believed that the underlying mechanism for patterning involving ligand exchange and aggregation processes accounts for solubility changes between the exposed and unexposed regions. For example, zirconium isobutyrate (ZrO2-IBA) with saturated alkyl side group and zirconium dimethylacrylate (ZrO2-DMA) with an unsaturated side group were synthesized via a sol-gel method, with organic content selected between 40 and 70% according to thermogravimetric analysis (TGA) data. The relatively high organic content enables good solubility in propylene glycol monomethyl ether acetate (PGMEA) and meanwhile effectively suppresses the aggregation of nanoparticles, leading to small particle size range from 1 to 3 nanometer demonstrated by dynamic light scattering (DLS). For ZrO2-IBA, EUV patterning shows high sensitivity at the level of 2.6 mJ/cm2 with 30 nm resolution, while ZrO2-DMA exhibits a remarkable resolution as small as to 20 nm and even higher sensitivity down to 1.4 mJ/cm2. These results demonstrate that unsaturated bonds are not necessary for patterning but that a larger aliphatic side group may help to improve lithographic performance. Moreover, this work opens a way to control EUV resist performance by tailoring of organic ligands.

9425-58, Session PS2

Development of new xanthendiol derivatives applied to the negative-tone molecular resists for EB/EUVL

Takumi Toida, Akihiro Suzuki, Naoya Uchiyama, Takashi Makinoshima, Masaaki Takasuka, Takashi Sato, Masatoshi Echigo, Mitsubishi Gas Chemical Co., Inc. (Japan)

We have been developing negative-tone molecular resists based on calix[4] resorcinarene derivatives. In our previous study, we could confirm the excellent patterns with high resolution and small LER by using this resist by EB/EUVL. However the pattern collapse was shown at sub 30 nm half-pitch, so it should be improved.

So we reported the new negative-tone molecular resists based on the xanthendiol derivatives, 13-biphenyl-13H-benzoxanthen-3,10-diol, MGR202. The molecular weight of MGR202 is 467. The EUV patterning result showed that the resist containing MGR202 could resolve the 20 nm half-pitch patterns by optimizing formulation and conditions.

Herein we report the negative-tone molecular resists based on the new xanthendiol derivatives. The new xanthendiol derivatives were easily synthesized by the condensation of aldehydes and dihydroxyaromatic

compounds. We found 13,13'-biphenyl-bis(13H-benzoxanthen-3,10-diol), MGR203, was showed the good applicability to the raw material for the resist for EB/EUVL. The molecular weight of MGR203 is 779, therefor we expect that the outgas of MGR203 is better than MGR202. MGR203 showed high solubility in conventional resist solvents such as PGME. The solubility of MGR203 is good for the raw material for the molecular resist.

The EB patterning result showed that the resist containing MGR203 on an organic layer substrate could resolve the 20 nm half-pitch pattern. Furthermore 15 nm half-pitch patterns were partially resolved. We will also present the EUV patterning result at the presentation.

9425-59, Session PS2

Light-scattering thermal cross-linking material using morphology of nanoparticle free polymer blends

Satoshi Takei, Toyama Prefectural Univ. (Japan)

A newly light-scattering thermal cross-linking material based on self-assembly for forming the morphology of nanoparticle free polymer blends was reported. The material design concept to use light-scattering thermal cross-linking material with high uniformity of light on display panel from LED for high quality such as brightness and evenness, mechanical properties, and gas and water barrier properties. The high light transmittance of 95 % and high light scattering rate of 5 % at 300-600 nm of wavelength, fast cure film at 150 ºC and 2 min in bake condition for high productivity were indicated in the light-scattering thermal cross-linking material using the nanoparticle free polymers with carboxylic acid functional groups. These novel system using morphology of nanoparticle free polymer blends in light-scattering package material for a LCD using LED was a valuable approach to the design of material formulations for newly light-scattering thermal cross-linking material.

9425-61, Session PS2

Blending approaches to enhance structural order in block-copolymer's self-assemblies

Xavier Chevalier, Célia Nicolet, Arkema S.A. (France); Raluca Tiron, Ahmed Gharbi, Patricia Pimenta-Barros, CEA-LETI (France); Guillaume Fleury, Georges Hadziioannou, Lab. de Chimie des Polymères Organiques (France); Ilias Iliopoulos, Christophe Navarro, Arkema S.A. (France)

Self-assembly of block-copolymers (BCP) is expected to be one of the most promising candidate to further decrease currently achievable lithographic dimensions. Indeed, the ability of these materials to form highly periodic structures with various morphologies (lamellaes, cylinders...) of interest and extremely aggressive features, render them as very appealing systems to produce nanosized patterns at low costs for microelectronics applications.

Although it has been proved that this technology presents several key advantages for microelectronics (short time bakes for the self-assembly process to take place, accessible and sizable dimensions ...), in order to introduce these systems on production tracks many challenges still remain to overcome. Among them, the level of defects in the self-assembly is probably one of the most important, and also one of the most tricky to answer about. Indeed, the ITRS roadmap requires less than 0.02 defects/cm2 for BCP's systems to find a place in microelectronics, and even if huge improvements on this topic have been made to reduce the defect level over the past years, this goal is still to be reached. The difficulties to answer this defect level problem come in part, at least, from a dual aspect of it. On one hand, as the self-assembly of BCP is governed by thermodynamic rules, the defect level is therefore intimately process-dependent; as end-users set the process's characteristics usable for the self-assembly (maximum time and temperature for example), this process-window has to be taken into account while answering the problem, whereas thermodynamic's laws cannot answer on its kinetics aspect. On the other hand, the defect level is material and feature's size-dependent as well, since BCPs with different blocks chemistries do not have the same physico-chemical properties (e.g. their glass transition temperature), and smaller features/periods will lead to assemblies with larger grain-size/correlation length/less defects than BCPs having larger features. From these two different aspects, since there is almost no room to tune the self-assembly process, it is therefore obvious that the material's properties will play a key role in the defect levels observed.

This contribution is dedicated to our studies on PS-b-PMMA BCPs systems blends. The BCPs materials used are synthesized in Arkema's factory at an industrial scale with a semi-continuous reaction process, enabling us to easily ramp up the synthesized quantities to tons level. We will highlight how it's possible to control the period of the blends, and compare blended systems with pure BCP in terms of defects level improvement and enhancement of the self-assembly's characteristics. More specifically, we will describe how the blends are influenced to produce characteristics simply unachievable with pure BCPs, like high aspect-ratio features for huge periods, or extremely weak defectives structures. Afterwards, an emphasis will be made on how this new properties observed on free-surfaces will be translated in some cases of interest for microelectronic applications like contact-hole shrink or lines and spaces graphoepitaxy approaches, as well as the transfer of the features in the substrate.

9425-62, Session PS2

Block co-polymer directed self-assembly for sub-10nm patterning

Kota Nishino, Yoshi Hishiro, JSR Micro, Inc. (United States); Masafumi Hori, JSR Micro N.V. (Belgium); Takehiko Naruoka, Hiroyuki Komatsu, Tomohiro Oda, Tomoki Nagai, Tooru Kimura, JSR Corp. (Japan)

Block Co-polymer (BCP) Directed Self-Assembly (DSA) method has become a key technology for enabling lithographic pattern feature shrinkage. BCP DSA process with different scheme has been developed for sub 20 nm patterning by using polystyrene-b-polymethylmethacrylate (PS-b-PMMA) block copolymer as typical material. Recently, DSA technology has achieved less than 10 nm patterning with high- ? BCP material, and new materials and process development is in progress to achieve better pattern fidelity.

We have developed several new high-? BCP materials and evaluated them for sub 10 nm patterning. In this paper, we will discuss the results of formation of 8.4 nm line patterns with our high-? block co-polymer. Furthermore, our high-? block co-polymer material is expected to be applicable to various next generations patterning techniques or process such as hole-pattern shrink and line/space multiple patterning. We will also discuss our high-? BCP materials performance and effect on CD placement error or CD variability.

9425-63, Session PS2

High-sensitivity green resist material with organic solvent-free spin-coating and tetramethylammonium hydroxide-free water-developable processes for EB and EUV lithography

Satoshi Takei, Toyama Prefectural Univ. (Japan); Makoto Hanabata, Osaka Univ. (Japan) and Toyama Prefectural Univ. (Japan); Akihiro Oshima, Miki Kashiwakura, Takahiro Kozawa, Seiichi Tagawa, Osaka Univ. (Japan)

We investigated the eco-friendly electron beam (EB) and extreme-ultraviolet (EUV) lithography using a high-sensitive negative type of green

resist material derived from biomass to take advantage of organic solvent-free water spin-coating and Tetramethylammonium hydroxide(TMAH)-free water-developable techniques. A water developable, non-chemically amplified, high sensitive, and negative tone resist material in EB lithography was developed for environmental affair, safety, easiness of handling, and health of the working people, instead of the common developable process of TMAH. The material design concept to use the water-soluble resist material with acceptable properties such as spin-coating properties on 200-300 mm wafer, prediction sensitivities of EUV at the wavelength of 6.7 and 13.5 nm, line and pillar patterns with less than 100 nm in high EB sensitivity of 10 μC/cm2, and etch selectivity with a silicon-based middle layer in CF4 plasma treatment was demonstrated for EB and EUV lithography.

9425-64, Session PS2

Aromatizing unzipping polyester for EUV photoresist

Kensuke Matsuzawa, Ryan Mesch, C. Grant Willson, The Univ. of Texas at Austin (United States); Marie Krysak, Intel Corp. (United States); Mike Olah, Scott Phillips, The Pennsylvania State Univ. (United States)

We designed and synthesized an unzipping polyester as a new candidate for photoresists. The concept of the polymer is depolymerizing in chain reaction when it absorbs a photon. Chemically amplified resists (CAR) are generally used as photoresists. This system improves the sensitivity by the acid diffusion produced by photo irradiation. But the acid diffusion should come out as line edge roughness (LER) with decreasing half pitch length and close to 10nm half pitch. Instead of the acid diffusion, the chemical change after photo irradiation is amplified by intra-molecular reaction in our design. It depolymerizes with aromatization in a chain reaction and produces low Mw aromatic compounds and carbon dioxide. By using it as dissolution inhibitor of Novolac, the polyester was exposed to EUV, and it showed sensitivity for EUV irradiation. The ideal material needs to have several properties. Dissolution inhibition effects for developer, solubility for developer after depolymerization and depolymerizing below 150°C. We are targeting to satisfy these properties and to achieve high resolution, high sensitivity and decreased LER by the unzipping polyester.

9425-65, Session PS2

Evaluation of novel lactone derivatives for chemically amplified EUV resists

Hiroyasu Tanaka, Tetsuhiko Mizusaka, Hiroyuki Tanagi, Kikuo Furukawa, Mitsubishi Gas Chemical Co., Inc. (Japan); Hiroki Yamamoto, Takahiro Kozawa, Osaka Univ. (Japan)

EUV lithography is the most favorable process for high volume manufacturing of semiconductor devices beyond 1X-Z nm half-pitch. Many efforts have revealed effective proton sources in acid generation in EUV resists, and the effective proton generation and the control of the generated acid diffusion are required to improve the breakthrough of the resolution - line width roughness - sensitivity(RLS) trade-off. To clarify the lithographic performance of these derivatives, we synthesized the acrylic polymers containing novel lactone derivatives as model photopolymers and exposed the resist samples based on these polymers to EUV and EB radiation. On the basis of the lithographic performances of these resist samples, we evaluated the characteristics of lactone derivatives upon exposure to EUV radiation. We discuss the relationship between the chemical structures of these derivatives and lithographic performance.

9425-66, Session PS2

Base developable negative-tone molecular resists based on epoxide cross-linking

Brandon Sharp, Richard A. Lawson, Hannah Narcross, Georgia Institute of Technology (United States); Jun Sung Chun, SEMATECH Inc. (United States) and SUNY College of Nanoscale Science and Engineering (United States); Mark Neisser, SEMATECH Inc. (United States); Laren M. Tolbert, Clifford L. Henderson, Georgia Institute of Technology (United States)

There has been renewed interest in recent years in negative tone resists for high resolution lithography. This interest has been driven by the numerous challenges faced by many positive tone materials as features sizes continue to shrink. In particular, the use of small molecules and molecular resists as the base material has received much attention because they appear to offer solutions to many of the problems encountered by early polymeric negative tone resists. Our group has seen excellent performance at sub-20 nm EUV imaging using a negative tone epoxide functionalized molecular resist (4Ep, shown in Figure 1) through the use of novel polymerization control additives.1 Although these types of materials show good patterning capability, they have all been developed in organic solvent where the cross-linking drives the solubility change. Development in aqueous alkaline solutions is favored over organic solvent in high volume manufacturing due to concerns such as cost, waste disposal, environmental health and safety, and other. Since the resist molecules lack sufficient aqueous base solubility, the materials studied so far can only be developed in solvent. In order to overcome this issue, we have synthesized a new molecular resist (3Ep) shown in Figure 1 which can be cleanly developed in standard aqueous alkaline developer. Although 4Ep and 3Ep appear very similar in structure, by leaving one phenolic OH group un-functionalized in 3Ep, the entire molecule becomes soluble in aqueous alkaline soluble. Synthesis of 3Ep is a multi-step process that required separation of the core molecule with different degrees of functionality and determination of reaction conditions which would allow for the desired functional groups to survive each step. While the 4Ep cross-links primarily through epoxide homopolymerization, the phenolic OH group in 3Ep also introduces a new cross-linking mechanism into the resist, epoxide-OH cross-linking, which occurs in addition to the pure epoxide-epoxide cross-linking seen in 4Ep. Comparison of the EUV imaging performance of 4Ep and 3Ep provides insight into the effect of this additional cross-linking mechanism and will be discussed. In addition, the ionizable phenolic group enables 3Ep to be developed in both organic solvent and aqueous alkaline developers such as standard 0.26N TMAH, thus offering a direct comparison between the two development methods. The contrast performance is different in each development method because the solubility switching is determined primarily due to molecular weight increase in organic solvent, while in aqueous alkaline developer there is both a molecular weight solubility effect and a functional group polarity switch as the OH groups are effectively protected when they react with epoxides. This study will show and discuss the EUV imaging performance for both 4Ep and 3Ep and compare the effect of organic solvent and aqueous base development on 3Ep. Figure 2 shows some early EUV imaging performance in 3Ep which is quite promising. Development of such aqueous alkaline developable negative tone molecular resists would add yet another tool to the arsenal of materials and processes that can help realize EUV patterning.

9425-67, Session PS2

Top-coatless 193nm positive-tone development immersion resist for logic application

Lian Cong Liu, Tsung-Ju Yeh, Yeh Sheng Lin, Yu-Chin Huang, Chien Wen Kuo, Wen Liang Huang, Chia Hung Lin, Chun Chi Yu, United Microelectronics Corp. (Taiwan);

Kwang-Hwyi Im, The Dow Chemical Co. (Korea, Republic of); Hae Jin Lim, Hyun K. Jeon, Dow Chemical Co. (Korea, Republic of); Yasuhiro Suzuki, Dow Chemical Co. (Japan); Chengbai Xu, Dow Chemical Co. (United States); Ray Hsu, I-Yuan Wan, Jeff Lin, Dow Chemical Co. (Taiwan)

Improving the defect and litho performances of contact hole (C/H) in the contact and via layers is one of the key requirements to build up logic application (node≤28nm). In this paper, we summarize our development efforts for a top-coatless 193nm immersion positive tone development (PTD) C/H resist with improved litho and defect performances.

The ultimate performance goal was to improve the depth of focus (DoF) margin, mask error enhancement factor (MEEF), critical dimension uniformity (CDU), contact edge roughness (CER), and defect performance. Also, the through-pitch proximity bias was supposed to be comparable to the previous control resist. In this study, various materials have been evaluated by patterning under the 193 nm immersion lithography tool. The material properties focused in the evaluation study were polymer activation energy (Ea), polymerization process type, diffusion length and acidity of photoacid generator (PAG), and embedded barrier layer (EBL) type. Additionally, the impact of post exposure bake (PEB) temperature was investigated for process condition optimization. As a result of this study, a new resist formulation to satisfy all litho and defect performance was developed and production yield was further improved.

9425-68, Session PS2

Novel optical resists with high-refractive index for printable photonic devices

Christophe Peroz, abeam Technologies, Inc. (United States)

We present here a powerful strategy to fabricate micro and nanophotonic devices with high refractive index at low-cost. Novel optical resist materials have been developed with high refractive index and high optical transmission, and are compatible with lithography processes. The optical properties of the films can be tuned by post-annealing [1].

9425-69, Session PS3

Nanoimprint lithography for green water-repellent film derived from biomass with high-light transparency

Satoshi Takei, Makoto Hanabata, Toyama Prefectural Univ. (Japan)

Nanoimprint lithography for green water-repellent film with high light transparency derived from biomass was investigated to modify the fundamental interactions between sugar chain chemical structures derived from biomass and the nanoimprinted surface structures for development of green water-repellent film in nanoimprint patterning dimensional accuracy, by replication of imprint process cycles. The development of the nanoimprint lithography for high 30-40% plant-based green water-repellent film enabled the patterning of a 230 nm pillar on the underlayer over 10 nanoimprint process cycles. The developed green water-repellent film was water repellency with a contact angle for water of about 120 and a high light transparency of more than 90% for wavelength ranging from 450 to 800 nm. The proposed plant-based green water-repellent film are expected to be effective in promoting the future production of advanced nanostructured materials using a source of energy and carbon instead of oil resources.

9425-71, Session PS3

Realistic scaling solution with spacer patterning towards 5nm node

Shohei Yamauchi, Sakurako Natori, Arisa Hara, Masatoshi Yamato, Noriaki Okabe, Kenichi Oyama, Tokyo Electron AT Ltd. (Japan); Hidetami Yaegashi, Tokyo Electron Ltd. (Japan)

EUV lithography is one of the most promising techniques for the next generation lithography, however it is well known that EUVL solutions still face significant challenges. Therefore we have focused on 193 immersion extension using a self-aligned multiple patterning (SAMP). The down scaling of FinFET continues to 10nn node beyond, because 1D cell design based on the SAMP is so much process-friendly. To date, we have demonstrated the effectiveness of self-aligned quadruple patterning (SAQP) and self-aligned octuple patterning (SAOP) as innovative processes and have reported on world-first scaling results at SPIE on several occasions. Under the theme of the 193 immersion extension in existing technology to sub-10nm logic nodes, this paper presents the results of sub-10nm hp resolution testing by SAOP technology and discusses the limits of the cutting patterns for fin or gate layer.

9425-72, Session PS3

Development of spin-on metal hardmask (SOMHM) for advanced node

Shintaro Yamada, Deyan Wang, Vivian Chuang, Charlotte A. Cutler, Cong Liu, Sabrina Wong, Dow Electronic Materials (United States); Michael B. Clark, The Dow Chemical Co. (United States); William Williams, Paul Baranowski, Mingqi Li, Joe Mattia, JoAnne M. Leonard, Peter Trefonas, Kathleen M. O'Connell, Chengbai Xu, Dow Electronic Materials (United States)

With the continuous demand for higher performance of computer chips and memories, devise patterns and structures are becoming smaller and more complicated. Hard mask processes have been implemented in various steps in the devise manufacturing, and requirements for those materials are versatile.

In this paper, novel organometal materials are presented as a new class of spin on solution in order to support the hard mask process. Type of metals, ligands and processing conditions were carefully designed to meet the fundamental requirements as a spin on solution, and their characteristic properties were investigated in comparison to other conventional films such as spin on carbons (SOC), organic bottom anti-reflective coatings (oBARC) and inorganic films formed by chemical vapor deposition (CVD).

Several advantages were identified with these spin on metal hard mask materials over other films which include; 1) better thermal stability than SOC once fully cured, 2) reworkable with industry standard wet chemistry such as SC-1 where conventional Si-BARC is difficult to remove, 3) a wide range of optical constants to suppress reflection for photoresist imaging, 4) high etch resistance, 5) gap filling property. Curing conditions showed a significant impact on the performance of SOMHM films, and X-ray photoelectron spectroscopy (XPS) was utilized to elucidate the trends. With SOMHM film as a BARC, photolithographic imaging was demonstrated under ArF immersion conditions and achieved 45nm LS patterning.

9425-73, Session PS4

A comprehensive approach for micro- and multiple-bridges mitigation in immersion photolithography

Lucia D'Urzo, Entegris GmbH (Germany); Wim Shollaert, JSR Micro N.V. (Belgium); Harold Stokes, Yan Thouroude, Dainippon Screen Deutschland GmbH (Germany)

As efforts to extend 193 nm lithography continue, micro and multiple line bridges are one of the primary challenges in photolithography. These defects originate from several root causes and are difficult to eliminate. Point-of-use filtration plays a significant role on the mitigation of such defects. The impact of filtration rate and pressure was previously documented [1, 2]. In this research, we show how the combination of membrane and pore size selection, photoresist optimization and hardware optimization can impact micro and multiple bridge mitigation in a 45 nm line/space pattern created through immersion lithography.

9425-74, Session PS4

Thickness optimization for lithography process on silicon substrate

Xiaojing Su, Yajuan Su, Yansong Liu, Institute of Microelectronics (China); Yayi Wei, Institute of Microelectronics (China); Fong Chen, Zhimin Liu, Wei Zhang, Bifeng Li, Tao Gao, XMC (China)

With the development of the lithography, the demand for critical dimension (CD) and CD uniformity (CDU) has reached a new level, which is harder and harder to achieve. There exists reflection at the interface between photo-resist and substrate during lithography exposure. This reflection has negative impact on CD and CDU control. It is possible to optimize the litho stack and film stack thickness on different lithography conditions.

In this paper, the film stack optimization can be done for any kind of substrate under different kinds of lithography conditions. A simple structure which has three layers, substrate, Bottom Anti-Reflective Coating (BARC) and photo-resist is considered. The substrate refers to the rest layers except photo-resist. The optimization procedure aims at controlling the reflectivity strictly towards every lithography process with various substrates by choosing the appropriate thickness for photo-resist and BARC. The simulations in this article were done by the Sentaurus Lithography Version I – 2013.12 SP1. For a film stack thickness optimization case, there are several steps to achieve the goals. Firstly, we establish the film stack and resist model. Secondly, the reflectivity curve through a range of thickness of BARC can be simulated. The thickness which corresponds to the first or the second wave trough is the common choice for the BARC thickness. Then we can adjust the thickness of BARC to the best value, which we get a model with the new thicknesses. Thirdly, simulate the swing curve for the new film stack model. We can choose the better photo-resist thickness according to the print CD, peak or bottom of the wave in the swing curve. Fourthly, , we can observe the original resist profile and the optimized resist profile, the zigzags in the original resist profile can be obviously eliminated. Finally, process window analysis can be done after the film stack thickness optimization.

The foundry expected to do some structure contrast experiments for some shallow trench structures to pick out the best one. So the optimizations and evaluations for 5 experiments of shallow trench A and 2 experiments for shallow trench B are done in turn. For the 7 experiments, the best BARC and photo-resist thicknesses are calculated and the process windows (PW) are also analyzed. The result helps foundry choose the appropriate structure, parameters and predict PW before tape-out. Besides, experimental results from the foundry validate the feasibility and reasonability of the method of thickness optimization for lithography process silicon substrate.

There are three distinguish advantages. Firstly, the flow of optimizing the litho stack and film stack thickness on any different lithography condition is introduced in the aspect of methodology systematically. Secondly, with the optimized stack, the total reflectivity for all incident angles at the interface can be controlled less than 0.5%, ideally 0.1%, which enhances process window (PW) most of the time. Finally, the theoretical results are verified by the experiment results from foundry and the best structures were made into production finally.

9425-75, Session PS4

Advanced chemical shrink material for NTD (negative-tone development) resist

Yoshihiro Miyamoto, AZ Electronic Materials (Japan) K.K. (Japan)

This report is about improvement of NTD chemical shrink material.

We will report improvement about XY shrink bias of NTD elongated pattern by developing new shirnk material based on new concept.

9425-76, Session PS4

Microbridge reduction in negative-tone imaging at photoresist point-of-use filtration

Toru Umeda, Shuichi Tsuzuki, Nihon Pall Ltd. (Japan); Tsukasa Yamanaka, Naoya Iguchi, FUJIFILM Corp. (Japan)

The process condition of the point-of-use filtration in photoresist dispensing is known to correlate with excursion of microbridge defects which may trigger critical problems such as disconnection and short circuit. As shown in Figure 1, many studies have been conducted in each lithography generation, to optimize process condition on filtration, and these have generated deep understanding of the requirements for optimization. Some are described below.

In regard to removal mechanism, for sieving effect, fine rated filter is effective especially in non-polar filtration membranes[1-3]. In contrast, polar nylon 6,6 membrane filtration is known to perform greater removal efficiency over sieving based ratings[1,4-8] and adsorption is concluded as the mechanism based on the membrane chemical structure and the observation of contact time dependence in artificial gel challenge tests[7]. Initial CD shift is also studied and the results show that these are predictable and controllable[9,10].

From a different perspective, detailed pump actuation studies for optimized filtration are conducted. As a result, stable flow and low flow rate are found to be effective in microbridge reduction[11,12].

Further, microbridge is also found as a major defect contributor in organic EUV resists[13,14], indicating that filtration is critical also in the future processes.

Above results are based on studies in positive tone imaging (PTI) process. However, as shown in Figure 2, as microbridge is caused by undissolved material in the developers, different polarity on the filter membrane may be desired in recently expanding negative tone imaging (NTI) process. NTI employs organic developer (non polar) in contrast to PTI, which employs alkaline developer (polar). In this study, we focus on the NTI filter optimization and are conducting evaluation for optimized resist point-of-use filtration in NTI process in comparison to PTI. Additionally, newly developed specially cleaned filtration products, which has been found to be effective in wet particle reduction[15] are evaluated for microbridge reduction.

Figure 3 shows the preliminary results of NTI pattern defects (before defect classification, typically relevant to microbridge count) in 45 nm line and space ArF immersion lithography as a function of resist throughput from filter installation. As a result, both filters showed reduction tendency throughout the test duration. As a comparison, both filter showed similar defect count at the beginning, then a 10 nm rated nylon 6,6 with double filtration area surpassed a 20 nm rated nylon 6,6 filter with single filtration area at approximately 3000 ml throughput. The reduction tendency

indicates possibility of relevancy to filter extractables. Higher removal efficiency of the 10 nm rated double area filter after 3000 ml may be due to utilization of the longer contact time between the defect precursor and the filter membrane, or reduced filter rating. Microbridge defect count is further explored in membrane polarity, filter rating, and cleanliness in NTI and PTI and will be presented at the conference.

9425-77, Session PS4

Novel thin film analysis to investigate actual film formation

Kenji Mochida, Shinichi Nakamura, Kazunori Sakai, Tooru Kimura, JSR Engineering Co., Ltd. (Japan); Naoki Man, Hirofumi Seiki, Hideki Hashimoto, Toray Research Ctr., Inc. (Japan)

High performance and low power semiconductor devices showcase the very cutting edge of lithography development. However, the manufacturing of these next generation devices increases in complexity and process length. This is due to the continued scaling of device design, pushing lithographic resolution to the limit. ArF immersion lithography is still used for most promising and mature patterning technologies.

To extend ArF immersion lithography, high quality and high resolution lithographic spin-on organic films are critical. Materials such as photoresists, spin-on carbon hard masks and top anti-reflective layers are needed. We study methods and procedures to identify certain properties of these organic films. We analyze the effects of the actual film formation process as well. Atmospheric, temperature and post-treatment processes change the structure and properties of many organic films. For example, carbon hard mask films cured at 300 and 350 °C show a difference in oxidation and the other chemical structure changes, detected by FT-IR, GCIB-XPS, and GCIB-TOF-SIMS (Fig 1).

Furthermore, photoresist films baked at 105 and 125 °C show a difference in film density detected by PALS. There is a correlation between material performance and the analytical results obtained, so improvements in organic film properties can simplify device manufacturing processes.

9425-78, Session PS4

Patterning variability control through the shrink process

Noriaki Okabe, Tokyo Electron AT Ltd. (Japan)

EUV lithography is one of the most promising techniques for sub-20-nm half-pitch HVM devices, however it is well known that EUV lithography solutions still face significant challenges. Therefore we have focused on 193 based self-aligned multiple patterning, because SAMP easily enables fine periodical patterning. As you know, these spacer based techniques have already been applied to all advanced mass productions. We have already introduced the process friendly SAMP schemes and have demonstrated results in past SPIE sessions. [1][2][3][4] Although SAMP technique can be easily extend to the gridded pattern for 1D layout,?the resolution limit of this 1D design will strongly depend on splitting hole design for the cut-pattern. Furthermore this cut-pattern requires the high precision patterning fidelity of trench or via involving the shrink process. According to resist smoothing treatment before the pattern shrink, this technique can be improved the trench roughness and cross-sectional profile (fig.1). In this paper, we will introduce the demonstration result of fidelity control through the shrink process and discuss about some techniques relevant to them (fig.2).

9425-79, Session PS4

Cost effective processes by using negative-tone development application

Keita Kato, Kei Yamamoto, Keiyu Ou, Michihiro Shirakawa, Sou Kamimura, FUJIFILM Corp. (Japan)

The high volume manufacturing with extreme ultraviolet (EUV) lithography is delaying due to its light source issue. Therefore, ArF-immersion lithography has still been the most promising technology for down scaling of device pitch. As the limitation of ArF-immersion single patterning is considered to be nearly 40nm half pitch (hp), ArF-immersion lithography has necessity to be extended by combination of some kinds of processes to achieve sub-20nm hp patterning.

Recently, there are a lot of reports about the extension of ArF-immersion lithography, e.g., self-aligned multiple patterning (SAMP) and litho-etch-litho-etch (LELE) process. These methods have been realized by the combination of lithography, deposition, and etching. On the other aspect, 1-D layout is adopted for leading devices, which contains additional cut or block litho and etch processes to form 2-D like layout. Thus, according to the progress of down scaling technologies, number of processes increases and the cost of ownership (CoO) can not be neglected. Especially, the number of lithography steps and etching steps has been expanded by the combination of processes, and it has come to occupy a large portion of total manufacturing cost.

We have reported that negative tone development (NTD) system using organic solvent developer have enough resolution to achieve fine narrow trench or contact hole patterning, since negative tone imaging enables to apply bright mask for these pattern with significantly high optical image contrast compared to positive tone imaging, and it has contributed high throughput multiple patterning. On the other hand, NTD system is found to be useful not only for leading device node, but also for cost effective process. In this report, we propose the cost effective process using NTD application. In the viewpoint of cost down at exposure tool, we have developed KrF-NTD resist which is customized for organic solvent developer. Our KrF-NTD resist has resolution comparable with ArF positive tone development (PTD) resist in narrow trench pattern, and it ought to realize downgrade of exposure tool. Also, we propose litho-litho-etch process with NTD resist and planarization materials. This method can reduce etching process and decrease total manufacturing cost more directly.

9425-82, Session PS4

Development of planar spin-on carbon hardmask in various patterns

Jae-Yeol Baek, Dominea Rathwell, Min-Soo Kim, Chung-Heon Lee, Seung-Hee Hong, Byeri Yoon, Hyun-Ji Song, Sang-Kyun Kim, SAMSUNG SDI Co., Ltd. (Korea, Republic of)

No Abstract Available

9425-24, Session 8

Material readiness for generation 2 directed self-assembly (DSA)

Eungnak Han, Todd R. Younkin, Manish Chandhok, David Shykind, Alan Myers, Intel Corp. (United States)

Over the last few years, research into the directed self-assembly (DSA) of block copolymers (BCPs) has seen an increased emphasis within the semiconductor industry. A complementary technique that can augment a wide-array of incoming patterns, DSA offers the promise of (1) density multiplication at a lower cost, (2) the generation of sub-resolution features, (3) reduced pattern variability, and (4) self-aligning strategies with

improved pattern placement error. Internally, we are using a first generation material set based on PS-b-PMMA BCPs to develop DSA into a robust integration strategy. Our development effort is focused on defect density improvements, assessing real integration possibilities in a timely fashion, and correlating simulations to experiment in order to reduce our cycle time and achieve the desired outcome. At the same time, we have made a recent, concerted effort to develop a 2nd generation DSA material set that pushes beyond the inherent resolution limit of PS-b-PMMA (~20-24 nm pitch) but still provides vertical morphologies. Herein, we will provide the current status of our high chi material development effort for DSA at pitches \< 24 nm.

9425-25, Session 8

Directed self-assembly of topcoat-free, integration-friendly high-χ block copolymers

Eri Hirahara, Margareta Paunescu, Orest Polishchuk, EunJeong Jeong, Edward Ng, Jianhui Shan, JiHoon Kim, SungEun Hong, Durairaj Baskaran, Guanyang Lin, AZ Electronic Materials USA Corp. (United States); Ankit Vora, Melia Tjio, Charles T. Rettner, Elizabeth M. Lofano, Chi-Chun Liu, Hsinyu Tsai, Anindarupa Chunder, Amy Bowers, Srinivasan Balakrishnan, Joy Y. Cheng, Daniel P. Sanders, IBM Research - Almaden (United States)

Directed self assembly (DSA) of block copolymers (BCP) is a promising candidate for extending the patterning capability of conventional lithography. PS-b-PMMA is the most widely used block copolymer for DSA. However, the minimum half-pitch of PS-b-PMMA is limited to ~10nm because of a low interaction parameter (χ) between PS and PMMA. Higher-χ block copolymers capable of smaller natural period, the Lo, are expected to be necessary for patterning for sub-10nm nodes IC (integrated circuit) devices. Due to large mismatch between domain-air interfacial energy, various orientation control strategies such as solvent vapor annealing and topcoat have been employed to generate vertically oriented domains from thin films of high-χ block copolymers. However, these strategies introduce additional process complexity in the integration of high-χ block copolymers into standard lithography processes.

Here we demonstrate the orientation control, self-assembly and DSA of novel high-χ block copolymer platforms without topcoat or solvent anneal. Vertically oriented lamellar and cylinder domains with a sub-10nm half-pitch were achieved by simple coat-and-bake process using block copolymer systems with χ higher than that of PS-PMMA chemistry. DSA performances were demonstrated via both topographical and chemical guiding prepatterns. Figure 1A and 1B show graphoepitaxy of ~17 nm pitch lamellae of BCP in 193i resist trench prepatterns. Figure 1C and 1D show chemoepitaxy of ~17 nm pitch lamellae over 84nm pitch chemical prepatterns fabricated using a 193i based LiNe flow. Impacts of process conditions on the DSA performance, as well as pattern transfer of the high-χ block copolymers will be discussed in this paper.

9425-26, Session 9

Driving DSA into volume manufacturing

Mark H. Somervell, Tokyo Electron America, Inc. (United States); Takashi Yamauchi, Soichiro Okada, Tadatoshi Tomita, Takanori Nishi, Shinichiro Kawakami, Makoto Muramatsu, Tokyo Electron Kyushu Ltd. (Japan); Etsuo Iijima, Tokyo Electron Miyagi Ltd. (Japan); Takeo Nakano, Fumiko Iwao, Tokyo Electron AT Ltd. (Japan); Seiji Nagahara, Hiroyuki Iwaki, Makiko Dojun, Koichi Yatsuda, Toshikatsu Tobana, Tokyo Electron Ltd. (Japan); Ainhoa Romo Negreira, Doni Parnell, Tokyo Electron Europe Ltd. (Belgium); Ben M. Rathsack, Tokyo Electron America, Inc. (United States); Kathleen Nafus, Tokyo Electron America (Belgium); Jean Luc Peyre, Tokyo Electron Europe Ltd. (Netherlands); Takahiro Kitano, Tokyo Electron Kyushu Ltd. (Japan)

Directed Self-Assembly (DSA) is extensively being evaluated for application in semiconductor process integration.1-5 Since 2011, the number of publications at SPIE has exploded from roughly 26 publications to well over 80, indicating the groundswell of interest in the technology. Driving this interest are a number of attractive aspects of DSA including the ability to form both line/space and hole patterns at dimensions below 15 nm, the ability to achieve pitch multiplication to extend optical lithography, and the relatively low cost of the processes when compared with EUV or multiple patterning options.

Tokyo Electron Limited has focused its efforts in scaling many laboratory demonstrations to 300 mm wafers. Additionally, we have recognized that the use of DSA requires further movement up the design flow so that robust designs utilizing DSA can be created. To this end, we have discussed the development of a DSA ecosystem that will make DSA a viable technology for our industry, and we have partnered with numerous companies to aid in the development of the ecosystem. This presentation will focus on our continuing role in developing the equipment required for DSA implementation specifically discussing defectivity reduction on flows for making line-space and hole patterns, etch transfer of DSA patterns into substrates of interest, and integration of DSA processes into larger patterning schemes. As an example, the defect map below shows champion defect data on a hole shrink defectivity learning vehicle, and represents a 33% improvement over data previously presented.

9425-27, Session 9

Directed self-assembly process integration for sub-10nm fin patterning

Safak Sayan, Intel Corp. (United States); Boon Teik Chan, Roel Gronheid, Paulina A. Rincon Delgadillo, Arjun Singh, IMEC (Belgium)

Directed Self Assembly (DSA) has the potential to extend optical lithography cost-effectively for sub-10nm nodes and present itself as an alternative pitch division approach. As a result, DSA has gained increased momentum in recent years, as a means for extending optical lithography past its current limits. The availability of a DSA processing line can enable further pushing the limits of 193nm immersion lithography and overcome some of the critical concerns for EUV lithography. Previously we have, successfully demonstrated DSA integration to CMOS process flows for the first time [1]. The integration scheme included cut/keep structures to form fin arrays, relevant film stacks (front-end-of-line device integration such as hard mask stacks, and STI stacks) and was consistent with IMEC's 7nm technology node assumptions [Figure.1]. This demonstration has received significant recognition and served to confirm and reinforce DSA viability as a candidate for sub-10nm technology nodes. [1]

In this contribution, we will present our most recent work on the previously proposed two fin patterning approaches, namely cut-last and cut-1st-HM [1]. These approaches differ with respect to sequence of active area definition. In cut-last approach, active area is defined after pitch division whereas in cut-1st-HM approach, the active area is defined before pitch division [Figure.2]. We will continue our analysis on potential advantages and challenges of each approach.

Conference 9425:
Advances in Patterning Materials and Processes XXXII

9425-28, Session 10

Novel processing approaches to enable EUV lithography toward high-volume manufacturing

Cecilia A. Montgomery, SEMATECH Inc. (United States); Jun Sung Chun, SEMATECH Inc. (United States) and CNSE of SUNY Polytechnic (United States); Yu-Jen Fan, Shih-Hui Jen, Mark Neisser, Kevin D. Cummings, SEMATECH Inc. (United States); Takashi Saito, Lior Huli, David Hetzer, Hiroie Matsumoto, Andrew W. Metz, Vinayak Rastogi, TEL Technology Ctr., America, LLC (United States); M. Warren Montgomery, CNSE of SUNY Polytechnic (United States)

With current improvements in the exposure source power and improvements using novel resist materials; EUV is coming closer to the production environment. Current resists do not meet industry targets, as published in the 2013 ITRS Lithography roadmap. Line width roughness, Pattern collapse, CER, and LCDU are known key issues for EUV Lithography for L/S and CH patterning. In this paper we describe several approaches to using novel processing to improve the final resist pattern.

Post processing techniques, such as pattern smoothing, patterned etch and rinses are known to improve the LWR, CER and LCDU. Double patterning is also known to improve LWR. We combined these two techniques to provide a high throughput EUV process for 15nm half pitch lines and spaces. The high throughput was achieved by selecting high photo speed resists and printing 30nm lines and spaces. Printing this size feature enabled us to use resists with a photo speed of 10mJ/cm2. We then use SADP to double the pattern density to 15nm half pitch and also to smooth the LER and LWR. The LER and LWR of these 15nm half pitch lines and spaces will be described and compared to what can be achieved with single EUV patterning. There has been a lot of progress in metal based resists for EUV recently, but little is known about their post processing behavior. We describe how metal based resists compare to traditional EUV resist after etch and other post processes. Finally we will describe how close all the techniques tested meet the requirements of EUV high volume manufacturing lithography for both line / space and contact holes.

9425-29, Session 10

Integrated fab process for metal oxide EUV photoresist

Andrew Grenville, Jeremy Anderson, Benjamin L. Clark, Joseph Edson, Michael Greer, Kai Jiang, Michael K. Kocsis, Stephen T. Meyers, Jason K. Stowers, Inpria (United States); Alan Telecky, Inpria (United States); Danilo De Simone, Geert Vandenberghe, IMEC (Belgium)

Inpria is developing directly patternable, metal oxide hardmasks as robust, high-resolution photoresists for EUV lithography. Our resists have previously demonstrated process stable imaging and EUV resolution below 10nm half-pitch. Here, we present recent advances in our Generation 2 materials that offer improved photosensivity while maintaining image fidelity. Targeted formulation improvements have enabled N7 node pitches at doses below 40 mJ/cm2 in an ultrathin resist that has greater than 30:1 etch selectivity into a typical carbon underlayer.

In addition to lithographic performance, we review progress in parallel advances required to enable the transition from lab to fab for metal oxide photoresists. This includes considerations and data related to: trace metals qualification, filtration, coat uniformity, edge bead removal, back side rinse, stability, metals cross-contamination, outgassing, susceptibility to out-of-band radiation, rework, strip, and defectivity. We bring this together to demonstrate a fully integrated process flow with full-field exposures on ASML NXE scanners.

9425-30, Session 10

High-sensitivity molecular organometallic resist for EUV (MORE)

James Passarelli, Ryan Del Re, Miriam Sortland, SUNY College of Nanoscale Science and Engineering (United States); Mark Neisser, SEMATECH Inc. (United States); Daniel A. Freedman, State Univ. of New York at New Paltz (United States); Robert L. Brainard, SUNY College of Nanoscale Science and Engineering (United States)

As the resolution of resist materials increases, the thickness of these resist films must decrease in order to maintain proper aspect ratio. As resist films get thinner, the photon absorption of these films decreases. Molecular Organometallic Resists for EUV (MORE) aims to address this problem through the inclusion of high EUV optical density metal centers into resist materials.

We will present on a new resist system that is a subset of MORE. This resist system has demonstrated remarkable sensitivity of Esize = 5.6 mJ/cm2 for 35 nm L/S features (Figure 1). Pattern modulation is also demonstrated down to 16 nm although pattern collapse occurs at these resolutions. This resist system results from the inclusion of a particular functional group that dramatically improves sensitivity. Inclusion of this functional group improves Emax by more than an order of magnitude over an otherwise identical molecule (Figure 2).

This resist system has the following attributes: (1) High Sensitivity—Esize 5.6 mJ/cm2. (2) No latent image after exposure—likely a low outgassing resist. (3) No I-line sensitivity—good for out of band sensitivity. (4) NMR unchanged after three weeks in solution—shows solution stability. (5) Aqueous development or hexane development. We will present on the primary system design as well as lithographic evaluation of several structural variants.

9425-31, Session 10

Development of EUV chemically-amplified resist which has novel protecting group

Shogo Matsumaru, Tatsuya Fujii, Takashi Kamizono, Kenta Suzuki, Hiroto Yamazaki, Masatoshi Arai, Yoshitaka Komuro, Akiya Kawaue, Daisuke Kawana, Taku Hirayama, Katsumi Ohmori, Tokyo Ohka Kogyo Co., Ltd. (Japan)

Extreme Ultra Violet (EUV) Lithography at a 13.5 nm wavelength is being thought to be one of the most promising candidate technologies to replace current optical lithography (193 nm immersion) for the high-volume manufacturing (HVM) of semiconductor devices at the 10 nm node and below. However, EUV lithography process still remains many problems to be solved [1-3]. One of the major challenges is through-put to be able to apply it for HVM. Its development is making progress, but it still seems to be under the target [4]. Therefore, EUV resist needs to play the most important part (faster sensitivity) for HVM requirements, and is strongly required high resolution and better LWR. However, chemically amplified (CA) resists also have challenges to overcome high resolution (R), low LER/LWR (L) and high sensitivity (S) trade-off (RLS-trade-off) [5]. Seeking for solution of RLS trade off, it was reported that increasing of PAG loading ratio into CA resist was good way [6], but this was not successful due to the plasticization effect of PAG molecules resulting in decrease in film glass transition temperature (Tg) [7]. In a CA resist system, acid diffusion control and protecting group (PG) reaction during post exposure bake (PEB) process are the most important factor for improving lithographic performance. To improve resolution, acid diffusion length has to be controlled, however, it causes a decrease in the efficiency of de-protection reaction and resulting in sensitivity loss. Therefore, the enhancement of PG reaction under the acid diffusion control is needed.

In this study, we focused on novel PG materials as having the character of low activation energy (Ea) and high Tg, and will discuss that novel PG

materials could have a potential to overcome those challenges.

At first, it was shown that low Ea PG could improve sensitivity under the low PAG loading ratio. Low Ea PG could be easily and efficiently de-protected through acid catalytic reaction during PEB process even though under low concentration of the acid induced by exposure. So several PG monomers having different Ea were prepared and lithographic performance of the resists consisting of them was investigated (Figure 1). From this experiment, the Tg of base polymer which is influences and induces by PG structure in this case is also dominant factor together with PG reactivity to the acid to control resist performance. One way of controlling acid diffusion length is to increase resist polymer Tg [8]. Resist polymer contains PG unit, adhesion unit and lacton unit, but only PG unit is changed characteristic after exposure and PEB process. So optimization of PG' Tg could improve image contrast between exposure and un-exposure area. Finally, the CA resist which has low Ea and high Tg PG by utilizing EB/EUV exposure tool will be shown and then it will be discussed that novel PG materials could have potentially influential factor for improving RLS trade-off.

9425-32, Session 10

Sensitivity study on the electron affinity of PAG in EUVL

Changwan Bea, Korea Kumho Petrochemical Co., Ltd. (Korea, Republic of)

There are many efforts on the resist material have been tried to improve sensitivity in EUV lithography, such as PBP(polymer bound PAG) and fluorinated resins etc.

In this paper, we report the relationship between the electron affinity and the reactivity of photo acid generator in EUVL. For deep-UV(DUV) resists, absorption coefficient has been optimized by adjusting the concentration or absorption coefficient of cation part of PAGs. This is because the direct excitation of PAGs by incidents photons is a major acid generation path in DUV resist.

However, for EUV resists, the secondary electron from the polymer in resist causes the reaction of photo acid generator. This is because the incidents photon's energy of EUV is too strong to be directly absorbed by PAGs. (EUV: 91.35eV, ArF: 6.5eV, KrF: 5.0eV)

We classify the performance as the substitution of electron withdrawing group to cation part of PAGs and the the number variation of fluorine atom to anion part.

For the substitution of cation part, we investigated the halogen atoms(Fluorine, Chlorine, Bromine, Iodine) and nitro-, nitrile- functional group as the typical electron withdrawing groups.

And for the anion part we evaluate trifluoromethanesulfonate and nonafluoromethanesulfonate.

We found the strong electron affinity of PAGs causes the high acid yield and sensitivity and it also gives changes on the pattern profile.

9425-33, Session 11

The role of guide stripe chemistry in block copolymer directed self-assembly

Robert Seidel, Lance D. Williamson, Paul F. Nealey, The Univ. of Chicago (United States); Youngjun Her, AZ Electronic Materials USA Corp. (United States); Roel Gronheid, IMEC (Belgium)

Directed self-assembly (DSA) of block copolymers (BCP) is attracting a growing amount of interest as a technique to expand traditional lithography beyond its current limits. It has recently been demonstrated that chemoepitaxy can be used to successfully direct BCP assembly to form large arrays of high-density features; a schematic of this process, known as the 'LiNe' flow, is shown in Fig. 1 below. This process uses lithography and trim-etch to produce a "prepattern" of stripes of alternating chemical composition, which in turn guide the formation of assembled BCP structures. The entire process is predicated on the preferential interaction of the respective BCP domains with particular regions of the underlying prepattern. The natural and relative strength of these interactions are at least partially responsible for many aspects of the resulting assembled BCP film, including equilibrium morphology, type and persistence of kinetically trapped defects, and domain roughness.

This study develops the understanding of how various guiding chemistries ultimately govern BCP morphology and characteristics in the LiNe flow. In particular, the work focuses on how stronger affinity between chemical patterns and the guided BCP film leads to faster assembly, lower ultimate defectivity levels, and better incommensurability tolerance, as well as the relationship between pattern strength and domain roughness. One issue in generating finely controllable chemical patterns is that all materials are affected to some degree by processing, which can modify or weaken the guiding ability of the pattern. This investigation addresses the non-idealities introduced in production processing and explores how this knowledge can be employed in improving BCP DSA for lithography.

9425-34, Session 11

Patterning sub-25nm half-pitch hexagonal arrays of contact holes with chemo-epitaxial DSA guided by ArFi pre-patterns

Arjun Singh, IMEC (Belgium) and Katholieke Univ. Leuven (Belgium); Boon Teik Chan, IMEC (Belgium); Doni Parnell, Tokyo Electron Europe Ltd. (Netherlands); Hengpeng Wu, Jian Yin, Yi Cao, AZ Electronic Materials USA Corp. (United States); Roel Gronheid, IMEC (Belgium)

The patterning potential of block copolymer (BCP) materials via various directed self-assembly (DSA) schemes has been demonstrated for over a decade. We have previously reported the HONEYCOMB flow; a process flow where we utilize EUVL and Oxygen plasma to guide the assembly of cylindrical phase BCPs into regular hexagonal arrays of contact holes [1]. In this work we report the development of a new process flow, the CHIPS flow, where we use ArFi lithography to print guiding patterns for the chemo-epitaxial DSA of BCPs. Using this process flow we demonstrate BCP assembly into hexagonal arrays with sub-25 nm half-pitch and discuss critical steps of the process flow. Additionally, we discuss the influence of under-layer surface energy on the DSA process window and report contact hole metrology results.

9425-35, Session 11

DSA graphoepitaxy calibrations for CH multiplication

Stewart A. Robertson, Mark D. Smith, KLA-Tencor Texas (United States); Alessandro Vaglio Pret, KLA-Tencor/ ICOS Belgium (Belgium); Trey Graves, KLA-Tencor Texas (United States); Jan Doise, Joost P. Bekaert, IMEC (Belgium); Roel Gronheid, IMEC (United States)

Directed Self-Assembly (DSA) is a leading candidate for lithographic patterning used in IC manufacturing. With the delay of EUV and the expense of multiple patterning techniques, DSA has the potential to extend ArF and correct EUV variability issues. Graphoepitaxy can be used to shrink a contact hole, or place two or more contacts with only one photolithographic pre-pattern. These obvious size and cost benefits are only possible if lithographic control of CD and LER can be maintained, simultaneously with block co-polymer (BCP) placement accuracy. Moreover, tight process and materials specifications are required to minimize 3D buried defects, only qualitatively measured a posteriori with cross-sections.

In order to control for process variations, the underlying physics and

chemistry should be represented well enough to model the sensitivy to various inputs such as prepattern shape and size, 3D defects, Edge Placement Error (EPE), etc. Here we present results of calibrating a model using one set of patterns, and then extrapolating the model to a different set of patterns. We study the sensitivity to pattern density, BCP film thickness, template properties, and other parameters. We model the detailed optics and chemistry of the photolithographic process in creating the prepattern, as well as the nonlinear and nonlocal effects of the block copolymer anneal. This interaction between detailed experimental results and physical modeling is a critical element in today's lithography.

9425-36, Session 11

Development and integration of systems with enhanced resolutions based on Si-containing block copolymers for line space applications

Guillaume Fleury, Karim Aissou, Muhammad Mumtaz, Univ. Bordeaux 1 (France); Xavier Chevalier, Célia Nicolet, Christophe Navarro, Arkema S.A. (France); Marta Fernandez-Regulez, Patricia Pimenta-Barros, Raluca Tiron, CEA-LETI (France); Cyril Brochon, Eric Cloutet, Georges Hadziioannou, Univ. Bordeaux 1 (France)

While directed self-assembly based on poly(styrene)-b-poly(methylmethacrylate) block copolymers for contact shrink or multiplication applications approaches industrial maturity, new systems with the ability to self-assemble with sub-10 nm features need to be evaluated taking into account the integration requirements (in terms of solvent, thermal budget, etching contrast,...).

In this contribution, two systems based on Si-containing block copolymers will be presented targeting line/space applications. These two systems are characterized by a high segregation strength (Flory-Huggins parameter, ? \> 1) allowing the design of block copolymers with sub-20 nm period while a high etching contrast inherent to the Si-containing block could be achieved between the different blocks.

Firstly original poly(dimethylsilacyclobutane)-b-poly(methylmethacrylate) (PDMSB-b-PMMA) block copolymers showing both lamellar and hexagonal arrays of PDMBS cylinders have been developed. Study of the self-assembly of these materials both on free surface and on patterned substrates show their high potential since long range order arrays can be obtained by a rapid thermal annealing as shown on Figure 1. Besides control of the orientation of the mesostructure are demonstrated for both morphologies and preliminary results on their track integration will be discussed. The second system is based on poly(dimethylsiloxane)-b-poly(lactid acid) block copolymers which self-assemble in a PDMS cylinder mesostructure in the thin film configuration. Such block copolymer system provides an easy access to line/space arrays of parallel PDMS cylinders (see Figure 2) which can be subsequently transferred into the desired stacked layers through plasma etching. Results summarizing this approach will be presented.

Finally, as transfer capabilities into substrates become increasingly more difficult with the reduction of the initial feature size, the optimal conditions leading to aggressive features using dry-etching techniques will be discussed.

9425-37, Session 11

Analysis of the self-assembling and the defect annihilation processes in DSA using meso-scale simulation

Hiroshi Morita, Yuki Norizoe, National Institute of Advanced Industrial Science and Technology (Japan)

It is considered that directed self assembly (DSA) method is one of the important next generation lithography techniques to obtain the shrunk patterns. To obtain the defect-free structure in DSA method constantly, many researchers have studied to control both the block copolymer and the processes. There are many kinds of problems for DSA lithography, such as the pattern near the guide or pattern in the corner, etc. To study these DSA patterning, the meso-scale simulation will be one of the important methods for both the analysis and the design of DSA process.

In the last SPIE, we proposed the several simulation methods to simulate the DSA using meso-scale simulation techniques. For example, self consistent field (SCF) method is applied to DSA simulation by several groups, and we also showed the availability of two-dimensional SCF method as a DSA simulation technique using our simulation system "OCTA." The disadvantage of SCF method is the high cost of computational resources. On the other hand, dissipative particle dynamics (DPD) method is one of the candidates to simulate the DSA process. Using DPD method, we can performed the three dimensional simulation for patterned structure in chemoepitaxy method.

In this study, we performed the DPD simulations to analyze the self-assembling process of block copolymer in DSA. Using DPD simulation, we can obtain the snapshots of the structures consisted by block copolymer chains and an analysis can be done based on the polymer chains. As shown in Fig. 1, the ordering process proceeds as time goes on. In this process, each defect breaks out point by point. We picked up this transition process, and analyzed. In our analysis, ends of polymer chains are focused on. End of polymer chains is one of the singular parts of polymer. For example, conformational entropy of polymer can be obtained by end parts of polymer chains. In this point of view, we check the dynamics of end particles of block copolymer in the ordering process. From our analysis, in the transition process from defect to ordered structures, specific distributions of ends of polymers can be found. In the session, we will present detail of the dynamics of ends of polymer and discuss how to analyze the defect annihilation in the dynamical processes.

9425-38, Session 11

Millisecond laser annealing of sub-10nm directed self-assembly of PS-b-PDMS

Jing Jiang, Brandon M. Wenning, Clemens C. Liedel, Michael O. Thompson, Christopher K. Ober, Cornell Univ. (United States)

Directed self-assembly of blcok copolymer is becoming a practical alternative choice for the next generation nanolithography. High χ block copolymers like PS-PDMS are capable of forming sub 10nm half pitch. However, the higher χ is, the slower the ordering kinetics is. As a result, thermal annealing temperature has to rise to decrease the thermal annealing time. Laser annealing is able to rapidly heat the Si substrate to hundreds of degree and cooled down in milliseconds time frame, preventing the polymer from being damaged. In this study, we applied laser annealing to the PS-b-PDMS and is able to order the parallel PS-b-PDMS from 5ms to 20ms. GISAXS studies reveals the ordering increase at the increasing laser power and heating time. With the help of topography on the Si substrate, PS-b-PDMS is able to align in long range ordering along the trench side walls at sub-10nm half pitch after 20ms laser annealing.

9425-39, Session 12

Dry development rinse (DDR) process and material for ArF/EUV extension technique toward 1Xnm hp and beyond

Shuhei Shigaki, Ryuji Onishi, Rikimaru Sakamoto, Nissan Chemical Industries, Ltd. (Japan)

We newly developed the novel process and material which can prevent the pattern collapse issue perfectly without any special equipment. The process is Dry Development Rinse (DDR) process, and the material used in

this process is DDR material. DDR material is containing the special polymer which can replace the exposed and developed part. And finally, the resist pattern will be developed by dry etching process without any pattern collapse issue. We applied DDR process to EUV PTD process. Resist pattern with 17nm hp was obtained which couldn't be created by previous process because of the pattern collapse.

DDR process was also effective to improve pattern profile and roughness. In our LWR study, LWR was minimized by increasing the bake temperature of DDR material. We found that the formation of inter mixing layer at inter face of PR and DDR material could influence to LWR. According to increase of bake temperature, inter mixing layer was grown and LWR tended to be going down. By optimization of bake temperature, LWR value was minimized and smooth pattern was created.

For the application of DDR process to PTD process, aqueous DDR materials are necessary. We developed the DDR material candidate which has higher stability to water by optimizing the polymer structure. The candidate material showed good aging stability up to 6 months, spin bowl compatibility, film thickness uniformity and defectivity.

DDR process has potential as resolution enhancement technique. For example, pattern sliming process was one of the advanced techniques as ArF extension. By combination of pattern sliming process and DDR process, slimed semi-dense line pattern was over coated by DDR material without any pattern collapse and semi-trench pattern was created after removal of PR pattern by dry etching. In the demonstration of combining sliming process and DDR process, we could create 18nm CD trench by ArF dry exposure condition.

In this paper, we'll discuss the material design for DDR and novel process which combining the DDR and sliming process for ArF/EUV extension toward 1Xnm hp and beyond.

9425-40, Session 12

Impact of dose optimization on NILS, CD, and CDU for helium-ion lithography on EUV resist

Diederik J. Maas, Wouter F. W. Mulckhuyse, TNO (Netherlands); Paul F.A. Alkemade, Nima Kalhor, Technische Univ. Delft (Netherlands)

For the introduction of EUV lithography, development of high performance EUV resists is of key importance. This development involves studies into sensitivity, resolving power and pattern uniformity. These resist attributes can be studied at (future) product resolution using a sub-nanometer-sized 30 keV helium ion beam [1]. We have developed a model to optimize pixel dose for arbitrary patterns, and analyzed the impact of shot noise in the ion dose on CD and CDU for a typical chemically amplified (CAR) EUV resists.

Our approach to optimize ion delivery comprises two steps. In the first step we derive a "requested resist activation map" from the pattern by filtering out unprintable high-spatial-frequency features. In the second step we solve a minimization problem that seeks to find the ion distribution that minimizes the discrepancy between desired dose map and the aerial image resulting from the computed ion distribution. We assume that the resist layer thickness is substantially less than the stopping range of the helium ions, which allows us to ignore dose variation perpendicular to the resist surface. A Gaussian point spread function models the combined resolution blur effect of ion point spread function, forward ion scattering, secondary electron propagation, resist response and processing related effects.

Earlier work [SPIE 2014] reports that a typical EUV CAR is activated at an effective dose of 0.5-2 He+ ions per grid point. Therefore, we anticipate a noticeable effect on CDU from the shot noise in the He+ ion dose. Using our model calculations, we analyzed the impact of the ion shot noise on CD and CDU over a relevant ion dose range.

Pattern fidelity is impacted by the choice of the grid pitch through a few factors such as interaction range, shot noise and imaging quality. We have investigated the quality of the aerial image as a function of the grid pitch by evaluation of the NILS and CDU.

In this paper we show optimized helium-ion dose maps and related resist response profiles for arbitrary patterns in a typical EUV CAR. We used a Gaussian point spread function to account for the combined factors in the activation of EUV resist. Furthermore, the NILS and the contribution to CDU by the shot noise variation in the primary ion dose are evaluated for helium-ion lithography. We aim to determine the effective range of the ion-resist interaction by matching our calculations to experimental results of helium-ion lithography on an EUV CAR.

[1] D. Maas et al., Evaluation of EUV resist performance below 20nm CD using helium ion lithography, SPIE 90482Z, 2014

9425-41, Session 12

Sustainability and applicability of spacer-related patterning towards 7nm node

Kenichi Oyama, Shohei Yamauchi, Sakurako Natori, Arisa Hara, Masatoshi Yamato, Noriaki Okabe, Tokyo Electron AT Ltd. (Japan); Hidetami Yaegashi, Tokyo Electron Ltd. (Japan)

We have reported many demonstrated results of the 193 extension that is due to self-aligned multiple patterning techniques. In particular, focus on the logic device scaling, we have finished the verification of patterning technology of up to 10nm node, we will talk about some patterning technologies that are required to 7nm node.

For critical layers in FinFET devices that presume a 1D cell design, there is also a need not just for the scaling of grating patterns but also for pattern cutting process. In 7nm node, cutting number increase in metal or fin layer, and also pattern splitting of contact or via is complicated, so both cost reduction and process controllability including EPE are strongly required. For example, inverse hardmask scheme in metal layer can improve the variation of the Cu wiring. Further hole shrink technology in contact layer, by the combination with the exposure technique which has k1 0.25 or less, can achieve both cost reduction and reducing the numbers of pitch split. This paper presents the possibility of 193-based multiple patterning techniques for up to 7nm node and discusses about the requirements in 5nm node.

9425-42, Session 12

Fabrication of micro lens array in Benzophenone doped PDMS by using 6 MeV pulsed electron beam

Suresh W Gosavi, Madhushree G. Bute, Sanjay D. Dhole, Vasant N. Bhoraskar, Univ. of Pune (India)

Two dimensional (2D) arrays of small lenses with diameter ranging from several micrometers to nearly millimetre, generally known as Microlens Arrays (MLAs), have diverse applications in micro-optical systems, high-definition displays, photovoltaic devices, biochemical systems, artificial compound eyes and in microfluidic and/or Lab-On-Chip applications.

In recent year's variety of methods for the MLA microfabrication were explored by using; thermal reflow, droplet method, hot embossing, and gray scale photolithography. Major limitation of these methods is that the final quality of the fabricated piece is highly dependent on the quality of the template used. The direct write laser lithography technique is also reported, which is a serial and time consuming process.

Various polymers were used for MLA fabrication, wowing to their properties, appropriate to specific application. Among these materials, Polydimethylsiloxane (PDMS) elastomer has unique physico-chemical properties viz. durability, high dielectric strength, flexibility, stability up to 250?Cand optical transparency above 230 nm. Similarly properties like impermeability to water, nontoxicity to cells, and permeability to gas molecules have made PDMS a potential candidate for bio-Lab-On-Chip applications.

E-beam lithography is an important technique used in IC manufacturing in

micron and submicron region, which cannot be used efficiently for mass production, because of its low throughput. E-beam lithography is reported as one of the processing techniques useful to fabricate microstructure in the cured PDMS stamp. However pits and cone structure formation after the e beam exposure of PDMS is reported in the literature. In order to overcome this, we have chosen the benzophenone as a dopant in the PDMS to enhance the quality of e-beam fabricated microstructures in the PDMS.

This paper reports a novel benzophenone doped PDMS self developable polymer composite resist. In the present work, we have successfully demonstrated a fast single step direct write e beam lithography process used for micro lens array (MLA) fabrication, in ambient condition. A freestanding metal mask of 500 μm thickness having an array pattern of 200 μm circular diameter holes and 100 μm spacing is used in contact mode printing. Lithographic evaluation of 3% doped benzophenone in PDMS is carried out using, 6 MeV energy electron beam which was obtained from microtron, having 2 μsec pulsed width, 50 PPS repetition rate and 2 μA average current. The e-beam fluence used ranging from 1013 to 1015 e/cm2 which corresponds to e-beam dose between 64 and 640 μC/cm2. The observed self developable-beam sensitivity is order of magnitude less than the previously reported one.

The effect of dose variation on (i) benzophenone concentration in PDMS, (ii) Surface roughness of the of the fabricated MLA and (iii) Optical performance of the fabricated MLA is investigated.

9425-43, Session 12

Dry development rinse process for ultimate resolution improvement via pattern collapse mitigation

Safak Sayan, Intel Corp. (United States); Danilo De Simone, Tao Sheng Zheng, Boon Teik Chan, IMEC (Belgium); Michael J. Leeson, Florian Gstrein, Intel Corp. (United States); Geert Vandenberghe, IMEC (Belgium); Yuhei Kuwahara, Kathleen Nafus, Tokyo Electron Kyushu Ltd. (Netherlands)

Pattern collapse currently limits the achievable resolution of the highest resolving EUV photoresists available. The causes of pattern collapse include the surface tension of the rinse liquid and the shrinkage of the resist pattern during the drying step. If these collapse mechanisms can be successfully mitigated with process approaches that do not require changes to the resist itself, the ultimate resolution of existing EUV resists can be improved. Described here is a dry development rinse process, applicable to existing resists, which prevents pattern collapse to both improve ultimate resolution and the process window of currently resolvable features. Reducing the burden of collapse prevention on the resist also allows improvements in line width roughness and cross section profile without and provides additional degrees of freedom for future resist design. As with any proposed patterning enhancement, defectivity is important and preliminary defect performance results will be discussed. Figure: Pattern collapse process window improvement with DDRP as compared to POR process. Cross-sectional line profiles are close to ideal behavior for DDRM, with no top edge rounding which is well pronounced in the photoresist profiles.

9425-44, Session 12

Block co-polymer approach for CD uniformity and placement error improvement in DSA hole grapho-epitaxy process

Tasuku Matsumiya, Tsuyoshi Kurosawa, Masahito Yahagi, Hitoshi Yamano, Ken Miyagi, Takaya Maehashi, Issei Suzuki, Akiya Kawaue, Yoshitaka Komuro, Taku Hirayama, Katsumi Ohmori, Tokyo Ohka Kogyo Co., Ltd. (Japan)

Directed Self-Assembly (DSA) of Block Co-Polymer (BCP) with conventional lithography is being thought as one of the potential patterning solution for future generation devices manufacturing. Many studies have been reported to fabricate the aligned patterns both on grapho and chemoepitaxy for semiconductor application. The hole shrink and multiplication by graphoepitaxy are one of the DSA implementation candidates in terms of relatively simple process and versatility of device design. The critical challenges on hole shrink and multiplication by using conventional Poly (styrene-block-methyl methacrylate) (PS-b-PMMA) BCP have been reported such as CD uniformity, placement error and defectivity. PS-b-PMMA BCP is widely studied including the extension such as the blending polymer, but the relatively weak phase separation ability of PS-b-PMMA BCP would be the one of the root cause of these issues. So it is needed to overcome these challenging issues not only process but material approach. From the material side, the surface treatment material for guide structure, and process friendly BCP material are key development items on graphoepitaxy.

Material design of surface treatment is required in consideration of each actual process and guide structure material. So the specific material development for each device manufacturer process is in-progress at the concept of appropriate surface energy for each BCP structure and also controlled reactivity for each guide material. On the other hand, once guide structure is treated and covered by surface treatment material to show appropriate surface, material design of BCP will become a common issue with less process dependency. In this paper, we will provide the CD uniformity and placement error improvement approach on hole shrink process in graphoepitaxy especially from BCP material.

At first the possibility of PS-b-PMMA BCP extension especially on casting solvent optimization will be shown. The purpose of solvent optimization is improvement of phase separation ability by using appropriate BCP solvent with keeping coating property on guide structure. After the experimental screening of various casting solvents, it was found that some test solvent can improve phase separation ability such as CD uniformity and open yield on finger print evaluation by comparing with conventional solvent. This result indicates that phase separation ability would be promoted by the remaining solvent in the film. It will be discussed what is the key parameter of casting solvent to improve phase separation (for example Hansen solubility parameter, boiling point, viscosity, surface tension etc.). Then high chi BCP material (than PS-b-PMMA) is also studied that is targeting not only smaller CD features but CD uniformity and placement error improvement for hole shrink process in graphoepitaxy including same approach from casting solvent. Finally experimental results on CD uniformity and placement error improvement will be shown and then be discussed on what is the key factor and solution from BCP material approach.

9425-45, Session 13

Progress in spin-on metal oxide hardmask materials for filling applications

Huirong Yao, Alberto Dioses, Salem Mullen, Elizabeth Wolfer, Douglas S. McKenzie, Dalil Rahman, JoonYeon Cho, Munirathna Padmanaban, AZ Electronic Materials USA Corp. (United States)

It is well known that metal oxide films are useful as hard mask material in semiconductor industry for their excellent etch resistance against plasma etches. In the advanced lithography processes, in addition to good etch resistance, they also need to possess good wet removability, fill capability, in high aspect ratio contacts or trenches. Conventional metal containing materials can be applied by chemical vapor deposition (CVD) or atomic layer deposition (ALD). Films derived from these techniques are difficult to control wet etch, low in throughput and special equipment needed leading to high costs. Therefore it is desirable to develop simple spin-on coating materials to generate metal oxide hard masks that have good trench or via filling performances using spin track friendly processing conditions. In this report, novel spin-on type inorganic formulations providing Ti, W, and Zr oxide hard masks will be described. The new materials have demonstrated high etch selectivity, good filling performances, wet removal capability, low trace metals and good shelf-life stability. These novel AZ® Spin-on metal hard mask formulations can be used in several new applications and

can potentially replace any metal, metal oxide, metal nitride or silicon-containing hard mask films currently deposited using CVD process in the semiconductor manufacturing process.

9425-46, Session 13

Aqueous-based thick photoresist removal for bumping applications

John C. Moore, Jared M. Pettit, Alex J. Brewer, Alman Law, DAETEC, LLC (United States)

Cleaning processes account for over 25% of all steps in microelectronic manufacturing [1] bringing the industry to be one of the most chemical intensive. The ITRS are focused on reducing chemical exposure, usage, and waste [2]. These efforts produce a safer working environment, or green factory, and may one day be certified similar to LEED in the building industry [3]. Qualifying aqueous processes meets these objectives while cutting costs by over 50%.

Photoresist (PR) stripping represents high chemical volumes at high cost. Stripping PR during bumping processes commonly uses organic solvents with acidic and alkaline additives [4-6]. Most tooling represents counter-current recycle down-flow units that rely upon complete dissolution. Simple fluid flow reversal can accommodate aqueous removal. Acrylic, novolac, and PHOST, both negative and positive are cleaned with aqueous systems, removing by dissolving and lifting-off. Each bumped wafer can contribute as much as 10g of PR, easily exceeding 1% solids in the tank after one cassette. In less than one day, the tank exceeds 10% solids, 3X the threshold for front-end operations, becoming a risk to yield and generating waste.

Aqueous removers lift-off negative PR from bumps, copper pillars, and RDLs, rinsed from the surface, collected onto a filter, and periodically back-flushed to the trash. The solids become a plastic waste while the liquids are mixed with developer waste and neutralized, filtered, and in most cases, disposed to the sewer. Processes are tuned to perform in \<10min for complete removal. A balanced formula is safe for metals, dielectrics, and eliminates workplace risks [7-8]. A surface tension below 35 dynes/cm provides small geometry penetration, particle removal, and sheet rinsing while foaming is held in check. Agitation by spraying, bubbling, or surface flow minimizes reaction time. Mixtures \>95% water offer superior performance at rates up to 10X faster and bath lives 3X that of organic solvents. Results have been proven on a range of bump shapes in conjunction with PR forms stemming from liquid and dry-film (Fig. 1).

A) Loose pitch B) Tight pitch C) Copper pillar D) T-top

[1] M. Quillen, P. Holbrook, and J. Moore, "Characterizing Solvent Systems for Wafer Cleaning Through Novel Process Modeling on a Laboratory Scale," Semiconductor Processing with Wet Chemicals Conference (SPWCC), February (2007).

[2] International Technology Roadmap for Semiconductors, 2009 ed., Environment, Safety, and Health, www.itrs.net.

[3] Leadership in Energy and Environmental Design (LEED), Green Building Rating SystemTM, U.S. Green Building Council, www.usgbc.org.

[4] J. Moore, "Successful photoresist removal: incorporating chemistry, conditions, and equipment", Proc. SPIE Microlith., Vol. 4690, p. 892-903, (2002).

[5] J. Moore, A. Smith, H. Hendriks, and H. Rapuano, "Rapid and Controlled Processing of GaAs Wafers Using 170 kHz Ultrasonic Agitation," Proc. CS-MAX Comp. Semi. Manuf. Expo., Nov. 11-13, pp. 181-3, (2002).

[6] J. Moore and C. Meuchel, "Characterizing Etch Residue Removal From Low-K ILD Structures Using Aqueous And Non-Aqueous Chemistries," J. Elect. Soc., Oct., (2003).

[7] J.Moore, I.Lorkovic, and B.Gordon, "Rapid Methods of Characterizing Triazole Inhibitors for Copper and Cobalt Processes," CMP Users Group Presentation, AVS Society, Oct., (2005).

[8] J. Marsh, R. Pearson, B. Strickland, J. Moore, and S. Raghavan, "A Review of Semiconductor Manufacturing Applications Using Triazole-Based Inhibitors for Copper and Related Metals," Semiconductor Processing with Wet Chemicals Conference (SPWCC), February (2005). [1] U.S. Patent Nos. 6,869,894, 678,861, 7,098,1527, 7,232,770 J. Moore, 2006-2010.

9425-47, Session 13

Coater/developer process integration of metal-oxide based photoresist

Benjamin L. Clark, Michael K. Kocsis, Michael Greer, Andrew Grenville, Inpria (United States); Takashi Saito, Lior Huli, Richard A. Farrell, David Hetzer, Hiroie Matsumoto, Andrew Metz, Shan Hu, Richard Gaylord, Jeffrey T. Smith, TEL Technology Ctr., America, LLC (United States); Shinchiro Kawakami, Masashi Enomoto, Tokyo Electron Kyushu Ltd. (Japan)

Inpria is pioneering a novel approach to EUV photoresist. Directly patternable metal oxide thin films have shown resolution better than 10nm half-pitch, with robust etch resistance, and efficient use of photons through high EUV absorbance. Inpria's Gen2 photoresists are cast from commonly used organic coating solvents and are developed in typical negative tone develop (NTD) organic solvents. This renders them compatible with CLEAN TRACK LITHIUS Pro-EUV coater/developer system (Tokyo Electron Limited) and solvent drains. The presence of metal in the photoresist demands additional scrutiny and process development to minimize contamination risks to other tools and wafers. In this paper, we review progress in developing coat processes that reduce metal contamination levels below typical industry levels. We demonstrate minimization of trace metals contamination from wafer-to-coater/developer, and wafer-to-wafer from the spin coat process. This will also include results from surface analyses of frontside edge exclusion and backside of wafer using best-known analytical methods. In addition, we discuss results of coat uniformity and defectivity optimization. Wet clean compatibility and dry etch selectivity to bottom anti-reflective coating (BARC) will also be presented. In conjunction with this work, we identify potential contamination pathways and means for managing contamination risk. We furthermore review equipment compatibility issues for using Inpria's metal oxide photoresists.

9425-48, Session 13

BARC/SOC planarization beyond 10nm

Po Tsang Chen, Lian Cong Liu, Jimmy Wu, Kuan Ying Lai, Lucas Chao, Chen Jui Chen, Chia Hsun Tseng, United Microelectronics Corp. (Taiwan)

Gap filling and planarization ability of underlayer is getting difficult as we are approaching to multiple patterning. We have develop the volume theory and successfully predict how underlayer provide planarization ability over the topography, and when underlayer has trouble at gap filling, how the failure of gap filling react on the planarization. This material that we tested in the research include spin-on carbon type underlayer, small organic BARC (with much less carbon %) and pure photoresist to understand the behavior of different type of material over various size/pitch of the pattern structures.

In the past years engineers discuss many times whether should we adopt double coating to get better planarization or how to quantify the planarization result of double coating. Through the planarization test over various size/pitch of the pattern structures, this data is obvious and easy to be quantified. Besides double coating, double baking approach to differentiate the performance between spin-on carbon type underlayer and small organic BARC.

At material vendor side, most of the material test is without RRC (or pre-wet) , and at foundry side, we use RRC mostly. And through the experiment we also found the RRC is related to the gap filling performance and planarization. Also the residue amount of RRC after baking also affect gap filling performance and planarization.

Overall, this paper presents a performance review and analysis on the conventional and novel spin-on planarization processes. The performance of planarization is tested on various etched pattern with different track recipe setting so we can differentiate the relation among material, surface condition and track recipes. The needs for good planarization will be critical for node development.

9425-49, Session 13

Enablement of resist core self-aligned multiple patterning

Jeffrey T. Smith, Nihar Mohanty, David O'Meara, Vinayak Ragosti, Dave Hetzer, Anton deVilliers, TEL Technology Ctr., America, LLC (United States)

As high volume manufacturing transitions from pitch-doubling to pitch-quadrupling, the associated costs and complexity of the process become appreciably greater. Significant development activity focusing on methods to significantly reduce the overall costs of multiple patterning approaches has been on-going in the industry for many years.

One method to reduce this complexity is to use the photoresist as the initial mandrel in the multiple patterning process. This initial soft-mandrel approach offers cost reduction associated with removing several film deposition and etch steps from the overall process flow, however this also presents a new set of processing challenges in terms of constraints on spacer material selection, maintaining good profile control of the soft mandrel throughout the spacer deposition and open, ect.

In this paper we will discuss our work which is enabling resist core multiple patterning as the first step in a self-aligned quad process for BEOL application. This work is spread across four focus points, including:

1. Resist etch trim processes which can maintain the vertical profile, line edge roughness, and CD uniformity control of the resist mandrel. This enables the starting lithography to be done at an optimized 1:1 pitch density in order to maximize the patter fidelity of the starting pattern and utilizing a controlled method to target the desired final mandrel dimensions for the starting point of a quad process

2. New low-temperature spacer materials which provide significantly improved selectivity to commonly used anti-reflective film stacks directly under the photoresist mandrel to mitigate gouging during spacer-open etching which can lead to pitch walking

3. Method for strengthening the resist mandrel through direct current superposition (DCS) which mitigates any photoresist profile distortion during spacer depositions and allows the incorporation of higher temperature spacer materials for the resist core multiple patterning process

4. Incorporation of novel 'non-resist' photoresist platforms to capture the improved LER performance of these materials as soft mandrels and development of associated on-track methods for trimming these materials

Figure 1 shows the current performance of an optimized etch trim process to target good control in trim rates to allow the starting lithography to be done as an equal line / space process. This trim etch process provides very good profile retention and no height loss of the resist mandrel and also provides the benefit of improving the line edge roughness of the mandrel prior to spacer deposition.

We will show current results demonstrating a 16nm half-pitch line / space process incorporating a soft-mandrel approach for the first spacer process utilizing these new technologies to enable resist-core mandrel processing.

9425-50, Session 13

Directly patternable dielectric based on fluorinated polyimide for use in chip packaging

Andrew R. Dick, William K. Bell, Brendan L. Luke, The Univ. of Texas at Austin (United States); Brennan K. Mueller, Georgia Institute of Technology (United States); Brandon M. Rawlings, Intel Corp. (United States); C. Grant Willson, The Univ. of Texas at Austin (United States)

Much effort has been expended in developing polymer dielectrics. At first this was for implementation as an interlayer dielectric material, with polyimides widely explored due their moderate dielectric constants (~2.7-3.5) and thermal stability, even at the very high temperatures required for aluminum metallization. While use as an interlayer material has been superseded by low k and ultra-low k organosilicate glasses, there has been renewed interest in directly patternable dielectrics for packaging applications. This is especially true with the development of 3D architecture and the requirement of increasingly complex wiring to connect a chip to other chips and the package.

The packaging dielectric requirements are quite different than the interlayer materials. Reduction of the dielectric constant is not the primary goal. The amount of material required for a device is also orders of magnitude larger in the case of the package, making commonly used interlayer deposition techniques such as CVD and ALD prohibitively time-consuming and expensive. Current methods of patterning require the use of a separate photoresist or laser ablation, which can damage low k materials.

Most of the work in polyimide dielectrics has either focused on improvement of material properties, or lithographic quality. To the best of our knowledge, no one has been able to print fully cured low k, low CTE polyimides at the resolution and thickness that we describe.

Our method for preparing a directly patternable dielectric utilizes a photochemically generated amine base to partially imidize a poly(amic alkyl ester). The imidized polymer exhibits reduced solubility, forming a negative tone resist. The method is shown in scheme 1. This method has the advantage over various commonly used acrylate-based crosslinking schemes as the cure shrinkage is greatly reduced. This creates fewer distortions in the final printed dielectric, as well as allowing thinner films to be used to print the equivalent final thickness.

The polymers are prepared by low temperature polycondensation of 2,2' bis(trifluoromethyl) benzidine (TFMB) and diester diacid chlorides of pyromellitic dianhydride (PMDA), biphenyl tetracarboxylic dianhydride (BPDA), and cyclobutane dianhydride (CBDA). The materials properties of each of the fully imidized polymers are well established, with all three reported to have sub 3.0 dielectric constant and in-plane coefficients of thermal expansion below 10 ppm/K for PMDA-TFMB and BPDA-TFMB. CBDA-TFMB has a CTE of around 20 ppm/K.

The use of an efficient, low 365 nm absorbance PBG based on a cinnamide allows vastly improved photospeed over the commonly used, but inefficient, nitroveratryl oxycarbonyl (NVOC) i-line PBGs. Addition of a thermal base generator allows for the complete curing of the resist at 200°C. Together, these strategies have created a directly patternable PMDA-TFMB material with dielectric constant around 3 at microwave frequencies and a CTE of 6±2 ppm (thermomechanical analysis) that is capable of printing 6 ?m features in 14 ?m thick films. Figure 1 shows SEM images of the printed dielectric

Conference 9426: Optical Microlithography XXVIII

Tuesday - Thursday 24–26 February 2015

Part of Proceedings of SPIE Vol. 9426 Optical Microlithography XXVIII

9426-1, Session 1

Optical lithography with and without NGL for single-digit nanometer nodes *(Keynote Presentation)*

Burn J. Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

This presentation addresses the challenges to pattern single-digit nanometer nodes. Next generation lithography such as Extreme UV, Multiple E-Beam Direct Write, Directed Self Assembly, and Nano-imprint may or may not help to meet the challenges. Optical lithography may still be needed for all layers, in combination with NGL for relevant layers, or not at all. The consideration will be based on necessary requirements such as overlay accuracy, resolution, CD control, and defects. However, even if all these requirements are met, only a satisfactory cost can dictate the application in high volume manufacturing. Some considerations on costs will also be presented.

9426-2, Session 1

Revolutionizing computing and communications with silicon photonics *(Keynote Presentation)*

Mario J. Paniccia, Intel Corp. (United States)

The silicon chip has been the mainstay of the electronics industry for the last 40 years and has revolutionized the way the world operates. Today a silicon chip the size of a fingernail contains over one billion transistors and has the computing power that only a decade ago would take up an entire room of servers. Recently silicon photonics has attracted a great deal of attention since it offers an opportunity for low cost opto-electronic solutions for applications ranging from telecommunications down to chip-to-chip interconnects as well as possible applications in new emerging areas such as optical sensing and or bio-medical applications. Recent advances and research breakthroughs in silicon photonic device performance over the last few years have shown that silicon can be considered as a material onto which one can build future optical devices. If successful, silicon may similarly come to impact optical communications as it has impacted the electronics industry.

This presentation will provide an overview of silicon photonics at Intel Corporation, describe some of the recent advances including the previously announced demonstration of an integrated silicon photonics optical link operating at 50Gbps and the scalability of this technology to >1Tbps. In addition the presentation will provide an overview and discuss the potential applications and future opportunities for enabling “photonics” in and around the PC and server platform and applications for data center and high performance computing.

9426-3, Session 2

Evolving optical lithography without EUV *(Invited Paper)*

Donis G. Flagello, Stephen P. Renwick, Nikon Research Corp. of America (United States)

Optical lithography has been extended to resolution well below the Rayleigh limit, and is currently being used to print features at one third of the optical wavelength. History has shown that this extension has been made possible using increased lens NA, decreased wavelength, and now multiple processing. However, the success of this extension depends on not only raw technology capability but also economic issues and the need for significant infrastructure additions. The current state of the art is the use of 193nm immersion lithography. The only viable solution to future resolution scaling is either decreasing the wavelength again with extended ultraviolet (EUV) lithography, or further extension of ArF immersion with multiple processing. Both of these have major economic implications.

This talk will examine the evolutionary path of optical lithography without EUV. We explore the previous history to understand the various solutions that have emerged. This will give insight into future possibilities. We will examine the possible limits and fundamental problems moving into the sub-10nm node regime. Finally, the cost implications and infrastructure will also be explored.

9426-4, Session 2

The impact of mask topography induced phase effects and their mitigation by absorber optimization *(Invited Paper)*

Jo Finders, ASML Netherlands B.V. (Netherlands)

We will compare lens aberration induced phase with mask topography induced phase. In magnitude the mask topography induced phase is much larger than current phase by aberrations in the projection lens (see Figure 2). For the mask 3D induced phase we were able to split it into even and odd aberrations looking into the symmetry across diffraction orders. The even phase effects drive the best focus through feature, well known for many years. The odd phase effects lead to contrast loss and pattern asymmetry (left-right differences for two bar structures). Wafer results showing these effects will be presented. Thus, all the effects introduced by lens aberration are also observed but now coming from the Mask topography.

We will show that our optimized absorber, which has lower induced phase range, improves on all features (1D through picth and 2D hotspots) and over all lithographic figures of merit (best focus range, contrast loss).

9426-5, Session 2

Patterning process exploration of metal 1 and via layers in 7nm node with 3D patterning flow simulations

Weimin Gao, Synopsys, Inc. (Belgium); Yves Saad, Synopsys Switzerland, LLC (Switzerland); Kevin Lucas, Synopsys, Inc. (United States); Wolfgang Demmerle, Synopsys GmbH (Germany); Ivan Ciofi, Philippe Matagne, Chris Wilson, Werner Gillijns, IMEC (Belgium)

In 7mn node (N7), the logic design requires the critical poly pitch (CPP) of 42-45nm and metal 1 (M1) pitch of 28-32nm. Such high pattern density pushes the 193 immersion lithography solution toward its limit and also brings extremely complex patterning scenarios. The N7 M1 layer may require a self-aligned quadruple patterning (SAQP) with triple litho-etch (LE3) block process. Therefore, the whole patterning process flow requires multiple exposure+etch+deposition processes and each step introduces a particular impact on the pattern profiles and the topography. In this study, we have successfully integrated a simulation tool that enables emulation of the whole patterning flow with realistic process-dependent 3D profile and topology. We use this tool to study the patterning process variations of N7 M1 and Via layers including the overlay control, the critical dimension uniformity (CDU) budget and the lithographic process window (PW). The resulting 3D pattern structure can be used to optimize the process flow, verify design rules, extract parasitics, and most importantly, simulate the electric field

and identify hot spots for dielectric reliability. As an example application, we will report extractions of maximum electric field at M1 tip-to-tip which is one of the most critical patterning issues and demonstrate the potential of this approach for investigating the impact of process variations on dielectric reliability. We will also present simulations of an alternative M1 patterning flow, with a single exposure block using extreme ultraviolet lithography (EUVL) and analyze its advantages in PW and cost when compared to the LE3 block approach.

9426-6, Session 3

Impact of bandwidth on contrast sensitive structures for low-k1 lithography

Will Conley, Cymer LLC (United States); Simon Hsieh, Cymer Southeast Asia, Ltd. (Taiwan)

Double-patterning ArF immersion lithography continues to advance the patterning resolution and overlay requirements and has enabled the continuation of semiconductor bit-scaling. Over the years Lithography Engineers continue to focus on CD control, overlay and process capability to meet current node requirements for yield and device performance. Reducing or eliminating variability in any process will have significant impact, but the sources of variability in any lithography process are many. The goal from the light source manufacturer is to further enable capability and reduce variation through a number of parameters. (1,2,3,4)

Recent improvements in bandwidth variation have been realized in the XLR platform with DynaPulse technology. This reduction in bandwidth variation could translate in the further reduction of CD variation in device structures. The Authors have studied this impact to determine the improvements realized between AP1 and DynaPulse© technology. The authors will discuss the impact that these improvements in bandwidth variation have on advanced lithography applications. This can translate to improved CD control and higher wafer yields. A simulation study investigates the impact of bandwidth on contrast sensitive device layers such as contacts and 1x metal layers. Furthermore the Authors will discuss the impact on process window through pitch and the overlapping process window through pitch that has been investigated. These improvements will be further quantified by the analysis of statistical bandwidth variation and the impact on CD.

References

1. I. Lalovic et al., Defining a physically-accurate laser bandwdith input for optical proximity correction (OPC) and modeling, Proc. BACUS XXII Photomask Technology Symposium 7122 -62, (2008).

2. P. De Bisschop et al., Impact of finite laser bandwidth on the CD of L/S structures, Journal of Micro / Nanolithography, MEMS and MOEMS (JM3), Vol. 7, No. 3, (2008)

3. M. Smith et al., Modeling and Performance Metrics for Longitudinal Chromatic Aberrations, Focus-drilling, and Z-noise; Exploring excimer laser pulse-spectra," Proc. SPIE Optical Microlithography XX 6520 -127 (2007)

4. U. Iessi et al., Laser bandwidth effect on overlay budget and imaging for the 45 nm and 32nm technology nodes with immersion lithography, Proc. SPIE Optical Microlithography XXIII 7640 (2010).

9426-7, Session 3

Solution for high-order distortion on extreme illumination condition using computational prediction method

Young Seog Kang, Hunhwan Ha, Jang-Sun Kim, Ju Hee Shin, Young Ha Kim, Young Sun Nam, Young-Sin Choi, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Cedric Affentauschegg, Rob W. van der Heijden, ASML Netherlands B.V. (Netherlands); Bernd Geh, Carl Zeiss SMT Inc. (United States); Eric Janda, ASML US, Inc. (United States); Jan Baselmans, Stefan van der Sanden, ASML Netherlands B.V. (Netherlands); Oh-Sung Kwon, ASML Korea Co., Ltd. (Korea, Republic of); Mariya Ponomarenko, Daan Slotboom, ASML Netherlands B.V. (Netherlands)

In this paper we present the limitations of 3rd order distortion corrections based on standard overlay metrology and propose a new method to quantify and correct the cold-lens aberration fingerprint.

As a result of continuous shrinking features of the integrated circuit, the overlay budget requirements have become very demanding. Historically, most overlay enhancements were achieved by hardware improvements. However there also is a benefit in the computational approach, and so we looked for solutions for overlay improvements in process variation with computational applications. Extreme illuminations settings have become common place in advanced DRAM manufacturing in order to successfully print the critical features. The combination of both extreme illumination method and product geometry leads to large sensitivities to aberrations. Additionally the aberration sensitivity induced pattern shift of overlay registration targets differs from that of critical product features.

These differing sensitivities between overlay targets and actual product features can lead to large intrafield distortion differences between the different features. This is especially evident when using extreme dipole illumination and the mismatch can be up to several nanometers. To compensate for this difference, customers perform destructive product testing to quantify this difference and offset the difference to ensure best product feature performance. This mismatch can also vary over time depending on lens performance and process variation, resulting in the need for continuous destructive measurements and long qualification times post various systems maintenance actions.

We present a computational model that combines simulated or measured sensitivities, lens aberration measurements and modelled geometric interactions between successive layers to predict overlay contributions from lens distortions. With this model, it was possible to correctly predict the intrafield overlay of the product feature on multiple systems using only simulated sensitivities. Using an empirical test method (aberration meander), we plan to quantify the aberration sensitivity of metrology targets. By applying the computational model using the measured sensitivities, it should be possible to accurately simulate the distortion and the mismatch between product & metrology features. With this information it is then possible to accurately correct the distortion using aberration tuning products such as Image Tuner & Flexwave, or adjusting the optimization of iHOPC.

In this paper we show the benefit of this accurate computational simulation and the correction potential via optimal lens correction. We tested product distortion and quantified the behavior of the features. Then we made a model based on lens aberrations and geometric effect of metrology artifact of relative displacement between product layers. We were able to get a good match of this model to actual results on multiple systems. With this accurate simulation we can make certain aberration corrections to correct the distortion.

9426-8, Session 3

Optimum ArFi laser bandwidth for 10nm node logic imaging performance

Paolo Alagna, Cymer LCC (United States); Vadim Timoshkov, ASML Netherlands B.V. (Netherlands); Patrick Wong, IMEC (Belgium); Jan Baselmans, ASML Netherlands B.V. (Netherlands); Gregory Rechtsteiner, Omar Zurita, Cymer LLC (United States)

Litho process window and CD uniformity requirements are being challenged with a scaling of all device types. In this study, the impact of bandwidth performance on 10nm node logic Metal 1 layer imaging performance was investigated.

The imaging metrics is contrast, process window, line width roughness and local CDU. The PW changes through bandwidth for Metal1 hot spots and

regular structures. Con of reduced bandwidth is a local intensity variability, and the impact was monitored through LWR and local CDU.

Bandwidth modification could be a potential option in next generation ArFi systems to meet CDU requirements in future nodes.

9426-9, Session 3

Lithographic performance comparison of thin OMOG and attenuated phase-shift masks for 64nm pitch contact holes

Burcin Erenturk, Sohan Singh S. Mehta, Lakshmi K. Ganta, Yuan Lei, GLOBALFOUNDRIES Inc. (United States)

As the 193nm ArF immersion (193i) continues to be the workhorse of the high-volume chip manufacturing for the next years, improving the lithography performance to print finer pitch patterns becomes more important than ever. In this paper, we compared the lithographic performance between thin OMOG (Opaque MoSi on Glass) binary mask and 6% attenuated phase shift mask (att.PSM) to print 64nm pitch contact holes. Depth of focus (DoF), normalized image log slope (NILS), critical dimension uniformity (CDU) across the field, mask error enhancement factor (MEEF), through pitch process window characterization and sub-resolution assist feature (SRAF) printing marginality are studied on silicon and via simulation. Experiments with 1.35NA immersion scanner are performed for both single and double patterning processes. Better resolution and improved DoF, CDU and MEEF were obtained by att.PSM for single and double patterning.

9426-10, Session 3

Single lithography exposure edge placement model

Jacek K. Tyminski, Nikon Research Corp. of America (United States)

The requirement to pack more integrated circuit (IC) functionalities at ever increasing density continues unabated as designers and IC makers continue to pursue Moor's law. To fabricate with the existing imaging tools smaller patterns at higher pattern densities, multi-patterning and multi-exposure lithographic techniques have been adopted in manufacture of advanced ICs. At the same time, the ICs are build layer-by-layer, on top of stacks other patterned layers, while the number of layers in advanced designs continues to grow. Given these design and manufacturing trends, stringent control of the pattern placement becomes key challenge for fabrication of advanced ICs. Indeed, understanding how and where pattern edges are formed becomes paramount when patterns requiring multiple exposure steps are to be successfully fabricated. Controlling pattern edge placement is equally important when the critical patterns fabricated on different layers are to be aligned with each other, with accuracy sufficient to delivering robust performance of the finished ICs.

Placement of the patterns and pattern edges by the lithographic tools is driven by a range of tool characteristics. The most obvious among them is overlay of the exposed pattern fields, representing IC layouts, within wafer coordinates established by the scanner alignment. Scanner manufacturers have developed a range of sophisticated alignment control and overlay correction techniques, to deliver exposure overlay at accuracy of single nanometers. However, in addition to pattern placement responses originating from wafer alignment, the pattern imaging also plays a key role in the pattern edge placement. The obvious link between the imaging and edge placement originates from the fact that the variations of the pattern dimensions, occurring during pattern imaging in the scanners, directly result in local shifts of the pattern edges.

To unify all edge placement contributions into a common, integrated environment, we have developed Single Lithography Exposure Edge Placement (SLEEP) model. It combines alignment and imaging contributions and provides graphical and statistical representation of the pattern edge placement. SLEEP model can be used as edge placement predictor, to analyze the impact of various imaging strategies on characteristics of layers composing ICs. Such analysis is essential to both, IC designers and lithography engineers, striving to successfully fabricate complex designs at economical manufacturing yields.

In this report SLEEP model and its components will be presented and discussed. Examples of SLEEP results based on real scanner performance will be presented. The interaction of the SLEEP alignment and optical components within the model framework will be analyzed with the goal of revealing their contributions to the distribution of pattern edges intra-field and across-wafer. Statistics of across-wafer edge placement performance based on SLEEP model will be presented. Conclusions on the edge placement performance of the current generation of the lithography tools will be presented.

9426-11, Session 4

Multicolor, visible-light nanolithography *(Invited Paper)*

John T. Fourkas, Zuleykhan Tomova, Univ. of Maryland, College Park (United States)

In conventional photoresists, regions that are exposed to electromagnetic radiation have a different solubility than regions that are not exposed. The minimum size and pitch of the exposed regions is directly dependent on the wavelength of light used for exposure, which has driven the push towards photoresists that are exposed by ever shorter wavelengths of light. Inspired by the success of stimulated emission depletion (STED) in improving the resolution of fluorescence microscopy, workers in the field of multiphoton absorption polymerization (MAP) have pursued the development of new photoresists for which exposure is driven with one color of light and inhibited with a second color of light. These methods have facilitated the creation of features that are far smaller than either of the wavelengths of light employed, and correspondingly small pitches. Ultimately, these materials and methods promise to be able to attain feature sizes and pitches that will surpass those of EUV lithography, while being able to create 3-dimensional structures. I will discuss the approaches and materials that are being used, the obstacles that must be overcome to attain the finest possible resolution, and next-generation schemes that promise to address these issues.

9426-12, Session 4

Progresses in 300mm DUV photolithography for the development of advanced silicon photonic devices *(Invited Paper)*

Bertrand Szelag, CEA (France); Charles Baudot, STMicroelectronics (France); Nacima Allouti, Corinne Comboroure, Sebastien Bérard-Bergery, Christian Vizioz, Sébastien Barnola, CEA-LETI (France); Fabien Gays, Denis Mariolle, Commissariat à l'Énergie Atomique (France); Thomas Ferrotti, STMicroelectronics (France) and Commissariat à l'Énergie Atomique (France); Aurélie Souhaité, Stéphane Brision, CEA-LETI (France); Christophe Kopp, Commissariat à l'Énergie Atomique (France); Frédéric Boeuf, STMicroelectronics (France); Sylvie Menezo, CEA-LETI (France)

The first generations of silicon photonic devices were essentially produced in CMOS foundries using available processes. Progressively, with the evolution of this technology, process add-ons are developed to extend our fabrication prospects for the implementation of advanced devices. Thus, the photonic device library is gradually consolidated with objects whose fabrication process is exclusive to silicon photonics. In this paper

we report on advances in DUV photolithography both for etching and implantation of silicon photonic devices. Silicon patterning is a critical building block in silicon photonics because the whole integrated circuit has to be patterned in the Silicon-On-Insulator at one go so that auto-alignment can be achieved. Thus, the challenge is to develop a photolithography that can shoot a selection of curvilinear patterns which vary from very dense networks (line 80nm, trench 80nm) to isolated polygons (few microns). Since, these different patterns are next to each other, density variations and geometric fluctuations result in abrupt changes in lithographic conditions. The singularity of silicon photonic architectures therefore requires a devoted development. Thus, the use of dedicated dummy structures and optical proximity checking rules are essential to ensure a proper lithographic process. Furthermore, it also occurs that some silicon photonic devices need implantation lithographic conditions which are also specific to this technology. For example, waveguides which are 400nm wide need an interlaced channel implantation of 150nm with a pitch of 300nm to fabricate interdigited Mach-Zehnder modulators. For this purpose, we developed a dedicated DUV 193nm implantation lithography to address this need (Fig. 1). The results obtained for the targeted devices are promising and will be overviewed in this paper.

9426-13, Session 4

Double-sided diffractive photomask for sub-500nm resolution proximity i-line mask-aligner lithography

Yannick Bourgin, Thomas Siefke, Thomas Käsebier, Ernst-Bernhard Kley, Friedrich-Schiller-Univ. Jena (Germany); Uwe D. Zeitner, Fraunhofer-Institut für Angewandte Optik und Feinmechanik (Germany) and Friedrich-Schiller-Univ. Jena (Germany)

I-line Proximity mask-aligner lithography is a well known method for the printing of micrometer sized features. In spite of a theoretical resolution in the range of half of the illumination wavelength, the feature size remains five to ten times higher than this value. We propose here diffractive photo-mask designs for the fabrication of structures having sub-500nm resolution by proximity mask-aligner lithography. The method used to increase the resolution of the transferred structures close to the theoretical limit of the i-line wavelength is based on the two-beam interference lithography. A binary diffraction grating located on the bottom side of the photo-mask is illuminated close-to-normal incidence and generates, if the period, the duty-cycle, the depth and the material of the grating are optimized, only the + and – 1st diffraction orders. In the overlapping area of the latter, a high-contrast sinusoidal intensity distribution is generated that has a period half of the one of the phase-mask. Due to the long depth of focus of the generated interferogramm, the wafer to be exposed can be placed several micrometers under the mask, and avoids the need to use the undesired contact mode for the photolithographic transfer. The only modification of the mask-aligner illumination setup is the introduction of an iris aperture to reduce the set of angle in the mask plane close to 0°.

Typically, such high resolution diffractive photo-masks need to be operated with monochromatic and linearly polarized light, which are obtained by placing a spectral filter and a polarizer in the beam path. This is however, a strong limitation, as only one single polarization can be used across the whole mask. Here we demonstrate the use of a UV-wire grid polarizer lithographically patterned on the back side of the photo-mask. As the local orientation of the wire grid polarizer as well as the grating lines of the phase-mask can be chosen arbitrarily it is possible to print sub-wavelength structures with different orientation on the wafer. This permits the fabrication of much more complex optical components such as radial gratings or holograms. A demonstrator consisting in several polarizers located on the opposite side of a 700 nm period phase-mask has been fabricated and 350 nm period linear gratings have been transferred in proximity lithographic mode in our mask-aligner.

Finally, to demonstrate the full potential of this approach, a 500 nm period phase-mask based on a high refractive index binary diffraction grating has been used to print 250 nm period gratings (i.e. 125 nm critical dimension structures). The transfer of the developed resist structure into the fused silica or silicon wafers by dry etching demonstrates that diffractive mask-aligner lithography can produce high aspect ratio sub-wavelength structures. The use of proximity lithography avoids any damage to the mask, and thus increase the life time of the mask and the potential production yield. It enables in fine to make UV lithography a serious alternative fabrication method for sub-micrometer structure with a potentially high throughput, compared to 248 nm or 193 nm lithography.

9426-14, Session 4

Optimization methods for 3D lithography process utilizing DMD-based maskless grayscale photolithography system

Xiaoxu Ma, Yoshiki Kato, Yoshikazu Hirai, Kyoto Univ. (Japan); Floris van Kempen, Fred van Keulen, Technische Univ. Delft (Netherlands); Toshiyuki Tsuchiya, Osamu Tabata, Kyoto Univ. (Japan)

DMD (digital-micromirror-device) lithography is a promising tool for three-dimensional (3D) microstructuring in thick photoresist since it is a maskless process providing rapidness and cost-effectiveness advantages. However, process parameter determination lacks efficient optimization tool, and thus traditional look-up table (indicating the relationship between development depth and exposure dose value under a fixed development time) approach with manual try-and-error adjustment is still gold standard. In this paper, we present a straightforward “input target-output parameters” computational optimization approach for 3D microstructuring utilizing DMD lithography. This numerical optimization based on lithography simulation and sensitivity analysis can automatically optimize a combination of three process parameters for target microstructure; exposure dose pattern, a focus position, and development time. Through a series of experiments and evaluations, validity of the proposed approach has been successfully verified.

Figure 1(a) shows a flowchart of the optimization procedure. Once the target structure is set, exposure dose pattern and development time are optimized under a single focus position for whole target area (Fig. 1(b)) [1]. The profile of 3D structure during development process is simulated based on the dedicated exposure and development simulation for thick-film photoresist [2]-[3]. The transient development profile is used to determine: the optimal development time and the objective function which should be minimized in order to achieve optimized result. Afterwards, modification to parameters based on sensitivity analysis [4] is continued until the accuracy of the simulated results reaches requirement. This procedure is repeated for different focus positions, and finally optimal parameters with the determined single focus position will be output.

In order to validate the proposed approach, the process parameters were optimized for a pyramid structure (Fig. 2). Table 1 lists the optimized parameters and Fig. 3 shows the fabrication results with clear improvement compared to traditional look-up table method. Figure 4 shows the quadratic mean error distribution of simulation and experiment as a function of focus position. The minimum error was obtained at the same focus position, and both simulated and experimental distributions revealed the similar tendency. From above results, the validity of proposed approach has been verified.

Further analysis of optimization results indicates that better target profile has been achieved around focus position comparing to the profile out of focus position (Fig.5). To address this problem, multiple-focus optimization method is proposed: a target structure profile is horizontally sliced by its height then exposed individually with corresponding focus position of the sliced area. The exposure dose pattern for each sliced area is determined by dividing a previously optimized entire pattern with focus position setting shown in Fig.6. Figure 7 shows the relationship between the entire exposure dose pattern and divided ones. Better optimization result was obtained by the multiple-focus optimization (Fig.8). Although, a relatively longer time for multiple exposure process is required, this multiple-focus optimization is a powerful strategy to further improve precision for thicker photoresist structure comparing to the single-focus optimization. In conclusion, the proposed optimization approach reached a state where it can optimize

process parameters on DMD-lithography and complement difficult experimental work on 3D fabrication.

Reference:

[1] F. V. Kempen et al., in Proc. Transducers2013, 1625-1628

[2] J. A. Sethian, "Level Set Methods and Fast Marching Methods", Cambridge: Cambridge University Press, (1999)

[3] Y. Hirai et al., J. Micromech. Microeng., 20, 065005 (2010)

[4] F. van Keulen et al., in Proc. EuroSimE 2009, 1-9.

9426-15, Session 4

Reduced voxel size in two-photon direct laser writing by double exposure

Carsten Eschenbaum, Uli Lemmer, Karlsruher Institut für Technologie (Germany)

Studies on two-photon polymerization (TPP) demonstrated the potential of writing three dimensional nanostructures having a lateral size of about 100 nm. We employ overlapping multiple exposure steps below the polymerization threshold to reduce the voxel size. In this case the voxel size depends on the exposure time, the laser power and in addition on the lateral distance between the Gaussian pulses used for of each exposure step.

The threshold behavior of the two-photon-polymerization allows the fabrication of structures well below the diffraction-limit for the laser wavelength. During the exposure the high photon density in the focal volume excites the photo-initiator via nonlinear two-photon absorption (TPA). The polymerization threshold is defined as the minimal exposure dose which is necessary to sufficiently crosslink the photoresist to remain after the development. In case of a single exposure step the degree of crosslinking is proportional to the dose distribution of the Gaussian pulse. The polymerized volume is called voxel. In theory the voxel size should be infinitely small, nevertheless the minimum voxel size is always limited by power fluctuations of the laser. If the dose drops below a limit the resin will only be partially cross-linked and washed away during the development. To overcome this limitation a spatial separation in-between the two single exposure steps was introduced. The total dose of these two overlapping pulses can exceed the polymerization threshold and leads to smaller voxel sizes compared to a single exposure.

The resulting voxel size was numerically calculated based on the distance between the two pulses, the exposure power and the exposure dose of the single pulses. Therefore the theoretical model of two-photon polymerization was extended to calculate the overall dose, which was compared to the dose of the polymerization threshold. Experimentally a single exposure was compared to a double exposure process with spatially separated exposure steps. For dosages higher than the limit the single exposure resulted in a polymerized structure. In this case the voxel size of the double exposure was increased with the spatial separation of the Gaussian pulses until the critical distance was reached. By reducing the exposure dose below the limit, a single exposure step did not lead to a polymerized structure. Nevertheless with an increasing distance between the two exposure steps the double exposure leads to a reduced voxel size compared to the voxel size limited by the laser power fluctuation.

In summary, we derived a theoretical model to describe the voxel size for a double exposure process with special separation of the single exposure steps. We proved the proposed model by writing multi exposed structures with dosages below and above the polymerization threshold of the SU-8 photoresist. In the case of exposure close to the limitation we could demonstrate a reduced voxel size with increasing spatial distance compared to single exposure.

9426-16, Session 5

Mask-induced best-focus-shifts in DUV and EUV lithography

Andreas Erdmann, Peter Evanschitzky, Fraunhofer-Institut für Integrierte Systeme und Bauelementetechnologie IISB (Germany); Jens Timo Neumann, Paul Gräupner, Carl Zeiss SMT GmbH (Germany)

The mask plays a significant role as an active optical element in lithography, for both EUV and immersion lithography. Mask-induced and feature-dependent shifts of the best focus position and other aberration-like effects were reported both for deep ultraviolet (DUV) immersion and for EUV lithography. We employ rigorous computation of light diffraction from lithographic masks in combination with aerial simulation to study the root causes of these effects and their dependencies from mask and optical system parameters. Special emphasis is put on the comparison of transmission masks for DUV lithography and reflective masks for EUV lithography, respectively.

Rigorous electromagnetic field simulation shows pronounced differences of the intensity and the phase of the diffracted light in comparison to the simplified Kirchhoff description of the mask. Simulation of the phase of diffraction orders of line and space patterns with different pitches reveals a typical phase deformation by the mask. With the exception of the the zero diffraction order, the shape of this phase deformation can be fitted by 4th order Zernike polynomials. The obtained Zernike coefficients provide insight to the type and magnitude of mask-induced aberration effects in DUV and EUV lithography. The so-obtained aberration characteristic of the mask depends on the tonality and size of the considered features. The extracted Zernike coefficients are analyzed versus absorber thickness, sidewall angles, incidence direction and polarization of the illuminating light. The mask-induced aberration-like effects are also investigated by complete imaging simulations, which include a through-pitch analysis of NILS, depth-of-focus, best focus, focus tilt and telecentricity error.

In general, DUV masks show a larger mask-induced variation of the best focus position versus pitch than EUV masks. The effects for DUV masks are dominated by the polarization of the illumination and the orientation of the features. In contrast to that, EUV masks exhibit a strong dependency of the best focus shift from the tonality of the feature. The talk finishes with the discussion of several mitigation strategies for mask-induced focus shifts. This includes tuning of the mask absorber stack, the application of dedicated projector pupil aberrations and modifications of the mask layout.

9426-17, Session 5

Intensity and phase fields behind phase-shifting masks studied with high-resolution interference microscopy

Krishnaparvathy Puthankovilakam, Toralf Scharf, Hans Peter Herzig, Ecole Polytechnique Fédérale de Lausanne (Switzerland); Tina Weichelt, Friedrich-Schiller-Univ. Jena (Germany); Uwe D. Zeitner, Friedrich-Schiller-Univ. Jena (Germany) and Fraunhofer-Institut für Angewandte Optik und Feinmechanik (Germany)

The need of high resolution lithography printing is very prominent these days. Simplest way to get high resolution in proximity printing technology is either by using Phase Shifting Masks (PSM) or by applying Optical Proximity Correction (OPC). Usually, optimized structures are obtained by rigorous simulations and specific for a given proximity distance. There is a direct relation between proximity gaps and optimized structures. In our research we are trying to find out details how light fields behind optimized photo masks develop to determine the best proximity gap of optimized structures and also its evolution in space towards the optimized structures. It is the first time that the experimental analysis of light propagation through masks will be done in details allowing access to intensity and phase including the

possibility to control the coherence of illumination. The instrument we use is known as High Resolution Interference Microscopy (HRIM).

HRIM is a Mach–Zehnder interferometer which is capable of analyzing 3D –light distributions. The interferometer applies phase shifting interferometry which allows precise extraction of information and records the real three-dimensional amplitude and phase fields by scanning the samples in the axial directions. The maximum scanning distance is 500 micron. We usually work with high Numerical aperture objectives, and apply at 405 nm wavelength a Nikon CFI Plan Apo VC 20X/ NA 0.75 dry objectives. The recording of interference fringes is done by a camera (CCD, Scion Corporation, CFW1312M camera with SONY ICX205AK image sensor of 1360*1024 pixels). The camera is placed in the back focal plane of the tube lens. The camera records the 2D images of the current image plane. The field of view is depending upon the magnification of objective lens. If we are using 20X objective, 1 pixel is equal to 232.5nm in object plane. The phase information is tabulated using Schwider-Hariharan Algorithm.

For our experiment it is important to manage the coherence of the illumination to manage diffraction effects accordingly. As a light source 405nm violet- blue LED is used that provides illumination similar to proximity printing machine. We also apply Kohler illumination setup in order to do coherence management. The Kohler illumination has two lenses (condenser lens and collector lens) and two diaphragms (field diaphragm and aperture diaphragm). For phase management a laser at 405 nm will be applied.

Here we present an example measurement of resolution enhancement done for corners using phase shifting mask (PSM) technology. If we add some optical proximity corrections to the phase shifting masks, the resolution enhancement will be much better than regular phase shifting masks.

Corners are the most difficult and commonly used structures in printing technology. Example measurement of corners is targeted for 30 micron proximity gap. Corners are optimized by combination of PSM and OPC [1]. Mask is an alternating aperture phase shift mask (AAPSM). Our characterization techniques allow plotting the 3d image evolution of the optimized structure to the desired structure. We discuss in detail the evolution of intensity fields at different position behind the mask and interpret the main parameters. The measurements give access to tolerances of the wafer positioning and its influence on lateral resolution and contrast. A comparison between resolution and depth of field between PSM and imaging techniques for high resolution lithography will be given.

9426-18, Session 6

Study of cut mask lithography options for sub-16nm metal routing

Yan Wang, Lei Yuan, Chenchen Wang, Jia Zeng, Youngtag Woo, Jongwook Kye, GLOBALFOUNDRIES Inc. (United States)

Printing contact-like cut mask to form the line end of very dense pitches is imposing a significant challenge to lithography, wherein multiple patterning optical solution are needed and EUV is a welcomed alternative due to process simplicity. Different lithography solutions of cut mask will impose different design restrictions and thus lead to different chip scalability. Optical double patterning is the most cost efficient option but has limitations on allowed metal configurations. Optical triple patterning or EUV lithography provides more pattern flexibility but suffers the drawback of added process cost. In addition, the cut mask shape plays an important role in metal line cut process margin given the tight line to line space, where ViaBar like cut mask can improve the accuracy of edge landing but has inverse impact on chip density. In this paper, three optical lithography cut mask options as well as 1 EUV option will be studied for 16nm half pitch metal line patterning for logic design. The options are: 1) optical double patterning with 32x32nm square shape cut mask patterns; b) optical triple patterning with 32x32nm square shape cut mask patterns; c) optical triple patterning with 32x64nm rectangular shape cut mask patterns; d) single EUV cut mask with orthogonal cut mask patterns and minimum feature size of 32nm. Key metal routing rules including minimum metal length, minimum metal space and neighboring line end region space for each cut mask option will be derived based on study of forbidden cut mask configurations. P&R routing experiment with >40K cell logic design will be conducted based on the restricted rules to derive maximum cell utilization, hence minimum logic area with each cut mask option. Cut mask edge placement accuracy will be simulated using the actual routing result. Relative process cost addition of each option will also be calculated. An overall trade-off study between logic area, cost and process marginality of the different optical and EUV cut mask options targeting for sub-16nm half pitch metal pattering will be conducted and summarized in the paper.

9426-19, Session 6

Inverse lithography using sparse mask representations

Radu C. Ionescu, EPFL (Switzerland) and IBM Research – Zürich (Switzerland); Paul Hurley, Stefan Apostol, IBM Research – Zürich (Switzerland)

We present a novel optimisation algorithm for inverse lithography, based on optimization of the mask derivative, a domain inherently sparse, and for rectilinear polygons, invertible. The method is first developed assuming a point light source, and then extended to general incoherent sources.

What results is a fast algorithm, producing manufacturable masks (the search space is constrained to rectilinear polygons), and flexible (specific constraints such as minimal line widths can be imposed). One inherent trick is to treat polygons as continuous entities, thus making aerial image calculation extremely fast and accurate. Requirements for mask manufacturability can be integrated in the optimization without too much added complexity. We also explain how to extend the scheme for phase-changing mask optimization. We seek to address some of the drawbacks of previous inverse lithography methods, namely optimisation time, inaccuracy, inflexibility in imposition of design constraints, and masks impractical to manufacture.

9426-20, Session 6

RET selection on state-of-the-art NAND flash

Neal V. Lafferty, Yuan He, Mentor Graphics Corp. (United States); Jojo Pei, Semiconductor Manufacturing International Corp. (China); Feng Shao, Mentor Graphics Corp. (China); Qingwei Liu, Xuelong Shi, Semiconductor Manufacturing International Corp. (China); Kostas Adam, John L. Sturtevant, Mentor Graphics Corp. (United States)

We present results generated using a new gauge-based Resolution Enhancement Technique (RET) Selection flow during the technology set up phase of a 3x-node NAND Flash product. As a testcase, we consider a challenging critical level for this flash product. The RET solutions include inverse lithography technology (ILT) optimized masks with sub-resolution assist features (SRAF) and companion illumination sources developed using a new pixel based Source Mask Optimization (SMO) tool that uses measurement gauges as a primary input, and also includes 3D mask scattering effects. The flow includes verification objectives which allow tolerancing of particular measurement gauges based on lithographic criteria. Relative importance for particular gauge may also be set, to aid in down-selection from several candidate sources. The end result is a sensitive, objective score of RET performance. Using these custom-defined importance metrics, decisions on the final RET style can be made in an objective way.

9426-21, Session 6

Pixel-based ant colony algorithm for source mask optimization

Hung-Fei Kuo, Wei-Chen Wu, National Taiwan Univ. of Science and Technology (Taiwan); Frederick Li, National Taiwan University of Science and Technology (Taiwan)

Source mask optimization (SMO) is considered one of the key resolution enhancement techniques for node technology below 20 nm prior to the availability of extreme ultraviolet tools. SMOs have been proven to enlarge the process margins for the critical layer in SRAM or memory cells. In this study, a new illumination shape optimization approach was developed based on an ant colony optimization (ACO) principle. ACO is widely used in imaging processing and features rapid searching solutions for complex continuous problems such as image compression, image classification, and image sequence segmentation. Implementing this heuristic pixel-based ACO method in the SMO process provides an advantage over the extant SMO method because of the rapid and stable searching capability of this method. The authors aimed to provide lithographic engineers with references for quick determination of the best illumination shape for complicated mask patterns. The test pattern used in this study was a contact layer for SRAM design.

Fig. 1 displays the schematic layout of the SRAM contact hole mask for testing the optimized illumination performance after applying the newly developed ACO. The minimal feature width was 45 nm, the pitch in the X direction was 110 nm, and the pitch in the Y direction was 90 nm. The illumination optimization procedure started by separating the pupil map into four quadrants and dividing Quadrant I into 225 pixels, as shown in Fig. 2. Each pixel is defined as a point source with the unit intensity and a total of four symmetrically located points in Quadrants II, III, and IV. Second, we applied the modified ACO algorithm based on Eqs. (1), (2), and (3) to determine the critical pixels for a particular mask pattern. The critical pixels were defined as the pixels for which the aerial image intensity exceeded the threshold value. Finally, the critical pixels in Quadrant I were mapped symmetrically to the other quadrants to complete the freeform illumination design. With the completed freeform illumination design, the aerial images were computed and input into the OPC tool in Prolith (KLA-Tencor) for mask layout optimization.

The statistical results were explored using the ArF immersion tool with a wavelength of 193 nm and NA 1.2 to verify the process windows. Table I summarizes the aerial image error results caused by various illuminations. The aerial image error in Table I was defined as the difference between the target and the computed aerial image. The favorable SMO shape produced the most satisfactory results, with an error of 23.86%. Fig. 3 demonstrates the exposure latitude as a function of the DOF for the CH features exposed by various illuminations.

This research has embedded the ACO principle in an SMO algorithm. Statistical analysis indicated that the process window significantly improved after the source shape was optimized using the suggested technique. Our pixel-based ACO optimization technique surpassed the traditional gradient-based technique, which enabled the direct use of MEMS mirror modules in the lithography system to project the calculated illumination shapes.

9426-22, Session 6

Low-contrast photoresist development model for OPC application

Cheng-En R. Wu, Synopsys Taiwan Ltd. (Taiwan); David Wei, Hua Song, Synopsys, Inc. (United States)

The optical proximity correction (OPC) model, a key factor for mask synthesis flow, is getting more and more critical and complicated in the advanced technology node (1Xnm). To achieve a good critical dimension (CD) prediction and model robustness on various types of patterns, a rigorously tuned compact model (RTCM) that takes, as real as possible, the chemistry effects of photoresist into considerations is strongly recommended. The main stages of a lithography process consist of three parts: Exposure, Post-Exposure-Bake (PEB), and Development. The chemistry effect on each stage is governed by different fundamental physics that is to address the effects of light interaction, thermal diffusion and reaction, and interaction with chemical developer, respectively. The final resist profile is determined by the process details of all these stages directly or indirectly.

A better understanding with well-defined physics equations in PEB stage inspired some math techniques such as signal cutting and Gaussian blur, that were widely used in the OPC model society for years to mimic the real chemical effect in a compact way. However, unlike the physics phenomenon in PEB stage, the resist profile influenced by chemical developer in Development stage is less clear and is also less addressed in literatures. A reason that we pay less attention to the chemical developer effect is that it can be modeled simply by thresholding the signal at certain energy level even the resist development process, which is the polymer dissolution fundamentally, is too much complicated. This is based on the truth of high contrast development curve of photoresist which is intentionally designed to behave like this by resist providers.

Recently, the negative tone development (NTD) process, that the development contrast is much lower than traditional types, was widely experimented and showed a promising profile for 1X nm node. However, the conventional signal-threshold model no more works well in this case. It is found that the time dependent development effect dominates the final resist profile that is highly deviated from optical response.

For OPC applications, the RTCM that can specifically characterize the effect of low development contrast is the main focus of this work. Differing from the Gaussian Lumped Parameter Model (GLPM), a more rigorous approach is adopted from the fundamental development rate equation to deduce the compact model with physical insights. A threshold then bias model is proposed by analyzing the development path integral. The development bias can be given in a closed form with limited assumptions so that it can be easily implemented in our compact modeling tool ProGen without losing physical features. A set of data with test patterns in 2D shapes are used for the validation of the proposed compact model. By comparing with traditional threshold-signal model, the proposed threshold-bias model shows a better prediction with fewer fitting parameters that have physical meanings. Finally, we would like to emphasize that the model can be applied generally in both positive tone development (PTD) and NTD process.

9426-23, Session 7

Characterizing the dependence of thick-mask edge effects on feature size and illumination angle using AIMS images

Aamod Shanker, Andrew R. Neureuther, Laura Waller, Univ. of California, Berkeley (United States); Martin Sczyrba, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); Brid Connolly, Toppan Photomasks, Inc. (Germany)

We use through-focus intensity data from an aerial image measurement system (AIMS) tool to experimentally measure thick-mask edge effects in both OMOG and ATT-PSM masks with 193nm light. The phase is recovered using a Transport of Intensity Equation (TIE) based phase imaging method [1]. Phase measurements with an on-axis source (sigma = 0.3) for various sizes of an isolated contact reveal the presence of polarization-dependent electromagnetic edge effects, even when features are smaller than the resolution limit (OPC sized). Since thick mask diffraction occurs primarily at the perimeter of a feature, very small features tend to have significant edge effects relative to their area, causing printing variations through focus. We show that these edge effects can be quantified by fitting to a thin mask boundary layer model. Subsequently, we analyze the impact of both feature size and source shape on thick-mask diffraction both theoretically and experimentally, comparing with predictions from rigorous EMF simulations.

Earlier work used phase imaging of well–resolved contacts to quantify thick mask diffraction effects [2], where the phase signature of diffraction from each edge is resolved and can be directly extracted for comparison with thin

mask boundary layer models [3]. In this work, we extend the analysis to sub-resolution features, where the edge effects are larger than the feature size itself and hence the edge diffraction is unresolved in the recovered phase. The phase imaging method used is based on an iterative version of the Transport of intensity Equation [2], which was developed for recovering the phase of strongly absorbing photomasks. This has enabled phase imaging of various mask types and feature sizes down to the resolution limit.

To extract edge effects in OPC sized features with phase imaging, we first characterize the dependence of electromagnetic edge effects on feature size, showing that they scale with dimension for both opaque and transparent features. Using a phase point spread function formulation, phase images of well-resolved features at the wafer are used to compute thin-mask boundary layer models that approximate experimental edge diffraction. The boundary layer models are then applied to extract individual edge contributions in phase images of sub-resolution features, where the edge effects are typically unresolved. This provides a quantitative interpretation of the phase images at the wafer as a function of edge phase, background phase, and possible crosstalk when edges are in close proximity, all present inherently in the experimental measurements.

Next, to study the dependence of edge diffraction on source shape, the experiment is repeated for an isolated contact feature under off-axis illumination with a quadrupole source. Since oblique illumination angles will modify thick mask edge diffraction behavior, we investigate the extent to which they influence the phase recovered from AIMS measurements. Errors in the phase recovery algorithm due to source shape are separated from changes in electromagnetic diffraction at the mask with the aid of rigorous simulations of the thick mask under off-axis illumination. Once the phase imaging method has been calibrated to the source, the impact of the source shape on the electromagnetic edge effects is then directly analyzed.

References:

[1] M. R. Teague, “Deterministic phase retrieval: a green’s function solution,” J. Opt. Soc. Am. 73, pp. 1434– ?1441, Nov 1983

[2] Aamod Shanker, Martin Sczyrba, Brid Connolly, Franklin Kalk, Andy Neureuther, and Laura Waller.“Critical assessment of the transport of intensity equation as a phase recovery technique in optical lithography.” Proc. SPIE , 9052:90521D-10,2014.

[3] M. Miller, Mask Edge Effects in Optical Lithography and Chip Level Modeling Methods. PhD thesis, EECS Department, University of California, Berkeley, Dec 2010.

9426-24, Session 7

Accurate, full chip 3D electromagnetic field model for non-Manhattan mask corners

Michael Lam, Chris H. Clifford, Michael R. Oliver, David Fryer, Edita Tejnil, Kostas Adam, Mentor Graphics Corp. (United States)

The physical process of mask manufacturing produces absorber geometry with significantly less than 90 degree fidelity at corners. The non-Manhattan mask geometry is an essential contributor to the aerial image and resulting patterning performance through focus. Current state of the art models for corner rounding employ “chopping” a 90 degree mask corner by replacing the corner with a small 45 degree edge. In this paper, a methodology is presented to approximate the impact of 3D EMF effects introduced by corners with rounded edges. The approach is integrated into a full chip 3D mask simulation methodology based on the Domain Decomposition Method (DDM) with edge to edge crosstalk correction.

9426-25, Session 7

A pattern- and optics-independent compact model of Mask3D under off-axis illumination with significant efficiency and accuracy improvements

Hongbo Zhang, Qiliang Yan, David Wei, Ebo H. Croffie, Synopsys, Inc. (United States)

As the critical dimension keeps shrinking, the mask topography effect (Mask3D) becomes considerable to impact the lithography modeling accuracy and the quality of full-chip OPC. Among many challenges in Mask3D modeling, it is critical and particularly demanding to treat off-axis illumination (OAI) properly. With rigorous modeling of Mask3D, the mask near field for each specific light incident angle can be accurately calculated, and the effect of Mask3D to optical imaging can be accurately simulated, provided that a sufficient number of incident angles are chosen to cover and well represent the illumination source. Unfortunately, such rigorous approach is too slow for full-chip applications, and not very useful for production-worthy compact Mask3D modeling.

Among various compact Mask3D modeling methods, one commonly shared drawback is that Mask3D-aware calibration relies and depends on specific test patterns and optical source map. Consequently, such existing models often suffer from compromised accuracy and predictive power due to strong pattern-dependency or process-dependency by overfitting, causing unacceptable sensitivity to mask patterns and process variations.

In this paper, a novel analytical Mask3D compact model is proposed, whose calibration is both pattern- and optics-independent. In the proposed modeling flow, the internal analytical correlations among mask near fields by different light incidents are analyzed and stored in a Mask3D library. The key information in this Mask3D library is then used to guide both mask image generation and optical kernel generation. Because the construction of the proposed Mask3D library only relies on basic process settings (e.g.: wavelength, magnification) and mask stack information (e.g.: layer definition and material setting), this Mask3D model is completely free from any influence of the test patterns and the optical source map. Thus, the calibration process for Mask3D is much simplified, and the common shortcoming in previous compact Mask3D models no longer exists. At the same time, the usability of Mask3D models (e.g.: supporting all-angle mask and ILT) is not compromised.

Furthermore, another great advantage of the new Mask3D model is high numerical efficiency. Compared to the previous Mask3D models, multiple tests of the new method have demonstrated better and more consistent performance on 1D/2D patterns and through focus process windows with negligible runtime impact on the full-chip simulation and OPC. More importantly, changes in the optical source and layout do not require recalibration of Mask3D. The obviation of repeated Mask3D-specific calibration effort promises significant reduction on engineer time/cost in fabs and huge improvement on ease-of-use, reliability and predictability for various optical source and layer patterns.

9426-26, Session 7

Printing circuits with 4nm feature size: Similarities and differences between EUV and optical lithographies

Michael S Yeung, Fastlitho (United States); Eytan Barouch, Boston Univ. (United States)

One of the main concerns about EUV lithography is whether or not it can be extended to very high numerical aperture. Since the mask must be illuminated by obliquely incident EUV light in order to separate the reflected light from the incident light, increasing the NA would require using a larger chief ray angle. This would lead to greater shadowing effect of the absorber and therefore to lower aerial-image contrast, as well as to greater non-telecentricity of the aerial image on the wafer side. Recently, various authors

have suggested the use of alternative mask concepts, multilayer tuning and increased reduction ratio to mitigate some of the problems associated with larger chief ray angles. In this paper, we will explore these concepts further, as well as propose new concepts, to extend EUV lithography to the 4 nm technology node.

9426-27, Session 7

Rigorous wafer topography simulation for investigating wafer alignment quality and robustness

Nicolo Morgana, Infineon Technologies Dresden (Germany); Ulrich Klostermann, Juergen Preuninger, Itaru Kamohara, Synopsys GmbH (Germany); Dmitrii Gavrilin, Synopsys Inc. (Germany); Andreas Greiner, Detlef Hofmann, Holger Moeller, Infineon Technologies Dresden (Germany)

In addition to logic devices, pursuing more than Moore strategy, power products and mixed technologies are manufactured in our facilities. The overlay budget of logic devices shrinks while at the same time processes become more and more complex and combining together different technologies will only sharpen the situation (not forgetting the new challenges brought by power processes).

To maintain cost-competitiveness you are willing to use further the actual tool parks and efficiently distribute the complex product mix. Furthermore with novel applications coming into manufacturing, before investing in updating or improving hardware features you need to understand your requirements in advance.

Most integration schemes are currently maintained taking into accounts mainly device performance and electrical data. Process adaptations are usually implemented within a process unit only. Sometimes these variations (carried out in other processes steps as etch, deposition, cmp ...) do impact the alignment performance in lithography.

Related severe changes in mark contrast have already been observed and some alignment stability issues in lithography been tracked back to process changes in other process units.

Alignment mark evaluations dependent on process changes are time consuming, expensive and hinder short time-to-market scenarios.

We have been testing rigorous simulation software (Synopsys Sentaurus S-Litho) in order to trustfully predict the alignment mark signal quality and mark contrast variation induced by processes changes.

Although this does not make an experimental evaluation of alignment marks on actual wafers redundant, it has the potential yet to reduce the number significantly.

Going further we have applied simulation in order to understand which parameters do mostly influence alignment mark quality, searching for the effective parameters that can be manipulated in order to improve it.

In presence of weak or bad alignment mark signal you have basically to look into two leverages: machine & marks on the wafer (separately and in combination).

Simulation of alignment signals has been done for resist marks and etched marks, coated and uncoated as well as in presence of increasing topology complexity.

We have so explored the influence of adopting distinct alignment modes on different processes steps and products technologies; we have also analyzed the impact of materials variation (i.e. thickness, topology, properties ...) on the alignment quality.

Here for example trenches in Silicium are etched with two different recipes:

Profile can be tuned from rounded to steep, but which one is better suited for a robust alignment mark signal?

Moreover is side wall profile or trench depth the bigger contributor to alignment Mark quality?

And what about resist influence and surface modulation?

To validate simulation analysis, mark signal collection for different processes (and/or variations of those) and products has been carried on; some cross sections have been generated too.

9426-29, Session 8

Investigating deprotection-induced shrinkage and retro-grade sidewalls in NTD resists

Thomas V. Pistor, Panoramic Technology Inc. (United States); Chenchen Wang, Yan Wang, Lei Yuan, Jongwook Kye, Yixu Wu, Paul W. Ackmann, GLOBALFOUNDRIES Inc. (United States)

Two aspects of NTD resists, deprotection-induced shrinkage, and retro-grade sidewalls, are investigated through experimentation and simulation. The goal is to provide insight for improving NTD resist models for OPC.

Previous work has shown that the process of deprotection in chemically-amplified resists can cause mechanical shrinkage of the resist. In the past, with non-NTD resists (ie. PTD resists), the deprotection-induced shrinkage was not of major concern because the shrunken regions were the regions that developed away. However for NTD resists, the shrunken regions are the regions of resist that remain. The shrinkage is predicted to lead to significant CD changes and distortions of the resist pattern.

Simulation also predicts that NTD resists profiles should often have retro-grade sidewall angles due to the attenuation of light as it propagates down through the resist. From a metrology point-of-view, simulations predict that these retro-grade sidewalls should exacerbate the shrinkage effects because the top of the resist, which is free to move, is observed rather than the bottom of the resist which fixed to the substrate. The interplay between the shrinkage and the retro-grade sidewalls will be investigated.

With the help of simulation, experiments are designed to observe and measure both the deprotection shrinkage and the retro-grade sidewall angles. Mask patterns are specifically designed to exhibit varying amounts shrinkage. To discern SEM-induced shrinkage from deprotection-induced shrinkage, SEM measurements will be made at multiple exposure levels so as to be able to extrapolate backwards to the pre-SEM pattern. Both simulated and experimental results will be presented. Effects of neglecting the shrinkage and ways to include it in model-based OPC will also be discussed.

9426-30, Session 8

Alternative to ILT method for high-quality full-chip SRAF insertion

Andrey Lutich, GLOBALFOUNDRIES Dresden Module Two, GmbH & Co. KG (Germany)

Insertion of Sub-Resolution Assist Features (SRAFs) is an inalienable part of the Resolution Enhancement Technology. The main purpose of using SRAFs in optical lithography is through-process-window manufacturability optimization. Typically SRAFs are additional shapes placed in the proximity of the target layer features to support printability of the shapes on the target layer. Placement of the SRAFs with optimum shapes and into right locations is extremely important. Indeed, wrongly inserted SRAF can not only deliver non-optimal advantage, but can also have negative effect on the printability.

Multiple SRAF insertion approaches have been developed and are available to be used in production. Rule-based SRAF generation methods are fast, but not generic and, therefore, require significant engineering efforts for initial set-up and maintenance. Higher SRAF quality at lower recipe complexity is offered by model-based approaches on the price of longer run time. Model-based SRAF insertion approaches can be classified in two major groups: (i) manipulated aerial/resist images are used to seed SRAF insertion and growth and (ii) Inverse Lithography Technology (ILT) generated images

are produced and simplified to fulfil mask manufacturability criteria. ILT is considered to be more preferable because it is information-richer, delivers guidelines not only for locations, but also for shapes of the SRAFs to be inserted. Generating ILT images is a very computation-costly procedure, making ILT approach not feasible to full-chip SRAF insertion in production.

This paper presents the method of linearly-added SRAFs (laSRAF). This method enables generation of ILT-quality guidelines for SRAF insertion at 3+ orders of magnitude faster rate compared to commercially available ILT engines. laSRAF method makes use of a cost function which peaks at the largest process window for a given set of process conditions.

A software package exercising this method has been prototyped in Matlab and tested on real 28nm CA clips up to 100x100 um in size. The method is found to be highly scalable. Extrapolating runtime measurements on clips results in the following estimate: 20 min would be needed to generate ILT-quality SRAF guidelines on a 1 cm2 dense layout with 500 CPUs. Quality of the laSRAF guidelines is found to be comparable to and in some cases better than of nominal ILT.

The laSRAF method itself, its' advantages and limitations along with the runtime and quality benchmarks will be discussed in the paper.

9426-31, Session 8

Uncertainty aware site selection method for OPC model calibration

Tamer H. Coskun, GLOBALFOUNDRIES Inc. (United States)

OPC model calibration requires a set of test structures which are able to represent as closely as possible the entire design domain and modeling space. However, it is equally important to minimize the redundant wafer measurements by carefully selecting a pattern set. Redundant pattern inclusion not only increases metrology time but can also cause over fitting due to nature of the point estimation of root mean square error (rmse) between simulated and measured data. The overfitting can also be minimized by eliminating the redundant data points. Test pattern selection is a time consuming task that involves analysis in terms of pattern geometry and response of the lithography/resist process to these patterns. Traditionally, an image parameter metric has been used to analyze the lithography and resist responses versus the test pattern coverage. This metric assumes a variable threshold resist model which is not necessarily the state-of-the art model type used in the latest technology nodes. Additionally, these methods don't consider the statistical nature of the variations where the number of the selected patterns can greatly affect the uncertainty of the model prediction for another set of patterns. We propose a new method that combines the lithography/resist response with uncertainty analysis to select test patterns for OPC model calibration. This method involves principle component analysis (PCA) to streamline the data analysis. We also explore a new set of metrics to be considered for the calibration of advanced resist models. Examples from advanced nodes are given. For example, Figure 1 shows how the proposed method improves the model quality by minimizing the not accurate patterns. In this figure it is also noticeable that the proposed method balances the model accuracy for both 1D and 2D patterns. Another benefit of the proposed method is shown in Figure 2. This figure shows that the new method gives a verification rmse closer to calibration rmse while reducing the overall rmse which indicates a better predictive model.

9426-32, Session 8

Experiments using automated sample plan selection for OPC modeling

Ramya Viswanathan, IBM Corp. (United States); Omprakash Jaiswal, IBM Corp. (India); Maria Gabrani, Nathalie Casati, IBM Research – Zürich (Switzerland); Amr Y. Abdo, James Oberschmidt, Josef Watts, IBM Corp. (United States)

As we reach physical limits of scaling in chip design, the complexity of the process increases and we are faced with the need to apply novel approaches to this domain, which is the focus of the field of computational lithography.

One such technique, widely used in modern lithography, is called optical proximity correction (OPC).

Currently, mathematically accurate models of the chemical reactions of photo-resist [10] cannot be computed in a reasonable amount of time.

Empirical approximation models are used, which require parameter calibration by fitting to a specific patterns. This set is called the sample plan. The two main challenges of creating a sample plan are adequate design space coverage, and reduced size to address metrology challenges. A novel technique (ASPAR) to quickly determine this best possible sample plan has been demonstrated in [4].

This paper presents experimental verification of this method, in addition to demonstrating the use of this method to effectively reduce the sample plan. Presented here are results of two sets of experiments.

In the first experiment we generated an SP using ASPAR of the same size with a plan of record (POR) SP. We then reduced the size of the ASPAR SP and compared the reduced sizes ASPAR SPs to both the POR (full) and full ASPAR SPs. The verification root mean square (RMS) values were obtained from models generated by the different models using the ASPAR generated reduced size SPs i.e.: (i) the full set, including the < 10% ground rule patterns, (ii) the full set without the <10% ground rule patterns and (iii) the most critical through pitch patterns. These results show that reducing the size of the ASPAR SP by up to 50% has minimal effect in the model quality. This can only be accomplished through the ASPAR methodology that maintains the criticality of the patterns.

In the second set of experiments we were given a POR SP and we usedASPAR to set criticality to the patterns. We then used the criticality to generate SPs of reduced size. The first set full SP (mx80e), and the 100 set is the subset of uniques from mx80e, also called the ASPAR full set. ASPAR was used to select the next six subsets based on criticality, namely, 90, 80, 70, 60, 50 and 40 (Column 1 of Table 1). For each of these subsets, we used the respective 60% of the highest criticality patterns as calibration set and the last 40% as verification set. Some of the patterns that had poor metrology data were removed. The model quality of the different sets and subsets, as this is verified through the calibration and verification RMS values,show that the 100 and 90 models outperform the rest of the models, indicating the criticality of the patterns in these sets. Please note that the 100 and 90 sets outperform the full set (mx80e) even though they have fewer patterns (corresponding to 80% and 65% of the full set). A more detailed explanation of how the ASPAR methodology is used to determine these sets will be provided in the paper. We will also demonstrate how ASPAR can automatically select the minimal SP set.

References:

[1] A. Abdo and R. Viswanathan. The feasibility of using image parameters for test pattern selection during OPC model calibration". In: Proc. of SPIE, Optical Microlithography XXIII. 2010.

[2] M. Al-Imam. Design driven test patterns for OPC models calibration". In: Proc. of SPIE, Optical Microlithography XXII. 2009.

[3] S. Bagheri, D. L. DeMaris, M. Gabrani, D. O. Melville, et al. Method for Fast Estimation of Lithographic Fabrication Diculty of Integrated Circuit Patterns. Patent. FIS8-2009-0202.

[4] N. Casati, M. Gabrani, R. Viswanathan, Z. Bayraktar, et al. Automated sample plan selection for OPC modeling". In: Proc. of SPIE, Optical Microlithography XXVII. 2014.

[5] D. DeMaris, M. Gabrani, S. S. Sarkar, N. Casati, et al. Fast source independent estimation of lithographic difficulty supporting large scale source optimization". In: Proc. of SPIE, Optical Microlithography XXV. 2012.

[6] M. Gabrani and P. Hurley. IC layout pattern matching and classica tion system and method. Patent. CH920080086.

[7] A. Krause, B. McMahan, C. Guestrin, and A. Gupta. Robust Submodular Observation Selection". In: Journal of Machine Learning Research (2008).

[8] A. Krause and D. Golovin. Submodular Function Maximization". In: Tractability: Practical Approaches to Hard Problems (to appear). Cam bridge University Press, 2012.

[9] H. Lin and J. Bilmes. A class of submodular functions for document

summarization". In: Proc. of the 49th Annual Meeting of the Associ- ation for Computational Linguistics: Human Language Technologies. 2011.

[10] C. Mack. Fundamental Principles of Optical Lithography: The Science of Microfabrication. Wiley-Interscience, 2007.

[11] G. Nemhauser, L. Wolsey, and M. Fisher. An analysis of approxi mations for maximizing submodular set functionsl". In: Mathematical Programming (1978).

[12] J. Oberschmidt, A. Abdo, T. Desouky, M. Al-Imam, et al. Automation of sample plan creation for process model calibration In: Proc. Of SPIE, Optical Microlithography XXIII. 2010.

[13] D. Vengertsev, K. Kim, S.-H. Yang, S. Shim, et al. The new test pattern selection method for OPC model calibration, based on the process of clustering in a hybrid space". In: Proc. of SPIE, Photomask Technology. 2012.

[14] G. Viehoever, B. Ward, and H.-J. Stock. Pattern selection in high dimensional parameter spaces". In: Proc. of SPIE, Optical Microlithog raphy XXV. 2012.

9426-33, Session 8

Optical proximity correction with hierarchical Bayes model

Tetsuaki Matsunawa, Toshiba Corp. (Japan); Bei Yu, David Z. Pan, The Univ. of Texas at Austin (United States)

Optical Proximity Correction (OPC) is one of the most important techniques in today's optical lithography based manufacturing process. Currently, the most widely used OPC approach is model-based method, where the fragmented edges are perturbed iteratively to match the predicted image on a wafer calculated by lithography simulation. Although model-based OPC is expected to achieve high accurate correction, it is also known to be extremely time-consuming. This paper proposes a regression model for OPC using Hierarchical Bayes Model (HBM). The goal of the regression model is to greatly reduce the number of iterations in model-based OPC. In our approach, known OPCed layout is used as a training data set and edge types, edge direction or other factors affecting correction value are defined as mixed effects in generalized linear mixed model. Bayes inference technique and non-informative prior distribution are used to learn the optimal parameters from the training data. Furthermore, to estimate the best model parameters, our approach utilizes Markov Chain Monte Carlo (MCMC) method. Experimental results show that utilizing HBM can achieve better solution than other conventional models, e.g., linear regression based model, or non-linear regression based model.

9426-34, Session 8

Application of SEM-based contours for OPC model weighting and sample plan reduction

Marshal A. Miller, Ioana C. Graur, Scott D. Halle, IBM Corp. (United States); Keiichiro Hitomi, Hitachi America, Ltd. (United States)

Continued improvements in SEM contour extraction capabilities have enabled calibrating more accurate OPC models for advanced technology nodes using a hybrid approach, combining CDs for 1D structures and full contour measurements for more complex 2D patterns. Previous work has addressed various components of contour modeling including alignment, edge detection, CD to contour consistency, and image parameter space coverage. This study covers weighting strategies for CDs compared to contours as well as contour-to-contour weighting. Additionally the total number of structures in a sample plan can be reduced by careful selection of calibration patterns based on pattern diversity and image parameters.

Repeated measurements of the same structure at separate locations are used to qcalculate the variation in contour extraction across several instances (Fig. 1). These values give a measure of the pattern variability, induced by both the process variation and the contour extraction itself. This enables a weighting strategy where better behaving structures can be given a higher weight due to improved confidence, while noisier measurements are de-emphasized while still providing visibility to the model calibration.

Using 14nm and 10nm process data, it has been shown that including more contours in hybrid OPC model calibration leads to improved model verification (Fig 2). In addition, within a reasonable range, higher weight on the contour patterns leads to improved model verification on measurement sites unseen by the calibration set. Calibrating a model with fewer contour structures, but at higher weight shows improvement over standard CD only model calibration.

9426-47, Session PS1

High-contrast imaging at hyper-NA using a fully optimized pupil function and polarization state

James J. Jacob, Actinix (United States)

Liquid immersion step and scan systems at 193 nm continue to be the workhorse lithography tools for the semiconductor industry as they are pushed far beyond their original design parameters. Hyper NA projection of photomask images does however present many challenges, one of which is the polarization state of the illuminator. The light diffracted by the finest mask features propagates through the lens pupil and enters the resist at high angles of incidence. The vector property of light polarization at these steep angles must be managed to maintain high contrast printing near the resolution limit. Specifically, hyper-numerical aperture optical systems require an azimuthal or TE polarization state of illumination for high image contrast. If the light is un-polarized or is polarized in the TM state, the image contrast for fine features will degrade significantly. Specially made optical polarization plates, liquid crystals and micro-mirror arrays have been utilized for azimuthal vector polarization control with some success. This paper describes a time-lapsed imaging method in which the polarization vector and pupil function are fully optimized using conventional optics.

The key aspects of the imaging system are shown in Fig. 1. A linearly polarized 193 nm laser illuminates the mask, but in this case the polarization state of the laser is time-varying, as a half-wave plate polarizing element is rapidly rotated, thereby creating a continuous linear sweep in polarization space. The photomask is thus illuminated by a swept linearly polarized beam, some of the mask features being illuminated properly with the TE state and some with the low contrast TM state, and some with in-between states. The diffraction spectrum of light is a two-dimensional map of the Fourier components of the mask representing the polar orientation of the features and their spatial frequencies. This diffraction spectrum is spatially filtered at the pupil plane of the imaging lens which then performs an inverse Fourier transform to form the resist image on the wafer.

To ensure that the unwanted spatial frequency components do not pass through the imaging lens, the pupil function of the imaging lens is a rectangular slit that is rapidly rotated and is precisely synchronized to the rotating waveplate in the illuminator. In this fashion only the mask diffraction components illuminated by the corresponding correct azimuthal polarization vectors pass though the slit. A high contrast image is then formed in a time lapsed exposure in which the polarization of the diffraction spectrum is fully optimized.

This vector imaging method is also applicable to wide-field immersion microscopy, where it could possibly find use in the optical inspection of defects on wafers and photomasks. The enhanced contrast at hyper NA will also aid in the high resolution imaging of biological cell structure, especially in applications where label-free or non-invasive methods must be used to maintain cell viability. This paper will describe the vector imaging concept and provide a simulation of the imaging results. Preliminary data will be given showing a comparison in the contrast of hyper-NA microscopy images with and without the vectorial compensation.

9426-48, Session PS1

Comparing the experimental resist image with image intensity in high-NA projection lense

Masato Shibuya, Tokyo Polytechnic Univ. (Japan); Akira Takada, Topcon Corp. (Japan); Toshiharu Nakashima, Nikon Corp. (Japan)

By taking care of the conservation law of energy or that of radiance, scalar imaging theory has been completed to be self-consistent theory. Even though Hopkins theory is correct and self-consistent in mathematical expression, since its expression by a text is rather ambiguous, it has been a little incorrectly understood. Therefore, we will review and reconsider scalar imaging theory from the view point of both the conservation law of energy and the self-consistency. This argument is important and necessary to discuss and construct vector imaging theory

In practical imaging, we should consider the vector imaging. However we think vector imaging theory might not have been completed. One reason is that electric field intensity contradicts with pointing vector (or photon number) on resist surface. In order to resolve this contradiction, we have considered the practical thickness due to the oblique incidence. Then we have phenomenologically obtained the vector imaging theory. We have confirmed the validity of this theory by comparing the results of numerical calculation with experimental results in high NA projection lens. Since in optical lithography the required pattern width is very fine and necessary preciseness of width is also severe, the comparing is valuable and meaningful.

We are not completely sure and further discussion should be necessary. But our proposal will be useful and valuable for optical lithography and fundamental optics.

9426-49, Session PS1

Advanced process characterization using light source performance modulation and monitoring

Paolo Alagna, Omar Zurita, Gregory Rechtsteiner, Cymer LLC (United States)

As DUV multi-patterning requirements continue to become more stringent, it is critical that all sources of lithography patterning variability are characterized and monitored. Advanced process characterization studies have been enabled using Cymer's novel technique to modulate Energy, Bandwidth, or Wavelength light source performance at the intra-wafer (field-to-field) level. This technique has been instrumental in helping identify process sensitivities that enable proactive light source monitoring and excursion detection using SmartPulse.

Demonstration of this the benefits of this technology are provided through results from recent experiments at IMEC. Changes in patterning performance are characterized using scatterometry and top down CD-SEM metrologies, enabling excellent correlation between optical parameters and on-wafer attributes such as CD or Side Wall Angle (SWA) for typical patterning geometries. In addition, new results show that changes in laser beam parameter performance can have measurable wafer patterning and illumination impacts for simple and complex structures. Chipmakers can benefit from the use of this capability to perform proactive, comprehensive characterization of current and next generation process nodes.

9426-80, Session PS1

Analytical analysis for impact of polarization aberration of projection lens on lithographic imaging quality

Lina Shen, Shanghai Institute of Optics and Fine Mechanics (China) and Xinjiang Normal Univ. (China); Sikun Li, Xiangzhao Wang, Guanyong Yan, Shanghai Institute of Optics and Fine Mechanics (China)

In hyper-NA lithography systems, the polarization aberration of projection lens leads to imaging degradations. Typically, numerical simulations [1] are used to explore the relationship. In this paper, analytical analysis for the impact of polarization aberration of projection lens on the aerial image of alternating phase-shift mask (Alt-PSM, as shown in Fig.1) is realized. The analytical expressions of image placement error (IPE) and best focus shift (BFS) caused by polarization aberration are derived from the intensity of aerial image. The derived expressions match simulation results extremely well, as shown in Fig.2, and can be used to understand more fully the detrimental impact of polarization aberration on lithographic imaging quality. The linear relationships between IPE and odd items of Pauli-Zernike polarization aberrations, as well as that between BFS and even items of Pauli-Zernike polarization aberrations are established, using linear polarization illumination. These relationships act as technical base for exploring polarization aberration test and compensation methods. The accuracy of the linear relationships is assessed by the least square method.

9426-50, Session PS2

Reducing the substrate dependent scanner leveling effect in low-k1 contact printing

Ching Shun Chang, Macronix International Co., Ltd. (Taiwan)

As the scaling down of design rule for high-density memory device, the small depth of focus (DOF) budget may be deteriorated by focus leveling errors, which arises in unpredicted reflectivity from multilayer structures on the topology wafer. The leveling sensors of ASML scanner use near infrared (NIR) range wavelength which can penetrate through most of films using in semiconductor fabrication such as photo-resist, bottom anti reflective coating (BARC) and dielectric materials. Accordingly, the reflected light from underlying substructures would disturb leveling sensors from accurate leveling. The different pattern densities and layout characteristics between array and periphery of a memory chip are expected to yield different leveling signal. Furthermore, the process dependent variations between wafer central and edge areas are also considered to result in different leveling performances during wafer exposure.

In this study, lower blind contact immunity was observed for peripheral contacts comparing to the array contacts especially around wafer edge region. In order to overcome this problem, a series of investigations have been carried out. The wafer edge leveling optimization through circuit dependent focus edge clearance (CDFEC) option didn't get improvement. Air gauge improved process leveling (AGILE) function of ASML immersion scanner didn't show improved result either. The inter layer dielectric (ILD) uniformity improvement and step height treatments around wafer edge such as edge exclusion of film deposition and bevel etching were also ineffective to mitigate the blind contact problem of peripheral patterns. Altering the etch hard-mask stack was finally found to be an effective approach to alleviate the issue. For instance, through either containing high temperature deposition advanced patterning film (APF) in the hard-mask or inserting higher opaque film such as SiON and amorphous Si in between the hard-mask stack.

9426-51, Session PS2

A fast and flexible library-based thick-mask near-field calculation method

Xu Ma, Jie Gao, Xuanbo Chen, Lisong Dong, Yanqiu Li, Beijing Institute of Technology (China)

As the critical dimension (CD) shrinks into the wavelength or sub-wavelength realms, thick-mask effects become increasingly pronounced, and the Kirchhoff approach is no longer accurate. In this case, the near-field of thick-mask can be calculated by the rigorous electromagnetic field (EMF) simulations. Although accurate, the rigorous methods are too slow to simulate large-scale masks. To keep balance between the accuracy and efficiency, a set of approximate near-field calculation methods have been developed.

In general, there are three types of approximation methods to calculate thick-mask near-field, referred to as the filter-based methods, boundary-layer (BL) methods and domain decomposition methods (DDM). The filter-based methods modify Kirchhoff model using filtering techniques in spatial, frequency or pupil domain. Meanwhile, the BL methods treat the mask near-field as the superposition of the interior transmission areas and boundary layers. However, the degrees of freedom in these above methods are fixed by the number of the calibrated parameters. On the other hand, DDMs decompose the mask into isolated edges, and use the diffracted field of each edge from a library to stitch up the near-field. The library of DDM contains the pre-calculated diffracted fields from different types of edges, which guarantee the diversity of the library samples. However, as the CD continuously shrinks, the near-field becomes more sensitive to the three-dimensional mask topography, incidence angle and illumination polarization. Thus, it is preferred to develop a more flexible method to simulate and characterize the thick-mask near-field.

This paper combines the library-based approach and data-fitting approach to propose a flexible thick-mask near-field calculation method with higher degree of freedom. Specifically, a set of typical features, such as convex corners, concave corners and edges, are selected from a training mask to serve as the library samples. Then, the near-fields of these library samples are calculated using FDTD method and saved for reuse. Given an arbitrary test mask, we first decompose it into several pieces around the convex and concave vertices and edge observation points. Then, we match each piece to the library samples based on nonparametric kernel regression method. Subsequently, we use the matched near-fields in library to replace the pieces of test mask, and rapidly synthesize the entire near-field for the test mask. As the numerical aperture of current optical lithography systems increases, higher frequency components of the near-field concentrated around mask corners may have more impacts on lithography imaging. Based on this concern, our proposed method extends the traditional DDMs by taking into account the mask corners during near-field synthesis. In addition, we adopt a data-fitting method to further increase the degree of freedom of the proposed method, and improve the accuracy of the synthesized near-field. In particular, we use a polynomial of the synthesized near-field to approximate the actual near-field, where the polynomial coefficients are fitted by least square estimate (LSE) using another training layout. Simulations based on a complex test mask show that the proposed method can speed up the current FDTD method by a factor of 2554, and effectively improve the accuracy of the Kirchhoff approach.

9426-52, Session PS2

Focus shift impacted by mask 3D and comparison between Att. PSM and OMOG

Yansong Liu, Xiaojing Su, Zhiyang Song, Moran Guo, Yajuan Su, Institute of Microelectronics (China); Yayi Wei, Institute of Microelectronics (China); LiSong Dong, Institute of Microelectronics of Chinese Academy of Sciences (China)

The impact of mask three dimension (Mask 3D) effect on lithography processes is getting more pronounced in smaller technology nodes. It can no longer be neglected since 32nm nodes.

In this paper, we report four research progresses on the basis of Mask 3D effect. All the experiments are simulated on the platform of ASML Brion Tachyon. Firstly, the impacts of Mask 3D effect on the best focus (BF) are studied. Various patterns with different CDs and pitches are selected for simulations. In order to single out the focus drift issue, we exclude the patterns that have large depth of focus (DOF) and their lithographic process windows are insensitive to focus at a given illumination condition, such as the small pitches (90nm to 115nm). The Mask 3D effect has negative impacts on the best focus (BF), generating the BF bias among various features. The BF bias depends strongly on the thickness of the absorber layer, but not so much on its sidewall angle (SWA). Secondly, opaque MoSi film is used in OMOG (Opaque MoSi on Glass) mask as an absorber to replace thick Cr. We calculate dependence of the OMOG mask transmission on the MoSi thickness in the range of 30nm to 60nm. The transmission increases sharply as the thickness of MoSi decreases from 40nm to 20nm. The optimum thickness is proposed at 47.5nm. Thirdly, thicker MoSi in mask creates more unbalanced intensity between 0th and 1st orders and makes contrast better. But, it leads to smaller space CD in wafer and higher mask error enhancement factor (MEEF). This phenomenon is much more noticeable for the pitch 90nm and the space smaller than 50nm. For small mask space, thick MoSi enlarges MEEF but inversely for large mask space. So the trade-off between contrast and MEEF still needs to be further studied. Finally, the lithography process window (PW) of Cr on glass (COG), OMOG and attenuated phase-shifting mask (Att.PSM) are compared comprehensively by using the 22nm SRAM design. Absorber thickness, source mask optimization (SMO), and Optical Proximity Correction (OPC) are all included in the discussion matrix. Including the Mask 3D effect into SMO model can enlarge the overlapped PW. OMOG and Att. PSM are comparable at peak performance while OMOG is more stable through mask duty ratio and has less M3D impact.

9426-53, Session PS2

UDOF direct improvement by modulating mask absorber thickness

Enchuan Liu, Dennis Yu, Po Tsang Chen, Chia Hsun Tseng, Kuei-Chun Hung, Charlie Chen, United Microelectronics Corp. (Taiwan)

As the process generation migrate to advanced and smaller dimension or pitch, the mask and resist 3D effects will impact the lithography focus common window severely because of both individual depth-of-focus (IDOF) decreasing and center mismatch induced by 3D effects. Furthermore, some chemical or thermal factors, such as PEB(post-exposure bake) also worsen the usable depth-of-focus (UDOF) performance. So the mismatch of thru-pitch IDOF center should be considered as a lithography process integration issue, and more complicated to partition the 3D effects induced by optical or chemical factors.

In order to reduce the impact of 3D effects induced by both optical and chemical issues, and improve IDOF center mismatch, we would like to propose a mask absorber thickness offset approach, which's directly to compensate the IDOF center bias by mask absorber thickness biasing, for iso, semi-iso or dense characteristics in line, space or via patterns to enlarge common process window, i.e UDOF.

Btw, since mask absorber thickness offset approach is similar to focus tuning or change on wafer lithography process, it could be act as the process tuning method of PR profile localized optimization to improve PR scumming in specific patterns or to modulate etching bias to meet process integration request.

For mass production consideration, and material available, current a-PSM blank, quartz, MoSi with Chrome layer as hard-mask in reticle process, will be implemented in this experiment, i.e. Chrome will be kept remaining above partial thru-pitch patterns, and act as the absorber thickness bias in different patterns. And then, from the best focus offset of thru-pitch patterns, the IDOF center shifts could be directly corrected and to enlarge UDOF by increasing the overlap of IDOF. Beside positive tone development

(PTD), some negative tone development (NTD) result will be demonstrated as well.

9426-54, Session PS3

120W ArF laser with high-wavelength stability and efficiency for the next-generation multiple-patterning immersion lithography

Takeshi Ohta, Gigaphoton Inc. (Japan)

ArF exicmer lasers are expected to be the main solution in the next generation multiple-patterning photolithography due to the difficulty of EUV lithography system development. For the next generation lithography, smaller CD with reduced cost and the potential extension to 450mm wafers introduces extremely difficult performance challenges on lasers.

New ArF Laser, GT64A has been developed to support the next generation multiple-patterning process. It offers the industry's highest output power of 120W with high wavelength stability and efficiency.

Basic improvements applied to the GT64A are high output power and wavelength stability to meet the requirements for the next generation multiple-patterning lithography and 450mm wafers. The GT64A can deliver up to 120W of output power. The industry's highest lasing efficiency is achieved through the proven Injection Lock technology. No additional utilities are required by this 120W light source, and the ingenious optical configuration makes it possible to maintain stable beam qualities.

The automatic output adjustment function enables the output power to be dynamically optimized to meet the specific requirements of customers' processes. Furthermore, this function can also prevent the generation of unneeded power, thus contributing to the reduction of the operational cost and environmental impact.

The wavelength-stability of the GT64A has been improved by approximately 50% compared to previous models. This enables very high overlay accuracy, CD control, and small LER required by the next generation multiple-patterning process technologies.

Another important feature of the next generation lasers will be the ability to support green operations while further improving cost of ownership and performance. For example, electricity consumption costs and the dependence on rare gases, such as neon and helium, will become critical considerations for HVM process going forward. As a laser vendor, Gigaphoton continues to innovate and develop solutions that address these important issues. The GT64A has reduced environmental impact while upgrading performance and power. Two effective green technologies are applied to the GT64A.

The first is the reduction of gas usage. More than 96% of the gas used by the lasers is neon. Another rare gas that requires attention is Helium. Recently the unstable supply of neon and helium became a serious worldwide issue. To cope with this situation, Gigaphoton is developing lasers that support reduction of neon usage and completely helium-free operations. GT64A has a new advanced gas control algorithm in which parameters, such as input power and gas pressure are closely monitored during operations and feed back to the injection/exhaust gas controller system. By this new gas control, the laser gas consumption can be reduced by up to 50%.

The second green technology targets improvement of efficiency. Gigaphoton's Injection-Lock architecture was proven to be superior in efficiency compared with traditional MOPA systems. Gigaphoton is developing a new chamber that reduces the electricity consumption by another 19% by reducing of cross flow fan rotation speed.

These technologies and the detailed properties of GT64A with actual data will be shown.

9426-55, Session PS3

Forbidden pitches: causes, source optimization, and their role in design rules

Stefan Apostol, Paul Hurley, IBM Research – Zürich (Switzerland)

Forbidden Pitches (FPs) are the result of unwanted, non-linear effects that limit yield, and not always well understood. Yet, as approximations, they are implicitly deployed through design rules. Many believe they result as a consequence of more complicated illumination sources. We develop an analytical model of aerial image quality as a function of light source. We show the effect is most pronounced for a point light source, the simplest of all. We develop a method to improve print image quality by illumination source optimization, and show promising first results. Additionally, it is shown how design rules unsatisfactorily capture forbidden pitches.

9426-79, Session PS3

Source optimization using particle swarm optimization algorithm in photolithography

Lei Wang, Sikun Li, Xiangzhao Wang, Guanyong Yan, Chaoxing Yang, Shanghai Institute of Optics and Fine Mechanics (China)

In recent years, with the availability of freeform sources, source optimization has emerged as one of the key techniques for achieving higher resolution without increasing the complexity of mask design. In this paper, an efficient source optimization approach using particle swarm optimization algorithm is proposed (Figure 1). The sources are represented by pixels and encoded into particles. The pattern fidelity is adopted as the fitness function to evaluate these particles. The source optimization approach is implemented by updating the velocities and positions of these particles. This approach is demonstrated by using two typical mask patterns, including a periodic array of contact holes and a vertical line/space design. The pattern errors are reduced by 66.1% and 39.3% respectively. Compared with the source optimization approach using genetic algorithm, the proposed approach leads to faster convergence while improving the image quality at the same time (Figure 2). The robustness of the proposed approach to initial sources is also verified.

9426-56, Session PS4

Advanced Mask Aligner Lithography (AMALITH)

Reinhard Völkel, Uwe Vogler, Arianna Bramati, SUSS MicroOptics SA (Switzerland)

Mask Aligners are very attractive for less-critical litho layers in BEOL, LED, Displays, MEMS, Advanced Packaging (AdP), Image Sensor Packaging, Micro-Fluidics, etc.. Mature technology, high throughput, ease of operation, low maintenance, moderate capital expenditure and attractive cost-of-ownership (CoO) are the key factors. Advanced Mask Aligner Lithography (AMALITH) comprises different measures to improve shadow printing lithography technologies beyond the limits: Customized Illumination, OPC, Phase Masks (AAPSM), Grey-Level Lithography, Talbot and Pinhole Talbot Lithography have been implemented with much success. We report on the next steps like the integration of UV diode lasers and 193nm excimer lasers and present examples for applications in research and industry.

9426-58, Session PS5

An improved virtual aberration model to simulate mask 3D and resist effects

Motokatsu Imai, Reiji Kanaya, Koichi Fujii, Nikon Corp. (Japan); Lin Qun Ying, A*STAR Institute of Microelectronics (Singapore); Tomoyuki Matsuyama, Takao Tsuzuki, Nikon corporation (Japan)

As shrinkage of design features progresses, optical lithography faces ever-challenging requirements such as how to improve critical dimension (CD) control beyond tool and process limitations. Depth of focus continues to be a key parameter for improving process CD control.

However, DOF for sub-wavelength lithography is becoming shallower due to the larger NA of a projection lens and smaller dimensions, and the difference in best focus position for different patterns is becoming a fatal issue. In advanced immersion lithography, common usable DOF is only about 100nm when many patterns co-exist in a layer, even in ideal cases. But in the real world of wafer printing, various factors such as aberrations in a projection lens, mask 3D topography effects, and resist thickness effects shift the best focus positions, and the amount of shift differs depending on the patterns. This will result in smaller common usable DOF.

The first step to solve this problem is to understand and estimate these factors correctly. In this paper, mask 3D topography and resist 3D effects are emphasized among the factors which impact the best focus position. The aberrations in projection optics have already been thoroughly investigated and can be easily measured with a PMI (Phase Measurement Interferometer) tool equipped on scanners. However, mask 3D and resist 3D effects are still under investigation.

It is well known that mask 3D topography effects can be simulated by many EMF analysis methods such as FDTD (Finite-Difference Time-Domain) and RCWA (Rigorous Coupled Wave Analysis). However, it is almost impossible to use it for full chip modeling because these methods are extremely computationally extensive. Consequently, it usually applies only to a limited range of mask patterns, which are about tens of square micro meters in area.

On the other hand, the effects of resist thickness on the best focus position are rarely treated as a subject of lithography investigations. Resist 3D effects are treated mostly for resist profile prediction, which also requires expensive EMF analysis for accurate predictions. In addition to the complexity of EMF calculation itself, it usually has much lower predictabilities compare to mask 3D topography effects.

In this paper, Virtual Aberration (VA) model is presented. It covers mask 3D-induced effects and resist thickness effects. A conventional simulator, when applied with these improved methods, can factor in both mask 3D and resist thickness effects. Thus it can be used to model inter-pattern best focus difference issues with the least amount of rigorous EMF analysis.

It is realized by following the steps below:

1. Formulate the resist thickness effect to equivalent pseudo Zernike 0_ terms.

2. Simulate mask 3D effects for several patterns with some discrete pitches.

3. Formulate the mask 3D-induced phase deviations between diffraction orders as a function of pattern pitch and illumination NA by rigorously analyzing several typical structures which could be on a mask.

4. Then the inter-pattern best focus Difference can be simulated by adding the resist thickness-induced pseudo Zernike terms and the mask 3D induced phase deviations in diffraction orders into conventional litho-simulator.

9426-59, Session PS5

Evaluation of compact models for negative-tone development layers at 20/14nm nodes

Ao Chen, Yee Mei Foong, GLOBALFOUNDRIES Singapore (Singapore); Dong Qing Zhang, Hongxin Zhang, GLOBALFOUNDRIES Inc. (United States); Angeline Chung, Mentor Graphics Corp. Singapore (Singapore); David Fryer, Yunfei Deng, Dmitry M. Medvedev, Yuri Granik, Mentor Graphics Corp. (United States)

With the introduction of negative tone develop (NTD) resists to production lithography nodes, multiple NTD resist modeling challenges have surpassed the accuracy limits of the existing modeling infrastructure developed for the positive polarity process. We report the evaluation of two NTD resist modeling algorithms. The new modeling terms represent, from first principles, the NTD resist mechanisms of horizontal shrink and horizontal development bias. Horizontal shrink describes the impact of the physical process of out-gassing on remaining resist edge location. Horizontal development bias accounts for the differential in the peak and minimum development rate with exposure intensity observed in NTD formulations. We review specific patterning characteristics by feature type, modeling accuracy impact presented by these NTD mechanisms, and their description in our compact models (Compact Model 1, CM1). All the new terms complement the accuracy advantage observed with existing CM1 resist modeling infrastructure. The new terms were tested on various NTD layers. The results demonstrate consistent model accuracy improvement for both calibration and verification. Furthermore, typical NTD model fitting challenges, such as large SRAF-induced wafer CD jump, can be overcome by the new NTD terms.

A comparison of through-pitch model errors between the traditional CM1 model form (Model A) and the new model form with NTD terms (Model B) is shown in Fig. 1. Systematic large negative model errors from the non-SRAF group are observed for Model A, indicating that the large SRAF-induced wafer CD jump was not fully captured by the traditional terms. This specific NTD effect was well accounted for with the new terms, as illustrated by the model error trend from Model B. Consistent results were obtained from the verification dataset measured on a different mask. As shown in Fig. 2, Model B exhibits smaller and randomly distributed model errors, whereas Model A gives different model error trends between SRAF and non-SRAF groups. With the new NTD terms, the through-pitch model error RMS is improved by 23% in calibration and by 33% in verification. The overall model performance for all gauges is characterized by the percentage of gauges that meet the model error specification, which increases by 3.6% and 4.4% for the calibration and verification dataset, respectively.

9426-60, Session PS5

Photoresist 3D profile related etch process simulation and its application of full chip etch compact modeling

Cheng-En R. Wu, Wayne Yang, Synopsys Taiwan Ltd. (Taiwan); Hua Song, Synopsys Inc. (United States)

The OPC model or post-OPC verification that takes the developed photoresist (PR) 3D profile into account is highly recommended in the advanced 2Xnm node and below. The process hotspots due to poor resist profile may not be fully inspected in the lithography process but will only be observed in the subsequent etch process. A complete OPC model flow for etch correction requires not only a resist 3D (R3D) profile model but also a model prediction for the final etch critical dimension (CD).

One important factor to affect the etch CD is the photoresist lateral erosion with finite etch rate during the etch process in the presence of non-vertical PR side wall angle (SWA) or anisotropy of etch plasma source. A simple example is in transferring from PR layer to hard mask (HM) layer, which is widely used in the advanced process. The PR lateral erosion contributes a HM etch CD bias which is deviated from patterned CD defined by PR.

The etch CD variation related to various SWA of PR is the main focus of this report. With a given geometry of PR, some etch process effects such as plasma ion reflection, neutral particle re-emission, and source anisotropy are taken into consideration in simulation. These are done with our TCAD tool Sentaurus Topography 3D using Monte Carlo simulation engine. As shown in figure 1, the etch CD bias is extracted from the simulated etch profile under

different etch conditions of ion reflection and anisotropy. The nonlinear behavior to the resist SWA indicates the complication of etch process.

A physically motived compact model for etch prediction is derived for the purpose of full chip application. We successfully deduce a compact formula that can apply to arbitrary SWA, ion reflection and anisotropy. The compact formula is tested under various input conditions and is found to be matched with Monte Carlo simulations very well. This opens opportunities in OPC etch correction or in etch hotspot detection in the production level.

9426-61, Session PS5

Resist profile modeling with compact resist model

Christian D. Zuniga, Yunfei Deng, Yuri Granik, Mentor Graphics Corp. (United States)

Resist profile shapes become important for 22nm node and beyond since a degraded shape may induce etching failures. Rigorous resist simulators can simulate a 3D resist profile accurately but they are not fast enough for correction or verification on a full chip. Compact resist models are fast but have traditionally modeled the resist profile at a single CD plane. However, they can be extended to simulate resist profiles by proper setting of optical parameters and by approximating the 3D acid diffusion with a lateral and vertical diffusion. Including height dependent modeling terms can further improve the accuracy. Large resist shrinkages in NTD resists can also be included in the compact model. This article shows how a compact resist model in Calibre can be used to simulate resist profiles as shown in Figure 1. The compact model can then be used to identify possible hotspots on a full chip and in some cases to correction of these patterns.

9426-62, Session PS5

Impacts of post OPC shapes on pattern

Wen-Han Chu, TSMC Taiwan (Taiwan)

As feature size getting smaller, it's crucial to gain depth of focus (DOF) common window in optical lithography. In addition to the DOF of individual patterns, one of the key elements that dominates DOF common window is the best-focus shifting between patterns. High order spatial frequencies, which could be diffracted from the sharp corner and small patterns on mask, induce additional phase term and could cause the best focus shift significantly. We analyzed the correlation between the pattern shape after OPC correction and its corresponding DOF and found that the more complicated shape leads to more focus shifting. The wafer experiment and simulation confirm the predictions. This provides another index for future OPC application.

9426-78, Session PS5

Calibrating etch model with SEM contours

Francois Weisbuch, GLOBALFOUNDRIES Dresden Module Two, GmbH & Co. KG (Germany); Ahmed S. Omran, GLOBALFOUNDRIES Dresden (Germany); Kenneth Jantzen, Mentor Graphics Corp. (United States)

State-of the art optical proximity correction (OPC) models can predict with high accuracy photoresist contours. This condition is necessary but not sufficient to ensure good patterning fidelity and high yields. A more effective method consists of taking into account the etch effects, usually measuring the bias between lithography and etch processes. The simplest approach is to use a global bias but it is often not selective enough and is replaced by rule based or even model based [1,2] corrections to predict the etch profiles. Rule based model is faster but also less accurate (see Fig.1) than model based etch correction. However it's challenging to get a well calibrated etch model because of its empirical nature and the necessity to measure complex 2D etched patterns. Moreover etch models are more difficult to implement in the OPC recipe and increase the overall OPC run time.

In this work, we will demonstrate that high quality variable etch bias (VEB) models can be calibrated quickly with SEM contours and used for applications in production. In particular, we want to stress the advantage of SEM contours over traditional CD when dealing with 2D measurements particularly relevant to characterize etch processes. In addition, the usage of contours dramatically increases the number of available calibration sites extracted within each SEM image. Our objective is also to highlight the importance of building post-OPC verification at both litho and etch levels to catch real issues on wafer. The implementation of etch model in the OPC flow is illustrated.

A 28nm node active layer was selected to generate various etch models calibrated at different steps in the patterning flow (see Fig.2). The different models are intended to give more latitude to define the measurements most relevant to the actual device geometry. We took benefit of experimental etch contours –also available after lithography- to analyze in detail quantitatively and qualitatively the biases of around 50 various structures (see Fig.3). The etch corrections predicted by a calibrated model are applied at the first step of the OPC flow to modify the drawn layer. Finally, post-OPC verification is performed at both resist and etch levels.

Quality of the contour-based etch model was assessed by analyzing along contours the Edge Placement Error (EPE) between simulated and experimental contours. The major contributors to EPE are especially interesting to identify the weaknesses of an etch model. Finally, the new model was used to highlight the limitations of available rule based bias table.

9426-63, Session PS6

7nm logic optical lithography with OPC-Lite

Michael C. Smayling, Tela Innovations, Inc. (United States); Koichiro Tsujita, Canon Inc. (Japan); Hidetami Yaegashi, Tokyo Electron Ltd. (Japan); Valery Axelrad, Sequoia Design Systems, Inc. (United States); Ryo Nakayama, Canon Inc. (Japan); Kenichi Oyama, Tokyo Electron AT Ltd. (Japan); Hiroyuki Ishii, Canon Inc. (Japan); Shohei Yamauchi, Tokyo Electron AT Ltd. (Japan); Koji Mikami, Canon Inc. (Japan)

The CMOS logic 22nm node was the last one done with single patterning. It used a highly regular layout style with Gridded Design Rules (GDR). Smaller nodes have required the same regular layout style but with multiple patterning for critical layers. A "line/cut" approach is being used to achieve good pattern fidelity and process margin.[1]

For the "cut" pattern, Design-Source-Mask Optimization (DSMO) has been demonstrated to be effective at the 20nm node and below.[2,3,4] Single patterning was found to be suitable down to 16nm, while double patterning extended optical lithography for cuts to the 10-12nm nodes. Design optimization avoided the need for triple patterning. Lines can be patterned with 193nm immersion with no complex OPC. The final line dimensions can be achieved by applying pitch division by two or four.[5]

In this study, we extend the scaling using simplified OPC to the 7nm node for critical FEOL and BEOL layers. The test block is a reasonably complex logic function with ~100k gates of combinatorial logic and flip-flops, scaled from previous experiments.

Simulation results show that for cuts at 7nm logic dimensions, the gate layer can be done with single patterning whose minimum pitch is 53nm, possibly some of the 1x metal layers can be done with double patterning whose minimum pitch is 53nm, and the contact layer will require triple patterning whose minimum pitch is 68nm. These pitches are less than the resolution limit of ArF NA=1.35 (72nm). However these patterns can be separated by a combination of innovative SMO for less than optical resolution limit and a process trick of hole repair technique. Fin and local interconnect are

created by lines and trims. The number of trim patterns are 3 times (min. pitch=90nm) and twice (min. pitch=120nm), respectively. The small number of masks, large pitches, and simple patterns of trims come from the simple 1D layout design.

Experimental demonstration of these cut layers using design optimization, OPC-Lite, and conventional illuminators at the 7nm node dimensions will be presented. Lines were patterned with 193nm immersion with no complex OPC. The final line dimensions (22nm pitch) were achieved with pitch division 4.[5]

1. Y. Borodovsky, "Lithography 2009: Overview of Opportunities," SemiCon West, 2009

2. M. Smayling, K. Tsujita, H. Yaegashi, V. Axelrad, R. Nakayama, K. Oyama, A. Hara "11nm Logic Lithography with OPC-Lite," Proc. SPIE Advanced Lithography 2014, San Jose, California.

3. M. Smayling, K. Tsujita, H. Yaegashi, V. Axelrad, T. Arai, K. Oyama, A. Hara "Sub-12nm Optical Lithography with 4x Pitch Division and SMO-Lite," Proc. SPIE Advanced Lithography 2013, San Jose, California.

4. M. Smayling, V. Axelrad, K. Tsujita, H. Yaegashi, R. Nakayama, K. Oyama, Y. Gyoda "Sub-20nm Logic Lithography Optimization with Simple OPC and Multiple Pitch Division," Proc. SPIE Advanced Lithography 2012, San Jose, California.

5. H. Yaegashi, K. Oyama, A. Hara, S. Natori, S. Yamauchi, M. Yamato, "Recent progress on Multiple-Patterning process," Proc. SPIE Advanced Lithography 2014, San Jose, California.

9426-64, Session PS6

OPC solution by implementing fast converging methodology

Ellyn Yang, Yaojun Du, Semiconductor Manufacturing International Corp. (China)

Traditionally, the optical proximity correction (OPC) is to deliver the solution to ensure the nominal after-development-inspection (ADI) contours on target. As the technology node keeps shrinking to 28nm and beyond, the OPC is expected to cover the lithography process window (PW), etch PW, and overlay margin as well. As a result, more and more advanced functions are included in OPC to achieve the awareness of multiple cost functions, such as the nominal EPE, PW effective EPE, the enclosure of above and underneath layers, and so on. These inclusions are at the cost of the run time and complexity of OPC solution. In this paper, we demonstrated a methodology by adopting design rule check (DRC) repair in accordance to nominal and PW optical rule check (ORC). The subsequent repair is applied to those PW hot spots only. With a straightforward recipe tuning, a fast convergence of OPC can be achieved. The results exhibit the run time improvement without compromising the OPC performance. We further discussed the possibility of substituting the DRC block by the PWOPC block within such a flow as proposed in this paper.

9426-65, Session PS6

The comparison of OPC repair performance with respect to various constraints

Yaojun Du, Qing Yang, Semiconductor Manufacturing International Corp. (China)

The optical proximity correction (OPC) designs a biased mask so as to ensure the after-development-inspection (ADI) contours on target. Meanwhile, the lithographic manufacture process is approaching the sub 28 nm technology node, imposing a tremendous challenge on OPC engineers. Even a well-tuned OPC recipe can render many off-target simulated contours for the most up-to-date chip designs; and these off-target contours indicate highly possible weak points on wafer. We have recently developed a high-performance repair flow that can automatically correct these OPC weak points based on the rule procedure. It is expected that one has to take both nominal and process window (PW) conditions into account to avoid potential weak points on wafer. For the contact holes, we require the nominal CD and PW CD to meet different criteria. In some cases, it could be difficult to satisfy both nominal and PW CD constraints which may pose conflicts to each other. In this work, various strategies have been used to accommodate such conflicts; for instance, one can release the nominal constraint or replace the PW CD constraint by the PW area constraint. We perform a systematic study on the various specifications of these constraints, in order to select the most optimal setup for the nominal and PW constraints. The several resulting masks will be put into wafer tests so that our optimized specifications can be verified experimentally. These optimized specifications may allow us to perform a highly efficient repair on a contact layer.

9426-66, Session PS6

Model-based HSF using by target point control function

Sungjin Kim, SK Hynix, Inc. (Korea, Republic of); Munhoe Do, Synopsys Korea Inc. (Korea, Republic of); Yongbae Ahn, Jaeseung Choi, Hyun-Jo Yang, DongGyu Yim, SK Hynix, Inc. (Korea, Republic of)

In this paper, we introduce a new HSF method that is able to make OPC TAT shorter than the common HSF method. The new HSF method consists of two concepts. The first one is that OPC target point is controlled to fix HSP. Here, the target point should be moved to optimum position at where the edge placement error (EPE) can be 0 at critical points. Many parameters such as a model accuracy or an OPC recipe become the cause of larger EPE. The second one includes controlling of model offset error through target point adjustment. Figure 1. shows the case EPE is not 0. It means that the simulation contour was not targeted well after OPC process. On the other hand, Figure 2. shows the target point is moved -2.5nm by using target point control function. As a result, simulation contour is matched to the original layout. This function can be powerfully adapted to OPC procedure of memory and logic devices.

9426-67, Session PS6

Sub-resolution assist feature (SRAF) printing prediction using logistic regression

Chin Boon Tan, Kar Kit Koh, GLOBALFOUNDRIES Singapore (Singapore); Dong Qing Zhang, GLOBALFOUNDRIES Inc. (United States); Yee Mei Foong, GLOBALFOUNDRIES Singapore (Singapore)

In optical proximity correction (OPC), the sub-resolution assist feature (SRAF) has been used to enhance the process window of main structures. However, the printing of SRAF on wafer is undesirable as this may adversely degrade the overall process yield. A reasonably accurate prediction model is needed during OPC to ensure that the SRAF placement and size have no risk of SRAF printing. Current common practice in OPC is either using the main OPC model or a threshold specifically tuned SRAF model to predict the SRAF printing. This paper studies the feasibility of SRAF printing prediction using logistic regression. Logistic regression is a probabilistic classification model that gives discrete binary outputs after receiving sufficient input variables. In the application of SRAF printing prediction, the binary outputs can be treated as 1 for SRAF-Printing and 0 for No-SRAF-Printing. The input variables can be obtained from the process conditions and SRAF intensity profile. In this work, the optimization algorithms are coded in OCTAVE programming language. The results cover SRAF printing prediction on via and metal layers with both positive tone development (PTD) and negative tone development (NTD) resist processes. The metal layer focuses on 1D SRAF whereas the via layer focuses on 2D SRAF.

9426-68, Session PS6

Accurate and fast computation of transmission cross coefficients

Stefan Apostol, IBM Research (Switzerland); Paul Hurley, IBM Research – Zürich (Switzerland); Radu C. Ionescu, EPFL (Switzerland) and IBM Research – Zürich (Switzerland)

Precise and fast computation of aerial images are essential. Typical lithographic simulators employ a Kohler illumination system for which aerial imagery is obtained using a large number of Transmission Cross Coefficients (TCCs). These are generally computed by a slow numerical evaluation of a double integral. We review the general framework in which the 2D imagery is solved and then propose a fast and accurate method to obtain the TCCs. We acquire analytical solutions and thus avoid the complexity-accuracy trade-off encountered with numerical integration. Compared to other analytical integration methods, the one presented is faster, more general and more tractable.

9426-69, Session PS6

Model-driven optimization of rule-based OPC fragmentation

Jingyu Wang, GLOBALFOUNDRIES Inc. (United States); Alexander Wei, Mentor Graphics Corp. (United States); Piyush Verma, William Wilkinson, GLOBALFOUNDRIES Inc. (United States)

The concept of model-based fragmentation was first introduced to ensure sufficiently dense sampling by the existing sparse-OPC engine. It aimed at keeping critical sites and avoiding overlooking convergence issues. When image-based intensity computation became the dominant OPC engine at the 32 nm tech node, the expectation for model-based fragmentation changed, as the primary technical concern was no longer an omission of simulation sites. Instead, major effort was devoted to correctly placing the fragmentation points by referencing the aerial image curvature, so that the frequency passed through the optical system is precisely compensated to minimize edge placement errors (EPE). However this goal was never well achieved, as by principal, a local 2D signal analysis does not lead to a global optimum. That is, while set steps of localized shift, addition, or removal of segment points can potentially solve weak points; they lack the power of overturning destructive optical settings. To provide insights into best practices and efficiently organize simulation resources, we propose a method of classifying rule-based fragmentation with respect to model-based aerial image. Specifically, by conducting a coarse simulation with default engine settings, we extract the rippling signal associated with signature geometries along all dimensions, which is predominantly physical hence a good representation of the unfiltered optical signal. By taking into account both the computed Nyquist frequency and the experimental rippling frequency, and fully respecting geometrical boundary conditions we derive a global solution for fragmentation. The methodology enables us retain the control over a robust recipe that is physically capable of achieving good EPE without compromising run-time.

9426-70, Session PS6

The study of lithography conditions to use advanced resist performance properly

Zhengkai Yang, Wuping Wang, Quan Chen, Shanghai Huali Microelectronics Corp. (China); Hajime Aoyama, Kengo Takemasa, Toshihiko Sei, Tami Miyazawa, Tomoyuki Matsuyama, Nikon Corp. (Japan); Chun Shao, Nikon Precision Shanghai Co., Ltd. (China)

ArF immersion lithography is the current primary technology widely applied to critical layers. At current imaging nodes, it is used even for dimensions less than the optical resolution limit by employing multiple patterning technology. At such a level, due to the to very low-k1 condition exposure conditions and tight CD variation requirements, imaging margin against various errors, such as defocus, dose error, and mask CD error is very small. This is confirmed based on rigorous optical simulations. Additionally, in the real world, we need to take into account process effects such as resist response degrading optical intensity distributions. Conventionally, the resist response is treated as additional uncertainty, which may amplify effect of the errors in lithography. Therefore, the resist image performance is always lower than expectation obtained by optical simulations.

Recently, we have found a case where this is not true. The most advanced resist group sometimes show better behavior than expectation based on optical simulation in dose latitude, MEEF (mask error enhancement factor), and even CD variation thru different spatial pitch as shown in Figure 1. This superior resist performance may allow greater margin for error in each component, such as mask, scanner, metrology in very low-k1 lithography.

On the other hand, since the resist pattern CD for the most advanced resist is very much different from the one based on optical simulation, it is a challenge to build OPC models using the exposure result with the resist. In order to solve this issue, we have tried to use several litho parameters to reduce the gap between optical simulation and resist CDs for OPC modeling. In this paper we discuss the effect of the parameters to reduce the gap between optical model and actual resist behavior with keeping superior performance as much as possible. The method we mention may be a key to use the most advanced resist in near future. As a result the life of ArF immersion lithography in the critical layer would be extended than we expect today.

9426-71, Session PS6

Local printability enhancement technique for hotspot fixer for sub-14nm nodes

SukYoon Chung, Hyejin Shin, Sejin V. Park, No-Young Chung, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Soung-Su Woo, Sergey Kobelkov, Kyohei Sakajiri, Mentor Graphics Corp. (United States); Jiwan Han, Mentor Graphics Corp. (Korea, Republic of); Sukjoo Lee, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Alexander Tritchkov, Mentor Graphics Corp. (United States); Byoung-il Choi, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

Various resolution enhancement techniques (RET) have been developed. Nonetheless, as technology node needs to be reduced to sub-14 nanometer, lithography hotspots associated with challengeable design rules still remain. In particular, it is necessary to improve process window (PW) of the hotspots as well as optimize every pixel on the mask for maximum PW by taking into account both main target and SRAF. To achieve this goal, inverse lithography technology (ILT) has been proposed as an ideal solution. However, due to long OPC Turn-around time (TAT), it takes a huge amount of time to finish full chip OPC operation.

To solve such an operating time issue, local printability enhancement (LPE) has been developed. In general, LPE is a posterior process in the sense that it inspects a particular area which has been already found to be out of process window (PW). Such an inspection is performed by referring to ORC error results and OPC outcome previously obtained.

For instance, ILT redoes a layout correction by means of OPC repair tool and identifies unfound hotspots or new ones by applying strict ORC rules, after which LPE begins to minimize fixing area. To do so, LPE creates three regions around hot spots, that is to say, core, context and visible region. LPE also iterates updating the repair regions, which leads to maximizing a repair rate. In the end, when the layout fulfills requirements, LPE integrates the three repaired regions together with the main OPC results. In doing so, we assure that pattern on the boundary of the repair regions passed ORC test without error.

In this paper, we introduce a full chip-based hotspot fixing flow relevant to LPE with pixel based OPC. By doing so, we maximize a lithography PW while OPC TAT increase is negligible compared to the runtime required for ILT simulation of full chip or the rerun of modified conventional OPC.

9426-72, Session PS7

Modeling and simulation of beam steering unit

Jiayun Feng, Xiaoping Li, Xin He, Jinchun Wang, Huazhong Univ. of Science and Technology (China)

With the development of lithography system, the production lithography cell is undergo a technology shift, and the requirements of beam delivery system (BDS) are increasing which also raises the precision requirements of the beam steering unit(BSU) in BDS. In essence, the BSU is a two rotational degrees of freedom stage used to adjust the beam direction to meet the pointing and location requirements. In the BSU, the rotational angle is ±2 milliradian and the precision requirement is less than 2 microradian. Because of the characteristics such as less driving elements, compact structure and high precision, 3-RPS flexure parallel mechanism is adopted here.

In this paper, a BSU based on 3-RPS flexure parallel mechanism is proposed. By replacing the traditional hinges with flexure hinges, the mechanism relies on the deformation of flexure hinges to transmit motion and force. In recent years, a lot of work has been done studying its kinematics, but research about the stress of BSU while the end-effector is moving is few, and even fewer is the people who present an exact method to determine the optimal parameters of BSU. Here, the stress during the moving stage and the design method which will get an optimal design will be discussed in detail.

As shown in Fig. 1(a), the BSU is composed of three branch chains, a moving platform and a fixed platform. The system can be simplified to a pseudo-rigid-body model (PRBM) by replacing flexure hinges with traditional hinges (as shown in Fig. 1(b)). Based on the transformation matrix and mechanical characteristics of the PRBM, the dimension model of the system, such as the motion displacement of each branch chain, the coordinates of flexure hinges, and rotational angle of each flexure hinge, can be obtained. By analyzing the mechanical properties of the moving platform and the branch chains respectively, the mechanical model of the system can be obtained. There are 12 equations and 14 unknown parameters (including forces and stiffness of flexure hinges), and forces can be expressed by k1 (stiffness of the spherical flexure hinge) and k2 (stiffness of the single-axis flexure hinge) through solving the equations. Based on the characteristics of the system, the relationship of k1 and k2, and the scope of k1 and k2 can be obtained. According to the calculation formula of flexure hinge stiffness, the relationship between flexure hinge stiffness and b (the value of flexure hinge width), r (the value of flexure hinge radius), and t (the value of flexure hinge thickness) can be got. Then the parameters can be optimized to get a BSU with less stress of the flexure hinges in different position. After optimization, it is verified whether the stress of flexure hinges meets the strength requirements through simulation. The stress analysis can be divided into two steps: static stress analysis and dynamic stress analysis (as shown in Fig. 2).

The simulation result shows that the design parameters are reasonable, and the design method of BSU is correct and effective.

9426-73, Session PS7

DUV ArF light-source automated gas optimization for enhanced repeatability and availability

Tanuj Aggarwal, Kevin O'Brien, Cymer LLC (United States)

The need for repeatable, reliable, and shorter DUV ArF light source gas optimizations drove the development of Automated Gas Optimization (AGO) and the bandwidth control technology (ETC) counterpart AGO+. These automate the manual gas optimization procedure previously used to select the laser chamber gas pressures and in addition, bandwidth actuation settings, to deliver consistent performance and long gas lives, while maintaining stability and bounds on laser inputs. Manual gas optimization procedure requires at least two refills and an on-site visit by a service personnel that can take over an hour to complete. Furthermore, it is susceptible to variations due to biases introduced by individual personnel in conjunction with chipmaker scheduling vagaries and time pressures. This results in inconsistent light source performance, and sometimes unscheduled downtime.

The key to AGO/AGO+'s technology is the real-time estimation and monitoring of the laser's gas and bandwidth states, and automatic adjustment of gas pressure and bandwidth actuators until the states reach their specified targets, thus creating a closed loop. AGO and AGO+ execute on every refill, typically complete in less than 5 minutes, and collect performance data to allow long-term trending. They include built-in safety features and flexibility to allow future upgrades of light source features or performance tuning. Deployed in many lasers in the field, AGO has proved to be a dependable automation, yielding repeatable, fast, and reliable optimizations and valuable long-term trending data used to assess chamber performance.

9426-74, Session PS7

Performance of ETC controller in high-volume production

Joshua J. Thornes, Kevin O'Brien, Will Conley, Hoang Dao, David Dunlap, Ronnie P. Flores, Matt Lake, Tanuj Aggarwal, Aleks Simic, Brian Wehrung, John Wyman, Cymer LLC (United States)

As chipmakers continue to reduce feature sizes and shrink CDs on the wafer to meet customer needs, Cymer continues developing light sources that enable advanced lithography, and introducing innovations to improve productivity, wafer yield, and cost of ownership. In particular, the ETC controller provides improved spectral bandwidth and wavelength stability, which enables superior CD control and wafer yield for the chipmaker. The XLR 660ix is Cymer's flagship argon fluoride (ArF) light source, and the first to provide flexible power output to meet ever-increasing productivity demands, particularly for double patterning applications. It has the unique capability to operate in a range from 60W for typical immersion applications, to 90W for higher dose or higher throughput applications.

Last year we reported that the XLR 660ix incorporates new controller technology called ETC for improvements in spectral bandwidth and wavelength stability. The ETC controller provides improved spectral bandwidth and wavelength stability, which enables superior CD control and wafer yield for the chipmaker. The Authors will present the data for the ETC platform that has become the volume light source supporting ASML NXT:1970C systems. The Authors will present metrics demonstrating the stability of the many systems that have been produced over the past year.

9426-75, Session PS7

Reduction of helium usage in the XLA and XLR platforms

Gamaralalage G. Padmabandu, Erich R. Gross, Don Haran, Eric Mason, Richard Ujazdowski, Matt Lake, Cymer LLC (United States)

Helium is one of the most abundant elements in the universe but commercial supply is becoming increasingly difficult to obtain and costly. Because the gas is inert and has a very high melting and boiling points many industries use helium including cryogenics, high-energy accelerators, arc welding, the medical industry and semiconductor wafer manufacturing.

Helium is used as a purge gas for some components within the light source. It's ideal due to the low index of refraction and thermal management properties. Our focus is the reduction of helium usage without negatively

affecting the performance of the Light Source. The authors will present data demonstrating the performance of the Light Source with reduced helium usage along with strategies to further reduce the impact that the Light source has on the overall consumption of helium in a semiconductor fab.

9426-76, Session PS7

New robust and highly customizable light source management system

Yuji Minegishi, Kenji Takahisa, Tatsuo Enami, Hitomi Fukuda, Young Sun Yoo, Hideyuki Ochiai, Takeshi Ohta, Gigaphoton Inc. (Japan)

Fueled by the "mobile" consumers, with their smartphones, tablets and now IoT, the demand for smaller, cheaper, faster, and more energy efficient chips continue to grow stronger every year. The competitive environment for chipmakers is also growing fiercer. Differentiation can no longer be achieved through design technology alone. Cost has now become just as important a differentiator — if not more important — for chipmakers.

In the lithography space, the light source plays a significant role in the wafer production process as well as the manufacturing cost per wafer. Software tools that offer the ability to effectively monitor the performance and health of light sources to anticipate and plan for maintenance and downtimes have been invaluable for managing operational cost. However, chip manufacturers going forward will be challenged to develop new and innovating ways to become more cost effective than their competitors, and the software tools necessary to compete in this environment must be capable of effectively adapting to the unique needs of each manufacturer.

REDeeM CloudTM is a new software system developed by Gigaphoton for managing light source performance and operation. It offers a simple and intuitive user interface that can be operated using a standard web browser on any PC, or on most of today's popular mobile devices such a tablets and smartphones.

There are two distinct components to the REDeeM CloudTM system: the Web UI and the Data Server. The Web UI is the system's front-end user interface for managing a single or a fleet of light sources. The Data Server is responsible for collecting, storing, and analyzing data from the light source, and also provides a server-side Web API service for searching and retrieving data over the local network. Each component runs independently as small, standalone web servers and can be installed on virtually any PC running the latest Windows, Mac OS or Linux operating systems.

REDeeM CloudTM is developed entirely using today's popular open source web technologies such as HTML5, CSS, PHP, and JavaScript. The Web UI may be used as-is or it can simply serve as a template for develop a fully customized user interface. Standard features offered on the Web UI include: light source utilization statistics, parts health status, lifetime forecasting, plot analysis, long-term trending, error analysis, wafer/burst level beam analysis, and user account management. Responsive design methods are implemented so the user interface will automatically adjust its content to fit the screen size ad dimensions of browser being used to access it.

The Web API's role is primarily to provide the necessary information to the Web UI pertaining the laser, but it can also be used by itself as a simple network data server. This is especially useful for users that develop their own software for managing tools and want to integrate laser management into their system. The Web API is designed based on a Representational State Transfer (REST) API architecture, which is widely used by many web sites today that allow their services to be integrated into third party web sites and applications.

9426-77, Session PS7

Extending green technology innovations to enable greener fabs

Kenji Takahisa, Yuji Minegishi, Tatsuo Enami, Hitomi Fukuda, Young Sun Yoo, Gigaphoton Inc. (Japan)

In the semiconductor manufacturing industry, there are growing concerns over future environmental impact as enormous fabs expand and new generations of equipment become larger and more powerful. Especially rare gases supply and price are one of prime concerns for operation of HVM (high volume manufacturing) fabs. Over the past year it has come to our attention that Helium and Neon gas supplies could be unstable and become a threat to HVM fabs.

To address these concerns, Gigaphoton has implemented various green initiatives for many years under its EcoPhoton program and been trying to promote our views on the importance of Green concepts, and the opportunities and benefits we see for the industry.

One of the initiatives is the GigaTwin deep ultraviolet (DUV) lithography laser platform based on injection-lock technology. It is the design choice based on two essential needs for high volume manufacturing fabs: efficiency and stability. GigaTwin lasers require only half the resources such as electricity or gas compared to lasers on different design. Together with other technical advances, injection-lock technology enables our laser systems to be technically and ecologically viable for HVM.

Injection locking is a newer approach to a twin-chamber laser system and offers some advantages over master oscillator power amplifier (MOPA) systems used in other lithography equipment. In a traditional MOPA system, the master oscillator laser chamber generates a narrow spectrum seed light through an optical resonator consisting of a line-narrowing module (LNM) and a mirror. This light is then fed into the power-amplifier chamber, where the power is amplified through a single-pass or double-pass amplification process. In the GigaTwin injection-lock technology platform, the narrow-spectrum seed light is generated by the master oscillator using the same process and technology as the MOPA systems. However injection-lock systems use a regenerative resonator with a pair of optical mirrors for power amplification chamber. The seed beam is regenerated by the round trip during the excitation lifetime of the dimer used (approximately 20 ns), which is equivalent to six-pass amplification. This is how the injection-lock system yields higher output energy efficiency compared to around two passes in traditional MOPA systems.

A further benefit gained by this efficiency is gas usage reduction. When less electricity is used, the gas deterioration rate is correspondingly smaller; therefore, applying injection-lock technology enables a 50% reduction in gas consumption along with electricity usage.

Last year we have developed two technologies to further reduce electricity and gas efficiency.

The electricity reduction technology is called eGRYCOS, and it reduces electricity by 15% without compromising any of laser performances. eGRYCOS system has a sophisticated gas flow design so that we can reduce cross-flow-fan rotation speed.

Also, newly optimized pre-ionization that generates uniform distribution of ions prior to main discharges, can improve radiation efficiency by 20%.

The gas reduction technology is called eTGM (enhanced Total gas Manager) and it is an improvement on gas management system optimizing the gas injection and exhaust amount based on laser performance, resulting in 50% gas savings.

9426-81, Session PS7

A complete compact mask 3D model in extreme ultraviolet lithography with high-efficiency and accuracy

Hongbo Zhang, Qiliang Yan, Xin Zhou, Sajan Marokkey, Ebo H. Croffie, Synopsys, Inc. (United States)

As the recent great improvement on EUV process throughput, it becomes urgent to have EUV-related model ready in EDA simulation tools to meet the requirement on the EUV production. Among the demanding topics, EUV-related mask topography effect is one of the most significant ones. Because of the tight CD in the targeted process, complex capping and multi-layer structure and inevitable mask incident angle, EUV lithography introduces many challenging new phenomena to compact full chip modeling. These include mask defocus, pattern shift variation through slit and through focus,

pattern dependent best focus variation, telecentricity errors, pitch- and slit- dependent H-V bias, mask reflectivity variation through incident angle, etc. Rigorous simulation can provide a reliable prediction on EUV mask topography effects within a small region for process study, but it is too slow for full-chip applications.

In the most commonly seen compact model for EUV lithography, part of the mask topography effects, or the shadowing effects, is handled by a geometry based mask bias. However, this simple shadowing model can only capture a small portion of the complex mask topography effects seen in EUV lithography, namely the H-V bias and its variation through slit, but fails to predict many other important effects. It works only for relatively large features, which misses the point of using EUV system. Also, the calibration on the geometric shadowing effect is arbitrary, highly relying on the test patterns, fitting cost functions, source and the calibration reference. Such calibrated model might be suffering from overfitting and has little tolerance on any changes/variations in the calibration process.

In this paper, a novel Mask3D for EUV compact model is proposed. The contribution of this novel model can be summarized as follows:

- This is the first ever EUV compact Mask3D model that unifies the mask topography behavior together with shadowing effect under the scope of off-axis illumination.

- The model in this paper is the first compact Mask3D model for EUV that does not requires intensive fitting on test pattern, EUV source and mask structure. In fact, the model accuracy is both test pattern- and source-independent.

- The model can accurately predict all the aforementioned challenging mask topography in an integrated modeling flow.

- Because of the above properties, the proposed Mask3D model can support all-angle mask and ILT technique without compromising the runtime speed and accuracy.

Multiple tests of the new model have demonstrates the consistent perform throughout a broad process window. For a large amount of regular pitch structures from 30 nm to 160 nm with CD from 15 nm to 40 nm, the CD RMS can be as low as 0.25 nm. More importantly, to achieve such high accuracy does not require special calibration on specific mask type, test pattern and EUV setup. Changes in the source and layout do not require recalibration of Mask3D. The obviation of repeated Mask3D-specific calibration effort promises significant reduction on engineer time/cost in fabs and huge improvement on ease-of-use, reliability and predictability for various source and layer patterns.

9426-35, Session 9

Layout optimization for the upcoming 10nm and 7nm printability scenarios *(Invited Paper)*

Andrzej J. Strojwas, Carnegie Mellon Univ. (United States) and PDF Solutions, Inc. (United States)

Process variability is creating daunting challenges for achieving predictable process and product times-to-market with economically acceptable yield levels. Aggressive scaling has increased the layout dependent systematic variability primarily due to resolution limitations and the application of stressors in modern device architectures. Complex DFM flows have been proposed to model such layout dependent effects. However, the lack of accuracy with these modeling attempts has marred their adoption. We can show, however, that there is hope for minimizing these systematic variations with a pro-active DFM approach that requires design and process to be developed based on a set of pre-characterized circuit elements.

It is important to note that if left unchecked, these systematic variations will have a prohibitive impact on 10nm and below designs. In particular, the continuing delays in EUVL set the need to define 10nm technology node using expensive triple patterning technologies. We propose a design methodology to overcome these challenges, thus taking the next step in Moore's law with the application of smarter and more efficient layout and lithography co-design techniques that can provide high density and increased yields at a sustainable cost. The key enabler of this methodology is the creation of a regular design fabric onto which one can efficiently map the selected circuit elements using a limited number of printability-friendly layout patterns called templates. The co-optimization of layout and process is achieved by co-developing layout pattern library and lithography solutions. Manufacturability robustness of this set of layout templates can be then rigorously characterized via the specially designed test structures in small silicon area.

We will demonstrate that this methodology will enable future technology nodes that utilize current generation lithography while minimizing the cost per good die. In particular, we will discuss the choice of regular design fabrics and their implications on design metrics, yields and cost; and show that the selection of circuit topologies can be mapped efficiently to the choice of regular design fabric, and compare lithography solutions such as multiple patterning, directed self-assembly (DSA) and the direct write multi-e-beam (MEBM) for the 10nm technology node and beyond.

To enable designs with a limited number of layout patterns without compromising the design density, we must rely on techniques that co-optimize layout styles (e.g., 1-directional vs. 2-directional M1 routing in standard cells) and lithography solutions. We will demonstrate this design-technology co-optimization methodology for the 10nm FinFET node and show that the improved manufacturability due to huge reduction of layout patterns can be achieved without any penalty in the power/performance/area (PPA). We will demonstrate drastic pattern count reduction for the standard cells and IP cores versus the standard restricted design rule designs. We will also present an entire eco system for the template development, verification and implementation in commercial design environments.

9426-36, Session 9

Hot spots prediction after etching process based on defect rate

Taiki Kimura, Yuki Watanabe, Toshiya Kotani, Toshiba Corp. (Japan)

Hot spots caused by etching process were accurately found on the proposed full-chip lithography simulation. The simulation correlates a peak intensity of optical image at a specified resist height with defect rates after etching process obtained by a wafer inspection tool. As minimum feature sizes have been shrinking, a resist cross-sectional profile becomes worse due to resolution enhancement techniques such as a highly coherent illumination. The bad resist profile may cause a hot spot after etching process so that a fast and accurate method to find the hot spot is crucial and anticipated to fix the hot spot at a design stage. Conventional methods mainly focus on a resist cross-sectional profile. However, the methods cannot accurately find hot spots caused by etching process because it is difficult to guarantee accuracy of the resist cross-sectional profile for variety of patterns and a resist profile does not accurately decide hot spot occurrence.

In this paper, we propose a new method to find hot spots after etching process. The proposed method consists of three steps. Firstly defect rate on several patterns is obtained based on hot spots after etching process obtained by a wafer inspection tool. Secondly, peak intensity of optical image at a specified resist height is calibrated to the defect rates. Thirdly, the peak intensity where defect rate is zero, shown by arrow in Fig.1, is determined as specification value for lithography simulation to find hot spots caused by etching process. In our presentation, we will show the proposed method is experimentally confirmed.

9426-37, Session 9

Hybrid OPC flow with pattern search and replacement

Piyush Verma, Shikha Somani, Yang Y. Ping, Piyush Pathak, Rani S. Ghaida, Carl P. Babcock, Fadi Batarseh, Jingyu Wang, Sriram Madhavan, Sarah McGowan,

GLOBALFOUNDRIES Inc. (United States)

Optical Proximity Correction is a mandatory step in the mask manufacturing flow for sub-wavelength lithography. In a typical Optical Proximity Correction step at these nodes, optical and resist models are used to modify the drawn layer such that the layout features can be accurately reproduced by the lithography process onto the wafer. A traditional model based OPC mask generation tool involves iteratively modifying the drawn shapes based on a cost function computed from the edge placement error. Due to the complexity of the models and the iterative nature of the correction, model based OPC often generates slightly different mask shapes for identical geometric patterns. This is especially true for some advanced RET tools like model based SRAF and inverse lithography flows. Inconsistency in model based SRAF generation for SRAM arrays is a major issue and continues to be one of the biggest impediments to its deployment in full scale production flows. Performing iterative correction on every instance of a repeated pattern in the VLSI design not only increases mask inconsistency, the mask generation runtime also goes up, making model based OPC a very expensive computational operation.

Previously, we have demonstrated a hybrid OPC flow that involves a pattern replacement step followed by model based OPC [1]. This paper extends the work in [1] on pattern-replacement based OPC to include pattern-based SRAF generation. We build a library of frequently occurring patterns in a VLSI design to build a pattern library. To this library, we also add the corresponding mask shapes obtained by performing rigorous model based OPC (including SRAF generation) on the drawn patterns. We then use this pattern library in the mask data preparation flow to apply pattern replacement to generate a partial mask solution for the design. Since, pattern replacement does not require any complex optical/resist model computation; it is a very fast step. Subsequently, model based OPC is performed only on regions that do not get a mask shape from pattern replacement step. Since, only a fraction of the entire design area needs to be simulated in the model based OPC step, significant runtime savings can be obtained. We further use the hybrid pattern replacement and model based OPC flow and demonstrate its capability to significantly improve the consistency of mask correction as applied to main features that occur as large chunks of repeated geometric patterns. By including the model based SRAF shapes in the pattern replacement library, we improve the SRAF consistency in designs with repetitive patterns, creating mask shapes with much better manufacturability, uniformity and process window.

References

1. Piyush Verma, Fadi Batarseh, Shikha Somani, Jingyu Wang, Sarah McGowan and Sriram Madhavan, “Pattern-based pre-OPC operation to improve model-based OPC runtime”, SPIE Photomask Technology (September 2014)

9426-38, Session 10

Overlay improvement methods with DBO and IM

YoungSun Nam, Jang-Sun Kim, Ju Hee Shin, Young-Sin Choi, Sang Ho Yun, Young-Hoon Kim, Si Woo Shin, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Jeong-Heung Kong, Samsung Electro-Mechanics (Korea, Republic of); Young Seog Kang, Hunhwan Ha, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

To accord with new requirement of securing more overlay margin, not only optical overlay measurement is faced with the technical limitations to represent the cell pattern’s behavior, but also larger measurement samples are inevitable for minimizing the statistical error and better estimation of circumstance in a lot.

Even though various approaches to break the current technical barrier are being implemented in this field, this paper is mainly going to propose the In-line metrology system in combination with the DBO (Diffraction Based Overlay), a new overlay measurement method using diffracted lights from the grating.

The DBO has already been introduced by many papers as an alternative solution of the IBO (Image Based Overlay)’s optical resolution drawback but we have mostly concentrated on the accuracy performance because the metrology KPIs like TMU (Total Measurement Uncertainty), MAM (Move Acquire Measure) and TIS (Tool Induced Shift) 3sig were on the similar level with IBO since the IBO technology has been also improved as well.

As the size of DBO target has been reduced enough, we applied them to our 2x nm node device with the optimized pitches showing the highest SS (Stack Sensitivity), lowest TC (Target Coefficient) and also appropriate aberration sensitivity as comparing with Cell pattern within our specific limitations. The result showed the preferable accuracy than IBO and other KPIs were on the similar level as we expected. It also opened the possibility not to have unconfirmed overlay error which cannot be fully reflected by the current metrology target we are using.

With the benefits of DBO, the In-line metrology system is also being evaluated as a part of supplementing the current insufficient samples without in-line cluster interruption. Now we are struggling to estimate the circumstance in a lot to have better correction potential against the overlay variations and abnormal overlay jumps. Even if many statistical modeling techniques are competitively being introduced to overcome the current insufficiency of samples, more powerful and practical data are definitely needed to maximize the estimation performance.

From our evaluation results, we were able to use these additional overlay data to support our current APC system as we could enhance the estimation level, but we were also experienced many technical and operational difficulties on harmony with the existing facilities.

In conclusion, the In-line metrology in combination with DBO has the strong potential to meet the current and next generation overlay requirements.

9426-39, Session 10

Intra-field overlay correction for illumination based distortion

Michael B. Pike, Timothy A. Brunner, Timothy J. Wiltshire, Bradley Morgenfeld, Nick Jing, IBM Corp. (United States)

The use of extreme freeform Illumination conditions and multi patterning processes used to generate sub 40nm images can result in significant intra-field overlay errors. When levels with differing illumination conditions are aligned to each other, these intra-field distortions can result in overlay errors which are uncorrectable using normal linear feed back corrections.

We describe a double exposure method which we use to isolate and measure intra-field overlay distortions caused by individual tool lens signatures and or illumination conditions. A full field test reticle is used to create a dual level expose pattern. The same pattern is exposed twice, but with 2 different illumination conditions. The first exposure is done with a chosen reference Illumination. The second exposure is the desired test illumination condition. A high density, 13x13, intra-field overlay measurement is collected and then modeled to determine additional 2nd and 3rd order intra-field terms. The resulting Illumination and scanner lens specific intra field subrecipe is independent of field size. The subrecipe can then be applied to any product exposure which uses the same illumination conditions as the test exposure. When the method is applied to all exposure levels in a product build cycle, the overlay errors associated with the reference illumination condition cancel out. The remaining errors are due exclusively to individual lens aberrations and tool scan errors.

Actual results correlated well with the model with more than 80% of the predicted overlay improvement being achieved.

Acknowledgement: This work was performed by the Research and Development Alliance Teams at various IBM Research and Development Facilities

9426-40, Session 10

Wafer to wafer overlay control algorithm implementation based on statistics

ByeongSoo Lee, Young Seog Kang, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Jeong-Heung Kong, Samsung Electro-Mechanics (Korea, Republic of); Hyunwoo Hwang, Myeong Gyu Song, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

To produce DRAM device in mass production line stable and effective overlay control become more and more important and critical as DRAM design rule is shrank. To make matters worse overlay margin decrease ratio is faster than that of device. To overcome this situation already many technology were applied like HOWA(High Order Wafer Alignment), HOC(High Order Correction), CPE(Correction Per Shot)etc.Nevertheless still we are suffered from tight overlay margin and forced to move wafer level overlay control stage. However wafer level control requires huge amount of measurement resource.

This paper was written to present the insight for the wafer level overlay correction and control using optimal measurement resource which can afford in mass production line. The experiment was fulfilled on D2X node DRAM and statistical method was used to design experiment and to verify results. Based on statistical method like regression or frequency analysis with certain criteria we could find more effective parameters which can be used for wafer level control. After parameters selection we used regression again to find k value trend among the wafers. As a result we could find out some tendency and also risky point together. Analysis for reducing risk is still going on. After finish this step we will test several ways of wafer level control algorithms and will present comparison table.

9426-41, Session 11

Computational approaches to DSA-assisted lithography applications

Tim Fühner, Fraunhofer-Institut für Integrierte Systeme und Bauelementetechnologie IISB (Germany); Ulrich Welling, Georg-August-Univ. Göttingen (Germany); Przemyslaw Michalak, Fraunhofer IISB (Germany); Juan Carlos Orozco Rey, Weihua Li, Marcus Müller, Georg-August-Univ. Göttingen (Germany); Andreas Erdmann, Fraunhofer-Institut für Integrierte Systeme und Bauelementetechnologie IISB (Germany)

We present extensions to our previous effort to rigorously model the directed self-assembly (DSA) of block co-polymers (BCP) to pattern contact holes. Like before, we aim at describing the joint lithography/grapho-epitactic DSA co-process in its entirety to facilitate the study of the mutual impact of process parameters. In addition to further investigations on contact shrink applications, we have extended our approach to other contact rectification problems. For example, we have examined a configuration consist-ing of two adjacent contact holes that cannot be resolved lithographically (using a 193-nm immersion projection system with a single exposure). As an alternative, a larger guiding pattern exhibiting a shape often referred to as “eggs box,” comprised of intersecting circles is generated through lithography. The subsequent DSA rectification consists of the following steps: (1) establishing a preference of the walls for one of the BCP phases, (2) deposition of the block co-polymer, (3) annealing and (4) etching out of the inner cylinder formed by one of the BCP phases. If successfully applied, two distinct con-tact holes meeting the intended sizes are obtained. In this study, the impact of the guid-ing structure on the DSA process and the final pattern are evaluated. For that purpose, lithographic process variations are considered. In addition to the common focus/exposure matrix (FEM), the influence of projector aberrations on CD, placement and on the morphology of the final pattern is examined and statistically quantified. In a second step, contact hole roughness (CHR) and placement errors (PE) caused by the DSA process are investigated. One reason for flaws in DSA-assisted lithography is the thermal fluctuations of the copolymer interface and the glass transition, which ultimately deter-mines the position of the inner cylinder within the complementary BCP phase. Fluctuations can be distinguished into high-frequency interface oscillations or long-range modulations of the shape and the position of the inner cylinder. Specifically, the long-range fluctuations can be considered harmful as they deteriorate the pattern transfer, which is accomplished through etch. We have studied the probability of such fluctuations in dependence of the morphology and the surface potentials of the confinement and discuss means to suppress associated deficiencies. As a numerical model for the aforementioned simulations, a particle-based coarse-grained model—embedded in a single-chain mean-field (SCMF) scheme—is applied. Such a model is well suited for this kind of investigations in that it is adequately exact while maintaining a feasible runtime. In contexts, however, in which computation time is of primary concern, such as optical proximity correction (OPC) or source/mask optimization (SMO), the use of faster, reduced models is inevitable. To this end, we have employed two alternative approaches to the contact hole rectification problem: (1) a continuum model based on the Ohta-Kawasaki and the Swift-Hohenberg formulations and (2) a geometric technique using interface Hamiltonians, which is derived from the strong segregation limit (SSL) of copolymers. Their validity constraints and their scope of application for DSA-assisted lithography are discussed by reference to the obtained simulation results.

9426-42, Session 12

Latest performance of ArF immersion scanner NSR-S630D for high-volume manufacturing for 7nm node

Takayuki Funatsu, Yusaku Uehara, Yujiro Hikida, Akira Hayakawa, Satoshi Ishiyama, Hirotaka Kono, Katsushi Nakano, Yosuke Shirata, Yuichi Shibazaki, Nikon Corp. (Japan)

In order to achieve stable operation in cutting-edge semiconductor manufacturing, Nikon has developed NSR-S630D with extremely accurate overlay while maintaining throughput in various conditions resembling to real production?conditions. In addition, NSR-S630D has been equipped with enhanced capabilities to maintain long-term overlay stability and usability improvement all due to our newly developed application software platform.

The semiconductor technology roadmap suggests that continuous improvement of on-product accuracy and yield will be required for the 7nm node, in which multiple patterning techniques are used. Furthermore, many customers such as MPU, memory manufacturers and foundries have various requirements respectively.

In order to meet such severe and wide-ranging requirements, we have newly developed an ArF immersion scanner dubbed NSR-S630D, which has three essential features. First, new reticle stage with encoder servo system for position error improvement. Secondly, newly designed projection lens optics with enhanced correction knobs for thermal aberration control. Finally, a newly designed wafer stage with high power motor for throughput enhancement. In the previous papers, we have reported preliminary data for NSR-S630D utilizing abovementioned technologies.

In this paper, we will show the most recent S630D performance in various conditions similar to real productions (Fig1). In customer’s real production, extreme accuracy with high dose conditions and high throughput with many alignment shots condition are often required; therefore, we will demonstrate data for overlay accuracy with high dose conditions obtained after applying thermal aberration correction knobs and in meantime we also demonstrate throughput results achieved by using our alignment sequence, which we call Stream Alignment, using Five-Eye FIA microscope. For productivity enhancements, customers continuously require quick recovery from scanner down due to modifications or maintenance. To demonstrate the capabilities of S630D for quick recovery, we will also report overlay data obtained after wafer stage maintenance. Furthermore, from the viewpoint of yield, reduction of immersion defect becomes more important along

with the device shrinkage. In this paper we will depict defectivity data obtained with the exposure sequence which is decided by using Nikon's new simulator for optimization of wafer stage orbit. The robust performance data under production conditions shown in this paper will demonstrate that NSR630D will be able to realize a high accuracy and high throughput in real production enviroronment.

Furthermore, we will also introduce Nikon's total lithography solutions based on a brand new application software platform, which has been developed in order to handle large amount of data with ease and setup lithography tool smooth and seamlessly. This platform is linked to metrology tool and customers host, which enables data flow automation and feedback loop for scanner calibration. Lastly we will report performance data obtained after utilizing our total lithography solutions.

9426-43, Session 12

Wavelength metrology and control improvements to enable light source extensions to 10nm

Russell Burdt, Thomas P. Duffey, Rahul Ahlawat, John T. Melchior, Joshua J. Thornes, David Dunlap, Ronnie P. Flores, Thomas Bibby, Kevin O'Brien, Will Conley, Mary Haviland, Daniel J. Brown, Cymer LLC (United States)

The semiconductor lithography industry continues to focus on reducing critical dimension (CD) and minimizing CD variations. These industry demands drive light source requirements for improved wavelength stability and better wavelength metrology reproducibility. To meet these requirements, Cymer is thoroughly characterizing and developing enhancements to the wavelength control and metrology modules within the current-generation 193nm immersion light source, the XLR 600ix.

In order to improve wavelength stability for future light sources, a new closed-loop wavelength control algorithm was developed that monitors and corrects for specific wavelength disturbances. With this tone cancellation algorithm, wavelength specifications based on the standard deviation of pulse-to-pulse laser wavelength can be tightened, and the light source contribution to the focus budget can be reduced. Wavelength metrology reproducibility is also addressed by a thorough characterization with new diagnostic capabilities, and specific enhancements that improve wavelength measurement reproducibility. This effort has led to more consistent tool-to-tool performance, as well as reduced performance variations to provide better CD and DOF control.

9426-44, Session 12

Total lithography system based on a new application software platform enabling smart scanner management

Hirotaka Kono, Kazuo Masaki, Tomoyuki Matsuyama, Shinji Wakamoto, Seemoon Park, Taro Sugihara, Yuichi Shibazaki, Nikon Corp. (Japan)

The semiconductor technology roadmap predicts continuous device shrinkage toward 10nm HP and beyond in the coming generations. This means extremely high accuracy will continuously be required from photo-lithography tools in order to enhance on-product yield. In order to achieve higher yield the advanced photo-lithography tools must be equipped with sophisticated tuning knobs on the tool and for the software and must be flexible enough to be applied per layer. Examples of sophisticated tuning knobs include: detailed correction using sub-recipe, intelligent applications for CDU/Overlay tuning, frequent machine maintenance based on wafer metrology results, and so on. This means photo-lithography tools must be capable of handling many types of sub-recipe and parameter simultaneously.

To enable managing such large amount of data easily and setup lithography tools smoothly, we have developed a total lithography solution based on a new software application platform, which we call Plug & Play Manager (PPM). Fig 1 shows a schematic drawing of the lithography system network centering around PPM, which is an integrated control station. PPM has its own graphical user interface, which enables total management of various data. Here various data means recipes, sub-recipes, tuning-parameter, measurement results, and so on. Through PPM, parameter making by intelligent applications such as CDU/Overlay tuning tools can easily be implemented. In addition, PPM is also linked to metrology tools and customer's host computer, which enables data flow automation. The automation is certainly effective for reduction of setup time and calibration time. Based on the measurement data received from metrology tools, PPM calculates high order correction parameters and sends them to the scanners automatically. This scheme can make calibration feedback loops possible. It should be noted that abovementioned functions are running on the same platform through a user-friendly interface. This leads to smart scanner management and usability improvement.

The main functions of PPM are divided into two main categories. One is smooth recipe optimization, the other is stable machine management, which leads to total yield enhancement. By optimizing recipes rapidly and precisely photo-lithographers can achieve higher initial yield and faster ramp of their products. By keeping lithography tools stable, users can improve yield and can eliminate instability during production, which results in yield curve improvement.

In this paper, we will demonstrate the latest development status of Nikon's total lithography solution based on PPM and also describe details of each application; and provide supporting data for accuracy and usability of the system.

9426-45, Session 12

Green solution: 120W ArF immersion light source supporting the next-generation multiple-pattering lithography

Takahito Kumazaki, Takeshi Ohta, Keisuke Ishida, Hiroaki Tsushima, Akihiko Kurosu, Kouji Kakizaki, Takashi Matsunaga, Hakaru Mizoguchi, Gigaphoton Inc. (Japan)

The difficulty of EUV lithography system development has prolonged the industry's dependence on ArF excimer lasers to realize further advancements in lithography process technologies. Smaller CD with reduced cost requires tighter specifications, and the potential extension to 450mm wafers introduces extremely difficult performance challenges on lasers.

One of the most important features of the next generation lasers will be the ability to support green operations while further improving cost of ownership and performance. For example, electricity consumption costs and the dependence on rare gases, such as neon and helium, will become critical considerations for HVM process going forward. As a laser vendor, Gigaphoton continues to innovate and develop solutions that address these important issues. The latest model GT64A with its field-proven, twin-chamber platform has reduced environmental impact while upgrading performance and power.

A variety of green technologies are employed on the GT64A.

The first is the reduction of gas usage. Parameters, such as input power and gas pressure are closely monitored during operations and fed back to the injection/exhaust gas controller system. By applying a special algorithm, the laser gas consumption can be reduced by up to 50%. More than 96% of the gas used by the lasers is neon. Another rare gas that requires attention is Helium. Recently the unstable supply of helium became a serious worldwide issue. To cope with this situation, Gigaphoton is developing lasers that support completely helium-free operations.

The second green technology targets improvement of efficiency. Gigaphoton's Injection-Lock architecture was proven to be superior in efficiency compared with traditional MOPA systems. Gigaphoton is developing a new chamber that reduces the electricity consumption by another 19% by reducing of cross flow fan rotation speed.

Other basic improvements applied to the GT64A are high output power and

wavelength stability. The GT64A can deliver up to 120W of ourput power, which is required by the next generation multiple- patterning processes and 450mm wafers. The industry's highest lasing efficiency is achieved through the proven Injection Lock technology. No additional utilities are required by this 120W light source, and the ingenious optical configuration makes it possible to maintain stable beam qualities.

The automatic output adjustment feature enables the output power to be dynamically optimized to meet the specific requirements of customers' processes. Furthermore, this feature can also prevent the generation of unneeded power, thus contributing to the reduction of the operational cost and environmental impact.

The wavelength-stability of the GT64A has been improved by approximately 50% compared to previous models. This enables very high overlay accuracy, CD control, and small LER required by the next generation multiple-patterning process technologies.

Finally, from the system point of view, a new monitoring system has been developed which provides detailed light source information of each shot of a scanner. It can provide wavelength, energy, E95, etc. In addition, a new on-board metrology tool can monitor beam performance data such as beam profile, pointing, divergence, and polarization.

These technologies and the detailed properties of GT64A will be discussed in detail.

9426-46, Session 12

Immersion and dry scanner extensions for sub-10nm production nodes

Stefan Weichselbaum, ASML Netherlands B.V. (Netherlands)

In parallel to the emerging EUV technology, immersion (ArFi) and dry (ArF/KrF) scanners will remain an essential player in semiconductor device manufacturing. Combined with multi-patterning methods and multiple mask-split/multi-exposure/etch sequences immersion scanners have supported sub-resolution printing for all recent imaging nodes. Progressing towards the 10nm and 7nm imaging node, pattern-placement and layer-to-layer overlay requirements keep progressively scaling down and drives many system improvements in immersion (ArFi) and dry (ArF/KrF) scanners. In this paper we report on the recent performance steps of NXT immersion step&scan systems.

A series of module enhancements in the NXT platform have been introduced; among others, the scanner is equipped with an exposure stages with better dynamics and thermal control. Grid accuracy improvements with respect to calibration, setup, stability, and layout dependency tighten MMO performance and enable mix and match scanner operation. The same platform improvements also benefit focus control. Improvements in detectability and reproducibility of low contrast alignment marks enhance the alignment solution window for 10nm logic processes and beyond.

The system's architecture allows dynamic use of high-order scanner optimization based on advanced actuators of projection lens and scanning stages. This enables a holistic optimization approach for the scanner, the mask, and the patterning process.

Productivity scanner design modifications esp. stage speeds and optimization in metrology schemes provide lower layer costs for customers using immersion technology. This paper will provide further details on the above mentioned scanner improvements. Imaging, overlay, focus, defect and productivity data will be presented.

Conference 9427: Design-Process-Technology Co-optimization for Manufacturability IX

Wednesday - Thursday 25–26 February 2015

Part of Proceedings of SPIE Vol. 9427 Design-Process-Technology Co-optimization for Manufacturability IX

9427-1, Session 1

The daunting complexity of scaling to 7NM without EUV: pushing DTCO to the extreme *(Invited Paper)*

Lars W. Liebmann, IBM Corp. (United States)

The history of semiconductor lithography has shown repeatedly that, given a choice, most of the microelectronics industry will adopt shorter wavelength or higher NA patterning solutions over RET-enhanced incumbent solutions in an attempt to maintain a constant level of design and process complexity. Even though frequency doubling RET such as off-axis-illumination and alternating phase shift were already demonstrated in 365nm lithography, the industry took the path of hardware enabled scaling until the lack of options beyond 193nm immersion lithography forced the adoption of increasingly complex and design invasive RET. The 14nm technology node introduced the process and design communities to the complexity of double patterning. Then the 10nm node increased the pain level by forcing triple patterning and sidewall image transfer solutions. While the end of scaling has been predicted and proven wrong many times over the 65 year history of VLSI, there is now a heightened sense that the escalation in complexity and associated cost, on both the design and process end of the technology, can not continue at the rate observed in the last three technology nodes.

Against this backdrop of staggering increases in patterning, process, and design complexity, prominent semiconductor manufacturers, on the IDM as well as the foundry side of the business, have proclaimed that at least one more cycle of scaling, the 7nm technology node, is feasible without reliance on wavelength-enabled scaling afforded by extreme ultraviolet lithography. This talk will describe specific methodologies used in the Design Technology CoOptimization (DTCO) and will demonstrate how these approaches can be used to quantify the increased complexity and reduced benefit of scaling to 7nm without EUV. Cell architecture constraints and routability challenges as well as process complexity and mask count increases will be contrasted between a 193i and a EUV implementation of the 7nm technology node to demonstrate the usefulness of established DTCO approaches.

9427-2, Session 2

High-coverage of litho hotspot detection by weak pattern scoring

Jinho Park, Jae-Hyun Kang, NamJae Kim, Seung Weon Paek, Steve Kwon, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Marwah Shafee, Mentor Graphics Egypt (Egypt); Wael El-Manhawy, Mentor Graphics Corp. (United States); Kareem Madkour, Mentor Graphics Egypt (Egypt); Joe Kwan, Jean-Marie Brunet, Mentor Graphics Corp. (United States)

Achieving lithographic printability at advanced nodes below 20nm can impose significant restrictions on physical design, including large numbers of complex design rule checks (DRC) and compute-intensive detailed process model checking. Early identifying of yield-limiter hot-spots is essential for both foundries and designers to significantly improve process maturity. A real challenge is to scan the design space to identify hot-spots, and decide the proper course of action regarding each hot-spot.

Building a scored pattern library with real candidates for hotspots for both foundries and designers is of great value. Foundries are looking for the most used patterns to optimize their technology for and identify patterns that should be forbidden, while designers are looking for the patterns that are sensitive to their neighboring context to perform lithographic simulation with their context to decide if they are hotspots or not.

In this paper we propose a framework to data mine designs to obtain set of representative patterns of each design, our aim is to sample the designs at locations that can be potential yield limiting. Though our aim is to keep the total number of patterns as small as possible to limit the complexity, still the designer is free to generate layouts results in several million of patterns that define the whole design space. In order to handle the large number of patterns that represent the design building block constructs, we need to prioritize the patterns according to their importance.

In this paper we propose a scoring scheme that helps in classifying the patterns according to the severity of hot-spots they cause, the probability of their presence in the design and the likelihood of causing a hot-spot. We will show how the scoring scheme helps foundries optimize their master pattern libraries and priorities their efforts in 14nm technology and beyond. According to the calculated score patterns are tagged into 3 groups:

(1) Patterns that drive technology and/or recipe optimization;

(2) Patterns that should be forbidden and appended to DRC/Pattern Matching Check;

(3) Patterns that require designers to perform lithographic simulation verification to ensure they are “Litho-Friendly” with-in their context.

Moreover, we will demonstrate how the hotspot scoring will help improve the runtime of lithographic simulation verification by identifying which patterns need to be optimized to correctly describe candidate hot-spots, so that only potential problematic patterns are simulated.

9427-3, Session 2

A pattern-based methodology for optimizing stitches in double-patterning technology

Lynn T. Wang, Sriram Madhavan, Vito Dai, Luigi Capodieci, GLOBALFOUNDRIES Inc. (United States)

A pattern-based methodology for optimizing stitches is developed based on identifying stitching topologies in a decomposed design and replacing them with pre-characterized, manufacturing-friendly fixing solutions. Stitching is a layout design technique used in Litho-Etch-Litho-Etch (LELE) Double Patterning Technology (DPT), the key enabler for 20nm nodes and beyond. Since decomposing features from one to two complementary mask layers often inflicts conflicting mask assignments, stitching has been introduced so that conflicts can be resolved with minimal area penalties. Current DPT-compliant physical design methodologies use Design Rule Checks (DRCs) to guide layout design decisions for stitching. These DRCs ensure that sufficient overlay stitching areas are drawn to prevent electrical opens caused by process-induced variability, such as mask-to-mask misalignment. However, DRCs do not indicate where and how to stitch, which results in a large variation of stitches being drawn in custom decomposed layout designs. As layout design regularity becomes increasingly more important for achieving high manufacturability and yield, the use of stitches needs to be better controlled.

An automated pattern-based replacement methodology simultaneously promotes layout regularity and optimizes stitches for manufacturability. By identifying stitching topologies in decomposed designs and opportunistically replacing them with consistent predetermined fixes, the design variability is reduced, and the design manufacturability is improved. This proposed methodology requires a topology-based library of stitches to be built a priori, in which each topology is associated with a predetermined fixing solution. A pattern-based engine then searches for matching topologies from the library in the decomposed layout designs. If a match were found, the engine would replace the existing stitch with the predetermined fixing solution. These fixings are opportunistic because only

the DRC-clean replacements are preserved.

The methodology was demonstrated using a 20nm test chip that contains ~8k custom-drawn stitches on the metal 1 layer. To reduce the study's sample size, a pattern classification engine was used to classify the stitches to unique classes. Using exact pattern classification and a 100nm extraction radius, the ~8k stitches reduced to 17 unique classes of stitches. A small library containing 4 stitching topologies was built a priori. For each topology, a corresponding manufacturing-friendly fix was predetermined and stored in the library. Using topology-based pattern matching and replacement engines, the predetermined fixes were opportunistically applied to the layout design. The original 17 unique classes were reduced to 10, which is a 41% reduction in stitching design variation.

9427-4, Session 2

Fast detection of manufacturing systematic design pattern failures causing device yield loss

Jean-Christophe Le Denmat, STMicroelectronics (France)

Starting from the 45nm technology node, systematic defectivity has a significant impact on device yield loss with each new technology node. The effort required to achieve patterning maturity with zero yield detractor is also significantly increasing with technology nodes. Within the manufacturing environment, new in-line wafer inspection methods have been developed to identify device systematic defects, including the process window qualification (PWQ) methodology used to characterize process robustness. Although patterning is characterized with PWQ methodology, some questions remain: How can we demonstrate that the measured process window is large enough to avoid design-based defects which will impact the device yield? Can we monitor the systematic yield loss on nominal wafers? From device test engineering point of view, systematic yield detractors are expected to be identified by Automated Test Pattern Generator (ATPG) test results diagnostics performed after electrical wafer sort (EWS). Test diagnostics can identify failed nets or cells causing systematic yield loss [1],[2]. Convergence from device failed nets and cells to failed design pattern are usually based on assumptions that should be confirmed by an electrical failure analysis (EFA). However, many EFA investigations are required before the design pattern failures are found, and thus pattern failure identification has been costly in time and resources. With this situation, an opportunity to share knowledge exists between device test engineering and manufacturing environments to help with device yield improvement.

This paper presents a new test results diagnostics flow for correlating critical design patterns for manufacturing, with the observed device yield loss. The results obtained with this new flow on a 28nm technology device are described, with the defects of interest and the device yield impact by design pattern. The EFA results to validate the correlation results from this flow are also presented, including physical cross sections. Finally, the application of this new flow for systematic design pattern yield monitoring, compared to classic in-line wafer inspection methods, is discussed.

9427-5, Session 2

Topology and context-based pattern extraction using line-segment Voronoi diagram

Sandeep K. Dey, Panagiotis Cheilaris, Univ. della Svizzera italiana (Switzerland); Nathalie Casati, Maria Gabrani, IBM Research – Zürich (Switzerland); Evanthia Papadopoulo, Univ. della Svizzera italiana (Switzerland)

Early identification of problematic patterns in real designs is of great value. The lithographic simulation tools faces significant timing challenges and to reduce the processing time, selects only a fraction of possible patterns that can have probable area of failure, with the risk of missing some problematic patterns. In this work, we introduce a fast method to automatically extract patterns based on their structure and context, using Voronoi diagram of line-segments. In a recent work that appeared in ICMS 2014, we described our implementation of the line-segment Voronoi diagram in the max-norm and detected problematic locations (gauges) in small design patterns with a few tens of polygons. In this work, we assess our method on larger design layouts (with tens of thousands of polygons). We use gauge locations suggested by the Voronoi diagram of the design polygons for extracting problematic windows or patterns from the design layout. We extract one window per gauge location, with the gauge location as the geometrical center of the window. For each gauge and its associated window, we also compute a score that depends on the structure and context of the surrounding polygons and models how problematic is the pattern contained in the window. The windows are sorted according to their scores. We did experiments for pattern selection in a 22nm design layout macro provided by the IBM-Research Zurich. The design layout had 38584 design polygons (made of 199946 line-segments), Mx layer, and 7079 ORC (Optical Rule Correction) generated markers. We verify our approach by comparing the coverage of our extracted patterns to the ORC generated markers. Our goal is to cover the ORC generated markers with as few patterns as possible. We considered four different side lengths of square windows: 5, 6, 7, and 8 times the pitch length. We observed that the smaller windows are not able to cover all the markers; as we increase the window size the covering of marker increases. The varying window sizes were considered in the early stage of our experiment to take care of the trade-off between the window size and markers covered. We considered a marker to be covered in three different ways, (1) the geometric center of the marker is strictly inside the corresponding window of a gauge, (2) the whole marker rectangle is completely inside the corresponding window of the gauge, and (3) the marker rectangle overlaps with the gauge window. The approach (1) performs best and can detect 100% markers using nearly 5000 windows in less than 20 seconds, the approach (2) can detect 99% markers using 4899 windows in less than a minute, and the approach (3) can detect 100% markers using nearly 5000 windows in less than 3 minutes. To further minimize the number of windows, we applied a heuristic algorithm that tries to put the nearby gauge centers into one window. We observe that the greedy algorithm reduces nearly 30% windows and we can cover all the 7079 ORC generated markers by using 3013 windows.

9427-6, Session 3

A systematic framework for evaluating standard cell middle-of-line (MOL) robustness for multiple patterning

Xiaoqing Xu, The Univ. of Texas at Austin (United States); Brian Cline, Greg Yeric, ARM Inc. (United States); Bei Yu, David Z. Pan, The Univ. of Texas at Austin (United States)

In standard cell library design, inter-cell compatibility is essential for achieving a robust library that can be used in any design implementation, no matter how the cells are arranged or configured.

Historically, inter-cell placement compatibility could be guaranteed by checking all 2-cell combinations, because the lithographic interactions were small in comparison to the cell sizes and limited to single mask layers.

With the industry extending 193nm lithography via multiple patterning, the lithographic interactions now include complex multi-mask interactions that extend beyond 2-cell interactions.

Multiple patterning coloring and decomposition - especially on middle of line (MOL) layers like the Contact-to-Active (CA) layer that routinely cross cell boundaries - breaks the locality of traditional rule checking and makes historical pair-wise cell compatibility checking obsolete.

In cutting-edge technology nodes like 10nm and beyond, N-wise checks are now needed to verify the multiple patterning colorability for cell interactions across boundaries.

Unfortunately, this means that what once was a tractable problem in pair-wise cell checking now becomes an exponential problem in N-wise checking.

In this work, we propose a graph-based approach and divide and conquer technique to reduce the size of the N-wise checks to an acceptable level.

Vertical and horizontal boundary checks are explored in order to predict illegal cell combinations in the placement level.

Our proposed approach evaluates cell compatibility with a two-stage framework: benchmark generation and colorability checking.

The benchmark generation stage uses intelligent sequences of standard cells to begin checking cell compatibility.

First, sequences of cells are abutted, horizontally, without overlapping any two cells at their place and route boundaries.

This horizontal sequence of cells grows exponentially with the number of cells and the length of the sequence.

We manage this exponential growth by exploiting the pattern regularity of the CA layer in the cells, which leads to redundancy among the various sequences.

A graph-based approach and divide and conquer technique are deployed to enable efficient redundancy reduction.

Then, multiple rows of independent sequence cells are combined, vertically, to explore the vertical boundary interactions.

In the second stage, the graph simplification, clique detection and backtrack coloring techniques are deployed in the multiple patterning colorability checker.

We test the proposed two-stage framework with a representative industrial 10nm standard cell library, which consists of 116 logic cells.

The experimental results show that there are only 28 independent cells after the cell redundancy optimization.

Additionally, the proposed techniques help exhaustively build all 3-cell independent sequences.

Moreover, the colorability checks on the two-row and multiple-row benchmarks yields a unique set of observations for the state-of-art 10nm technology:

(1) The four-clique exists due to the row to row interactions, which means triple patterning is infeasible and quadruple patterning needs to be deployed to enable implicit coloring for standard cells;

(2) There is no local five-clique for the CA layer in the 10nm technology used;

(3) For all the benchmarks generated, the colorability for quadruple patterning can be easily proved during the graph simplification stage.

9427-7, Session 3

Self-aligned quadruple patterning-aware standard cell placement

Fumiharu Nakajima, Chikaaki Kodama, Koichi Nakayama, Shigeki Nojima, Toshiya Kotani, Toshiba Corp. (Japan)

Due to shrinking of semiconductor technology node, Self-Aligned Quadruple Patterning (SAQP) will be one of the leading candidates for sub-14nm node and beyond. Despite its robustness against overlay, SAQP is a challenging process since predicting wafer image instantly is almost impossible and we must follow stricter constraint than in triple patterning process in order to design feasible layout.

A feasible layout drawing for SAQP process has been studied so far. Nakayama et al. analyzed SAQP construction process and revealed that patterns could be distinguished into three kinds1. Kodama et al. proposed the first SAQP layout method using pre-colored grid2 which can obtain resultant layout painted into three colors, but strict constraints are imposed to draw a feasible layout. Nakajima et al. relaxed a part of the routing constraints and developed a standard cell layout method without using pre-coloring grid3. Therefore, SAQP-aware standard cell placement is natural issue for further SAQP application.

Triple patterning-aware standard cell placement was studied by Yu et al4. They presented the first systematic study for the triple patterning-aware ordered single row placement. It can solve cell placement and color assignment simultaneously. However, we cannot easily apply their method to SAQP process since there are following problems for standard cell placement. (1) When coloring conflicts occur between two adjoining cells, they may not be solved easily since SAQP layout has stronger coloring constraints. In triple patterning layout, color of patterns can be exchanged each other flexibly under no coloring conflicts, but in SAQP, only two of three colors are permitted to exchange each other. (2) SAQP layout cannot use stitch to solve coloring conflict like triple patterning, so another counter method is required. (3) Since trimming process is necessary for SAQP, trim mask form and its OPC should also be considered in cell placement stage.

In this paper, we present a framework of SAQP-aware standard cell placement considering the above three problems. When standard cell is placed, the proposed method try to solve coloring conflicts between two cells as many as possible by exchanging two of three colors (Fig. 1). If some conflicts remain between adjoining cells, dummy space will be inserted and they are connected keeping coloring constraints. Trim mask is derived according to feasible cell placement. Some examples will be shown to confirm effectiveness of the proposed framework. To our best knowledge, this is the first framework of SAQP-aware standard cell placement.

9427-8, Session 3

Impact of a SADP flow on the design and process for N10 M2 layer

Syed Muhammad Yasser Sherazi, Werner Gillijns, Darko Trivkovic, Boris Vandewalle, Praveen Raghavan, Julien Ryckaert, Diederik Verkest, Kurt G. Ronse, Gregory R. McIntyre, IMEC (Belgium); Vassilios Gerousis, Cadence Design Systems, Inc. (United States)

This work addresses the difficulties in creating a manufacturable M2 layer in the Self-Aligned-Double-Patterning (SADP) process for N10 and proposes a couple of solutions. As a first approach the place and route tool is restricted to only guarantee an SADP-compliant design. Together with the standard SADP flow (consisting of a core and keep layer), we highlight the challenges to obtain a reasonable process window, based on silicon. The main challenges come from a very complex keep mask, consisting of complicated 2D structures which are very challenging for 193i litho. Therefore, a solution is proposed from processing standpoint and design standpoint. From processing standpoint we propose an adapted SADP process flow to address the difficulties in creating a manufacturable M2 layer in the SADP process. From design side we optimize design rules and dummy placement to increase manufacturability. These techniques are not only assessed on their manufacturability but also on their impact on the electrical properties.

Double Keep Process

From processing side an additional Keep layer by a double patterning strategy is defined and in these test cases an LELE approach is assumed. This 2-Keep solution has the advantage of (i) being very easy to decompose in two colors and (ii) results in 2 easy-to-print 1D layers. From simulation standpoint, the impact on the process window using this approach is investigated. Additionally, some preliminary wafer data has shown the proof-of-concept. Furthermore, on the design side exploration on different design rule sets are made in order to quantify their impact on the process window. Figure 1, shows the difference between single and double Keep Mask.

Adaptive Dummy Layer Insertion

The experiments show that metal layout patterns, which are printed by the Trim mask, experience the highest levels of image transfer sensitivity. Therefore, there is a need to carefully generate a layout that leads to an error-free final product. The insertion of dummy assists in the layout is based on the fact that by addition of extra assists, the shape of the intended layer and the electrical properties can be maintained more easily. This also helps in protection of the intended connections on the intended edges, increasing thereby the process window. With the application of this technique, robust layout patterns are generated. Figure 2, shows both the original layout and the modified layout after the application of the algorithm.

Targets

With these solutions the intention is to show that the trade-offs for a 2-Keep solution or different design rules can lead to larger process windows. Furthermore, with the insertion of dummy layers can the design rules be change to reduce the area. For a required process window, there is a tradeoff between 1-Keep or 2-Keep versus different design rules. Depending on the application it might be better to have a tighter design and use the 2-Keep solution or if a single Keep is required the design rules need to be tightened to allow a certain process window. This paper proposes design based and process based solutions to improve an SADP solution for an M2 layer. The proposed solutions include double patterning Keep layer on one side, dummy placement on the other hand with and an updated design rule set.

9427-9, Session 3

An efficient auto TPT stitch guidance generation for optimized standard cell design

Nagaraj C. Samboju, Synopsys (I) Pvt. Ltd. (India); Soo Han Choi, Srini Arikati, Erdem Cilingir, Synopsys, Inc. (United States)

As the technology continues to shrink below 14nm, triple patterning lithography (TPT) is the obvious choice for decomposition of dense layers such as Metal1. However, this increases the complexity of standard cell design, as it is very difficult to develop a TPT compliant layout without compromising on the area. Hence, this emphasizes the importance to have an accurate stitch generation methodology to meet the standard cell area requirement as defined by shrink factor of the technology. In this paper, we present an efficient auto TPT stitch guidance generation technique for optimized standard cell design. The techniques described in this paper are protected under pending patents. The basic idea here is to first identify the conflicting polygons based on the Fix Guidance1 solution developed by Synopsys. Fix Guidance is a reduced sub-graph containing minimum set of edges along with the connecting polygons, by eliminating these edges in a design a 3-color conflict can be resolved. Once the conflicting polygons are identified using this method, they are then categorized into four types2 (Type 1 to 4). The categorization is based on number of interactions a polygon has with the coloring links and Triangle loops of fix guidance as shown in fig.1 & fig. 2. Type 1 corresponds to polygons having less than or equal to three links. Polygons interacting with one triangle loop and an additional coloring link are categorized as Type 2. Type 3 corresponds to polygons interacting with two triangle loops whereas polygons interacting with more than three triangle loops are categorized as Type 4. For each type a certain criteria for keep out region is defined, based on which the final stitch guidance locations are generated. This technique provides various possible stitch locations to the user and helps the user to select the best stitch location considering both design flexibility (max. pin access/ small area) and process-preferences. The fig 1.c & fig 2.c, shows a sample layout with categorized polygons and all possible stitch locations generated by this method.

Based on this technique, a standard cell library for place and route (P&R) can be developed with colorless data and a stitch marker defined by designer using our proposed method. After P&R, the full chip (block) would contain the colorless data and standard cell stitch markers only. These stitch markers are considered as “must be stitch” candidates. Hence during full chip decomposition it is not required to generate and select the stitch markers again for the complete data; therefore it reduces the decomposition time significantly. We implemented this technique for the decomposition of Metal 1 layer in 10nm node and could get the decomposed TPT complaint layout with an acceptable runtime.

9427-10, Session 3

Yield-aware mask assignment using positive semidefinite relaxation in LELECUT triple patterning

Yukihide Kohira, Univ. of Aizu (Japan); Chikaaki Kodama, Toshiba Corp. (Japan); Tomomi Matsui, Atsushi Takahashi, Tokyo Institute of Technology (Japan); Shigeki Nojima, Satoshi Tanaka, Toshiba Corp. (Japan)

Multiple patterning technique enables us to fabricate small features without using advanced technologies such as extreme ultra violet (EUV) lithography. Triple patterning lithography (TPL) is one of the most promising techniques in the 14 nm logic node and beyond. In order to realize a target pattern, various types of techniques including design for manufacturability1–21 are used in addition to a basic litho-etch process with optimized mask.

Two types of TPL technologies are often discussed in literature. In LELELE, litho-etch process is repeated three times. However, it is difficult to achieve high yield due to native conflict and overlay problems. In LELECUT, the third mask called cut (or trim) process removes a part of a fabricated pattern. It is used to improve the quality of fabricated patterns as well as to enhance the flexibility of layout. However, it has overlay problems and lithographical limitations. In order to prevent yield loss caused by overlay error as much as possible, LELECUT mask assignment which is tolerant to overlay error is desired.

To our best knowledge, two LELECUT mask assignment methods have been proposed. In,13 LELECUT mask assignment problem is formulated as an integer linear programming problem. Although it minimizes the weighted summation of the number of conflicts and stitches, the effect of cuts on layout quality is not taken into account. In,21 LELECUT mask assignment problem is solved by positive semidefinite relaxation. Although it minimizes the weighted summation of the number of conflicts, stitches, polygons in the cut mask, the yield of obtained layout is also not discussed. Fig. 1 shows mask assignments in LELECUT. A target pattern is shown in Fig. 1 (a). The layouts obtained by two LELECUT mask assignments which are represented by blue, magenta, and cut masks without overlay are shown in Fig. 1 (b) and Fig. 1 (d). These mask assignments have no conflicts, no stitches, and the number of polygons in the cut mask is same. The layouts of them with overlay in which blue, magenta, and cut masks move to the upper right, the lower left and the left, respectively, are shown in Fig. 1 (c) and Fig. 1 (e), respectively. The former is expected to have lower yield than the latter since a longer dimension of features such as p1 and p2 is determined by the cut mask and is affected directly by the overlay error. The length of a boundary of a feature that is determined by cut mask should be small enough to prevent the yield loss caused by overlay error.

In this paper, we propose a method that obtains an LELECUT assignment which is tolerant to overlay error. The proposed method is an enhancement of the method proposed in21 and uses positive semidefinite relaxation and randomized rounding technique. In our method, the cost function that takes the length of boundary of features determined by the cut mask into account is introduced to obtain an overlay tolerant LELECUT assignment. The effect of the proposed method is discussed by using lithographical simulation.

9427-11, Session 4

DTCO at N7 and beyond: patterning and electrical compromises and opportunities *(Invited Paper)*

Diederik Verkest, Julien Ryckaert, Praveen Raghavan, Arindam Mallik, Sushil S. Sakhare, Bharani Chava, Yasser Sherazi, Philippe Leray, Abdelkarim Mercha, Jürgen Bömmels, IMEC (Belgium); Gregory R. McIntyre, IMEC (United States); Kurt G. Ronse, Aaron Thean, Zsolt Tökei, An Steegen, IMEC (Belgium)

No Abstract Available

Conference 9427: Design-Process-Technology Co-optimization for Manufacturability IX

9427-13, Session 5

Standard cell design in 7nm node: EUV versus immersion

Bharani Chava, Peter Debacker, Yasser Sherazi, Praveen Raghavan, Werner Gillijns, IMEC (Belgium); David Rio, ASM Belgium N.V. (Belgium); Ahmad Elsaid, Mircea Dusa, ASML (Belgium); Julien Ryckaert, IMEC (Belgium)

While waiting for EUV lithography to become ready for adoption, we need to create designs compatible with both EUV single exposure as well as with 193i multiple splits strategy for technology nodes 7nm and below needed to keep the scaling trend intact. However, the standard approach of designing standard cells in two dimensional directions is no more valid owing to insufficient resolution of 193-i scanner. Therefore, we propose a standard cell design methodology which exploits purely one dimensional interconnects.

In IMEC, three options for cell design are being considered, M1, either Vertical or Horizontal and M2 being orthogonal to the M1 choice and a 2D option compatible with EUV. The process options for these options are shown in Table 1. Key challenges for both these options are the challenges posed by Middle end of line (MOL) which are shown in Figure 1 . We pursue M1 vertical option in IMEC for standard cell libraries with fewer than 9 tracks to ensure proper tolerances for design rules in MOL between FIN and GATE layers. The choice of M2 pitch of 32nm driving the cell height allows to satisfy a minimum M1 area of 1500nm2 for a 9 Track cell and hence chosen. The fin pitch of 24nm matches with the M2 pitch with a gear ratio of 3/4 to enable 8 active fins in a 9 Track cell.

Given the regularity of the design, all the cells in a standard cell library can be built based on a combination of a set of 13 basic templates. In this work, 45 cells have been designed based on this approach, which can be extended to a much larger set of cells. The cells are being placed and routed staring from a fully 1D M2 SAQP compatible. At a standard cell library level, we observed an average area penalty of 12.5% in 1D cells compared to 2D cells. Comparison for an AO22D0 is shown in Figure 2. However, this penalty will have to be re-assessed after Place and route as parameters such as M2 usage within cell and port accessibility can largely influence the overall area.

This paper is going to present a systematic approach of design choices to be made in 1D cell design with regards to transition between N10 to N7. The design flavors in this paper are shown in Table 1. The primary focus will be on: (1) Systematic design approach for 1D cells and their pros and cons compared to 2D counterparts. (2) Highlight the challenges in MOL for nodes below N10. (3) SAQP compliance of the 1D standard cell library after Place and Route. (4) PV band study of selected layers. (5) Decomposition strategy for the block mask.

9427-14, Session 5

Layout dependent effects analysis on 28nm process

Helen Li, Mealie Zhang, Waisum Wong, Semiconductor Manufacturing International Corp. (China); Huiyuan Song, Wei Xu, Michel L. Cote, Cadence Design Systems, Inc. (United States); Yifan Zhang, Hua Ding, Cadence Design Systems, Inc. (China); Jason Huang, Cadence Design Systems, Inc. (Taiwan); Ya-Chieh Lai, Philippe Hurat, Cadence Design Systems, Inc. (United States)

Advanced process nodes introduce new variability effects due to increased density, new material, new device structures, and so forth. This creates more and stronger Layout Dependent effects (LDE), especially below 28nm. These effects such as WPE (Well Proximity Effect), PSE (Poly Spacing Effect) change the carrier mobility and threshold voltage and therefore make the device performances, such as Vth and Idsat, extremely layout dependent. In traditional flows, the impact of these changes can only be simulated after the block has been fully laid out, the design is LVS and DRC clean. It's too late in the design cycle and it increases the number of post-layout iteration. SMIC and Cadence collaborated to develop a method for SMIC 28nm process to embed several LDE sources into a LDE kit. We integrated this LDE kit in custom analog design environment, for LDE analysis at early design stage. These features allow circuit and layout designers to detect the variations caused by LDE, and to fix the weak points caused by LDE. In this paper, we will present this method and how it accelerates design convergence of advanced node custom analog designs by detecting early-on LDE hotspots on partial or fully placed layout, reporting contribution of each LDE component to help identify the root cause of LDE variation, and even providing fixing guidelines on how to modify the layout and reduce the LDE impact.

9427-15, Session 5

Breaking through 1D layout limitations and regaining 2D design freedom-part I: random 2D layout decomposition and stitching techniques for hybrid optical and self-aligned multiple patterning

Hongyi Liu, Jun Zhou, Yijian Chen, Peking Univ. (China)

As 1-D design rules are adopted in leading-edge logic ICs, the patterning bottleneck has shifted from chasing down the half pitch (HP) of fin/gate grating structures to metal1(M1) decomposition and synthesis. A widely discussed approach is to decompose 2D M1 layer into regular grating arrays in one direction and connect these metal lines with vias and via links in the other (orthogonal) direction. Unlike the HP scaling capability of the metal grating structures defined by spacer based self-aligned multiple patterning (SAMP), via links are still patterned by optical lithography with their density limited by the optical resolution. In addition, shrinking random via/contact CD and HP has become increasingly difficult due to its extremely small process window. Even considering EUV and DSA technologies, scaling via/contact CD & HP to sub-10nm still seems to be prohibitive. In other words, the brute-force 1-D gridded design relying on heavy cut/via/contact patterning may not be sustainable, and we need to research scalable patterning solutions that maximize the 2-D design freedom and minimize the cut/via/contact steps.

These incentives have stimulated our proposal of a computation efficient random 2-D layout decomposition and synthesis technique which combine optical and self-aligned multiple patterning processes. Similar to double patterning, we develop a polynomial time algorithm to decompose the target layout into two parts, each of them containing one or multiple sets of unidirectional components (e.g., in X and Y directions as illustrated in Fig. 1). Unlike a decomposed layout (in double patterning) which still contains random 2-D patterns with its HP capability limited by the optical resolution, each decomposed layout in this new approach may contain multiple sets of unidirectional components. Each component can be oriented in a different direction but all of them (in one decomposed layout) can be patterned together by a SAMP+cut process. Without using vias (e.g., for M1 connection in 1-D gridded design), the final random 2-D patterns are formed by stitching two parts together, as shown in Fig. 1(e). Therefore, the HP capability of each decomposed layout (and the stitched random 2-D patterns) is defined by SAMP processes. Considering that SAMP processes only allow limited CD range, the remaining question is then how the synthesized 2-D random patterns will accommodate desired CD flexibility. The first goal of layout decomposition is to generate two sets of mandrel and cut masks (totally 4 masks) to form the unidirectional patterns, as illustrated in Fig. 3. However, the CD range available from a SAMP process is limited. To accommodate more CD flexibility, it is necessary to introduce assisting feature(s) overlapping the original feature to enlarge its CD. Fortunately, this does not produce insurmountable computation barriers owing to its simple role of CD compensation.

Moreover, a full-chip layout usually includes different regions with various pattern densities. Two cut masks, if designed as clear-field masks, can act in a way similar to double patterning to generate some specific 2-D random patterns whose density is twice of what is available by the optical (single-exposure) lithography. First, we construct a conflicting graph according to the distance between two features. Graph simplification technique is then

applied to group the patterns in the target layout. Accordingly, different decomposition methods are developed to decompose them. For those groups containing only large features that can be resolved by optical lithography, we collect them into one cut mask. For those groups that can be formed by double patterning, we decompose them into two cut masks. Those features with the highest density will be decomposed using the proposed technique. We tested our layout decomposition/synthesis algorithm using 15-nm cells designed by NCSU. A M1 layer decomposition algorithm is shown in Fig. 2 and an example of decomposition process is shown in Fig. 4. The results verify the functionality of our method.

9427-28, Session 5

Layout optimization with assist features placement by model based rule tables for 2x node random contact

Jin-Hyuck Jun, Shinyoung Kim, Chan-Ha Park, Hyun-Jo Yang, DongGyu Yim, SK Hynix, Inc. (Korea, Republic of)

Model based rule tables use lithographic simulation to reduce the number of mask-making and wafer-printing experiments that are required to generate rule tables for Rule Based Assist Feature (RBAF) placement. Its inputs are a set of lithography models and MRC rules, and its outputs are rule tables that can be used by RBAF to place AFs.

Since RBAF is needed now and in the future, what is also needed is a faster method to create the AF rule tables. The current method typically involves making masks and printing wafers that contain several experiments, varying the main feature configurations, AF configurations, dose conditions, and defocus conditions – this is a time consuming and expensive process. In addition, as the technology node shrinks, wafer process changes and source shape redesigns occur more frequently, escalating the cost of rule table creation. Furthermore, as the demand on process margin escalates, there is a greater need for multiple rule tables: each tailored to a specific set of main-feature configurations.

Model based rule tables create a set of test patterns, and evaluates the simulated CD at nominal conditions, defocused conditions and off-dose conditions. It also uses lithographic simulation to evaluate the likelihood of AF printing. It then analyzes the simulation data to automatically create AF rule tables. It means that analysis results display the cost of different AF configurations as the space grows between a pair of main features. In summary, model based rule tables method is able to make it much easier to create rule tables, leading to faster rule-table creation and a lower barrier to the creation of more rule tables.

9427-16, Session 6

Full chip two-layer CD and overlay process window analysis

Rachit Gupta, John L. Sturtevant, Shumay D. Shang, Mentor Graphics Corp. (United States)

In-line CD and overlay metrology specifications are typically established by starting with design rules and making certain assumptions about error distributions which might be seen in manufacturing. Lot disposition criteria in photo metrology (rework or pass to etch) are set assuming worst case assumptions for CD and overlay respectively. For example poly to active overlay specs start with poly endcap design rules and make assumptions about active and poly lot average CDs, and incorporate general knowledge about poly line end rounding to ensure that leakage current is maintained within specification. In practice however, when a given lot is measured for poly to active overlay, mean active CD and mean poly CD values are already known. This knowledge should in theory guide the allowed misalignment error which can protect yield sufficiently for that specific lot. So there is an opportunity for improved fab productivity by using such information.

Furthermore, there is an opportunity to go beyond design rule based specifications with general guard bands to full-chip design specific model-based dispositioning. Such an approach can leverage not only the above mentioned coupling of CD and overlay errors, but can interrogate all layout configurations for both layers to help determine lot-specific, design-specific CD and overlay dispositioning criteria for the fab. An additional advantage of such an approach is that orientation-specific analysis can be conducted to determine whether allowed overlay errors may be asymmetric due to design-process window interactions.

This paper will investigate examples of two-layer model-based analysis of CD and overlay errors. It is shown, somewhat non-intuitively, that there can be small preferred misalignment asymmetries which should be respected to protect yield. We will show this relationship for double patterning metal and the via-metal overlap. We additionally present a new method of displaying edge placement process window variability, akin to traditional CD process window analysis

9427-30, Session PS1

20nm CMP model calibration with optimized metrology data and CMP model applications

Ushasree Katakamsetty, GLOBALFOUNDRIES Singapore (Singapore); Dinesh Koli, GLOBALFOUNDRIES Inc. (United States); Sky Yeo Wee Kwong, Colin C. W. Hui, GLOBALFOUNDRIES Singapore (Singapore); Ruben G. Ghulghazaryan, Mentor Graphics Corp. (Armenia); Burak Aytuna, Jeff S. Wilson, Mentor Graphics Corp. (United States)

Chemical Mechanical Polishing (CMP) is the essential process for planarization of wafer surface in semiconductor manufacturing. CMP simulation model will help to early predict CMP hotspots and minimize the CMP and CMP induced Lithography and Etch defects. In this paper, CMP modeling technology from Mentor Graphics is used to build a multilayer 20nm Cu-CMP model and study hotspots. In this paper we will demonstrate calibration of CMP model with only 1 spare wafer, instead of 4 spare wafers and with same accuracy of CMP model. This is achieved by modifying the CMP modeling parameters and target conditions in the CMP Optimize tool. The created model was successful in fitting the measured data. Validation of the model showed that it follows trends closely for a broad range of metal width and densities on different production designs.

The next phase of this project is to close the loop by using the CMP model to improve the insertion of the dummy fill shapes. With a quality CMP model and a correct by construction fill solution this work can be fairly straight forward. However, the current advanced technologies complicate the complexity of fill because there are a number of manufacturing processes that influence fill methodology to improve the robustness and uniformity of the design. Finally, we provide DFM recommendations to the designers on CMP hotspots fixing methodologies.

9427-31, Session PS1

Topography aware DFM rule based scoring for silicon yield modeling

Vikas Tripathi, Ushasree Katakamsetty, GLOBALFOUNDRIES Singapore (Singapore); Colin Hui, globalfoundries (Singapore)

DFM rule base scoring is associated with Manufacturability rules checking and applying scoring to predict yield for an input design. Achieving good DFM score is one of the key requirements to get high yield. The DFM score varies from 0 to 1 range where 1 consider as highest score and 0 is the lowest score. The DFM scoring methodology is currently limited to DFM recommend rules and their associated failure rates.

In contrast to failure mechanism, CMP topography places a key role to it.

CMP Topography variation can introduce printability challenges and leads to re-prioritization of the DFM rules. The geometries falling in extreme topography (low and high) region or steep gradient transition will be susceptible to higher probability of failure and hence should be treated differently. Features at extreme topography (low and high) region should have lower DFM score as compared to feature falling in average topography region. Currently the conventional DFM score does not vary for a similar feature across the topography range. So as to achieve good correlation with topography and silicon yield, it is very critical to incorporate topography information while computing DFM score for accurate Yield prediction.

In this paper, we will present advance DFM analysis flow to compute DFM score that incorporate topography variation along with recommend rule scoring using complex scoring model for achieving high silicon yield correlation. This is anticipated to converge the yield modelling and actual yield figure.

9427-32, Session PS1

A compact model to predict pillar-edge-roughness effects on vertical nanowire MOSFETs using the perturbation method

Pu Wang, Chuyang Hong, Qi Cheng, Yijian Chen, Peking Univ. (China)

The surrounding-gate (SG) nanowire MOSFET is widely considered as a promising device structure for future CMOS scaling. Among many possible nanowire MOSFET schemes, vertical nanowire MOSFET is especially attractive as it provides a perspective solution to break through the physical limits of horizontal scaling. On the other hand, process variations such as pillar-edge roughness (PER) is becoming a serious concern with aggressive downscaling of device dimensions. PER can significantly change the nanowire/channel shape and potentially impact the device behavior. However, to our knowledge, little progress has been made in developing an efficient compact model capable of guiding IC engineers to gain physical insight into the PER related phenomena. In this paper, we shall present such a compact model to correlate PER to vertical nanowire MOSFET device variability using the perturbation method.

In our model, the electric potential φ is divided as: $\varphi=\varphi0+\varphi1$ ($\varphi1$ $\varphi0$) according to the perturbation method. The zeroth-order solution (?0) corresponds to the ideal cylindrical nanowire MOSFET device behavior and the first-order solution ($\varphi1$) describes the PER effect. In 3-D Poisson's equation, the PER effect is described by a small deviation of the nanowire radius from the ideal (single) value: $\Delta r=t(\theta,z)$, as shown in Fig. 2. We separate the 3-D Poisson's equation into a 2-D Poisson's equation (zeroth-order) and a 3-D Laplace's equation (first-order) using the perturbation method. The zeroth-order solution ($\varphi0$) of the 2-D Poisson's equation has been well known. The variable separation method is used to solve the 3-D Laplace's equation in cylindrical coordinate, and we obtain the coefficients Amn and Bmn in equation (2) by considering the Fourier series. The PER induced drain current fluctuation ΔIds (ΔIds=Ids-I0ds) can be analytically derived by inserting $\varphi0$ and $\varphi1$ into equation (5). Other key device parameters such as subthreshold slope and DIBL can be solved based on ΔIds.

We also carry out TCAD simulations to investigate the PER effects. In our TCAD simulations, we consider a simple mixed-frequency radius fluctuation functions, e.g., $\Delta r=A*\sin(2\theta)+B*\sin(2K\theta)$. Here ($A*\sin2\theta$) describes the low-frequency fluctuation while ($B*\sin2K\theta$) is for high-frequency components, as shown in Fig. 3. The diameter of the channel is chosen to be 7 nm and 10 nm, and the channel length is set as 15 nm. Apparently the PER induced device variability is more serious in a 7-nm channel than in a 10-nm device, as shown in Fig. 4 (a). In Figs. 4 (b) -(d), we can see drain currents vary with the amplitude of PER fluctuation function and its frequency as well. More calculation results will be reported in this paper, followed by a theoretical discussion on developing a relevant metrology approach to characterize the PER angular spectrum which can be related to vertical nanowire MOSFET device variability.

9427-33, Session PS1

Efficient etch bias compensation techniques for accurate on-wafer patterning

Mohamed Salama, Ayman Hamouda, GLOBALFOUNDRIES Inc. (United States)

As technology development advances into deep submicron nodes, it is very important not to ignore any systematic effect that can impact CD uniformity and the final parametric yield. One important challenge for OPC is in choosing the proper etch process correction flow to compensate for design-to-design etch shrink variations. Although model-based etch compensation tools have been commercially available for a few years now, rules-based etch compensation tables have been the standard practice for several nodes. In our work, we study the limitations of the rules-based etch compensation versus model-based etch compensation. We study a 10nm process and provide the details of why using Model-Based Etch Process Correction can achieve up to 15% improvement in final CD uniformity. We also provide a systematic methodology for identifying the proper etch correction technique for a given etch process and assessing the potential accuracy gain when switching to the model-based etch correction.

9427-34, Session PS1

An efficient litho hotspot severity analysis methodology using Calibre PATTERN MATCHING and DRC application

ZeXi Deng, Semiconductor Manufacturing International Corp. (China); ChunShan Du, Mentor Graphics Shanghai Electronic Technology Co. (China); Lin Hong, Semiconductor Manufacturing International Corp. (China); Liguo Zhang, Mentor Graphics Shanghai Electronic Technology Co. (China); JinYan Wang, Semiconductor Manufacturing International Corp. (China)

As the IC industry moves forward to advanced nodes, the manufacturing process window, especially lithography, tightens continuously and design layout pattern count rapidly increase in certain design area as critical feature size shrinkage, this definitely brings more and more challenges to lithography process and requires a tool and method to carry forward the manufacturing hotspots to designers with identifying, ranking clearly and quickly to let designers decide and fix the hotspots according to the hotspot severity or ranking.

Using pattern classification and pattern matching (Calibre PM) technology, incorporating with simulation-based litho DFM check (Calibre LFD) technology, SMIC has built a unique hotspot pattern analysis flow to analyze the potential yield detractor patterns with ranking related to real fab process in millions of design layouts.

In this paper, we described the hotspot pattern classification, pattern definition with variety, the method of pattern scoring and ranking, the automatic flow of storing the hotspots and applications for design modification or guidance of process enhancement.

9427-35, Session PS1

A holistic methodology to drive process window entitlement, and its application to 20nm logic

Lalit Shokeen, Ayman Hamouda, Mark Terry, GLOBALFOUNDRIES Inc. (United States); Dan J. Dechene, Stephen D. Hsu, Michael Crouse, Pengcheng Li, Keith D.

Gronlund, Gary Guohong Zhang, Brion Technologies, Inc. (United States)

Early in the process development cycle, the technology definition is locked down using somewhat risky assumptions on what the process can deliver once it matures. In this early phase of the development cycle, detailed design rules are starting to be codified, while the wafer patterning process is still being fine-tuned. As the process moves along the development cycle, and wafer processes are dialed in, key yield improvements focus on variability reduction. Design retargeting definitions are tweaked and finalized, and finely tuned etch models for target compensation are applied, to accurately capture the more mature wafer process. The resulting mature patterning process is quite different from the one developed during the early stages of the technology definition.

By using advanced model-based OPC solutions, the impact of process changes can be minimized, so as to be limited largely to model updates. Model-based OPC solutions, including model-based sub-resolution assist features (MB-SRAF), process-window OPC solvers, and model-based hotspot repair mechanisms, can limit the extent of OPC recipe changes required for iterations along this development curve. While these changes can translate into improved yield on-wafer, there may still be a gap between the delivered process window and the process window entitlement realizable with systematic study and recipe tuning.

In this paper we describe an approach and flow to drive continuous improvement during late process development and into production. First, we establish the process window entitlement within the design-space by utilizing advanced mask optimization (MO) combined with the baseline process (i.e., model, etch compensation, and design retargeting). Secondly, gaps to the entitlement are used to identify issues with the existing production OPC solution and to drive continuous improvements to close these performance gaps across the critical design rules. Finally, fine-tuned OPC recipes are combined with measured ArF scanner fingerprint data, including pupil, aberrations and stage dynamics, for a holistic lithographic assessment of the design space. We demonstrate this flow on a 20 nm contact layer.

9427-36, Session PS1

Practical DTCO through design/patterning exploration

Neal V. Lafferty, Jason Meiring, Dan Schumacher, Mentor Graphics Corp. (United States); James A. Culp, IBM Corp. (United States); Glenn Wawrzynski, Gurpreet S. Lamba, Mohamed S. Bahnas, Joe O'Neill, Kostas Adam, John L. Sturtevant, Chris McGinty, Mentor Graphics Corp. (United States)

Design Technology Co-Optimization (DTCO) becomes more important with every new technology node. Often, complex patterning issues can no longer wait to be detected experimentally using test sites because of compressed technology development schedules. Simulation must be used to discover complex interactions between an iteration of the design rules, and a simultaneous iteration of an intended patterning technology. The problem is often further complicated by an incomplete definition of the patterning space. The DTCO process must be efficient and thoroughly interrogate the legal design space for a technology to be successful. In this paper we present our view of DTCO, called Design and Patterning Exploration. Three emphasis areas are identified and explained with examples: Technology Definition, Technology Learning, and Technology Refinement. The Design and Patterning Exploration flows are applied to a logic 1x metal routing layer. Using these flows, yield limiting patterns are identified faster using random layout generation, and can be ruled out or tracked using a database of problem patterns. At the same time, a pattern no longer in the set of rules should not be considered during OPC tuning. The OPC recipe may then be adjusted for better performance on the legal set of pattern constructs. The entire system is dynamic, and users must be able to access related teams' output for faster more accurate understanding of design & patterning interactions. In the discussed example, the ground rules and opc recipe is tuned at the same time, leading to faster design rule revisions, as well as improved patterning through more customized OPC and RET.

9427-37, Session PS1

Comparison of OPC job prioritization schemes to generate data for mask manufacturing

Kenneth Jantzen, Mentor Graphics Corp. (United States); Travis Lewis, Vijay Veeraraghavan, Minyoung Park, GLOBALFOUNDRIES Inc. (United States); Stephen H. Kim, Gordon Russell, Mark C. Simmons, Mentor Graphics Corp. (United States)

Delivering mask ready OPC data to the mask shop on-time is critical for a foundry to meet the cycle time commitment for a new product. With current OPC resource sharing technology, different job scheduling algorithms are possible, such as, priority based resource allocation, fair share resource allocation, or just in time (JIT) scheduling. In order to maximize computer cluster efficiency, minimize the cost of the data processing and deliver data on schedule, the trade-offs of each scheduling algorithm need to be understood. Using actual production jobs, each of the scheduling algorithms will be tested in a production tape-out environment. Each scheduling algorithm will be judged on its ability to deliver data on schedule and the trade-offs associated with each method will be analyzed. It is now possible to introduce advance scheduling algorithms to the OPC data processing environment to meet the goals of on-time delivery of mask ready OPC data while maximizing efficiency and reducing cost.

9427-38, Session PS1

Design analyzer: A physical design profiling and data mining tool

Shikha Somani, Piyush Verma, Sriram Madhavan, Fadi Batarseh, Robert C. Pack, Luigi Capodieci, GLOBALFOUNDRIES Inc. (United States)

As the complexity of VLSI designs continues to grow, undesirable and unexpected interactions between the geometrical constructs in the physical layout and manufacturing process flows are emerging. These interactions are particularly hard to predict as the charactacteristic length scale of the defect inducing design geometry is highly variable. Ideally, a physical design verification step should be able to catch all the geometrical constructs in the physical design that can be potential yield detractors. However, the traditional DRC decks lack the sensitivity required to catch all that is undesirable in the physical design. The design rule decks today are based on a large number of pre-decided dimensional configurations that are checked for in a design and assigned either a pass or fail flag. In other words, these decks only check for 'known' bad configurations and together with the silicon data generate only 'supervised' learning data sets. While physical design is very rich in intralayer and interlayer dimensional data, only a very small fraction of this data is really mined and analyzed when performing DRC verification.

A true physical layout profiling/verification tool would be one that does not make any apriori assumptions about the configurations or their dimensions that it expects to find in the design. It would not only classify known geometries into pass/fail buckets, but also discover new geometries and their dimensions for which no process data is available. Thus, in addition to generating the supervised data sets that the DRCs decks attempt to do today, it would also generate input data for unsupervised learning such that new design-process correlations can be built over time. The design analyzer tool presented in this work is built with this aim. At the heart of the design analyzer is a statistical engine that communicates with a database populated with comprehensive intralayer and interlayer dimensional information from the VLSI design. Feeding into this database

is a data transformer module that reads in the output from a myriad of measurement extraction tools and converts into a universal common format (UCF). The UCF is chosen such that no critical information is lost from the output of the measurement extraction tools, while maintaining a data size that is reasonable to store and process for a large number of designs. The measurement tools extract all possible dimensions in the design over very large dimensional ranges without any preconceived notion of good or bad configurations. The design analyzer not only allows the comparison of various configurations in a given design, it also allows the comparison of one VLSI design to the another. Such comprehensive data mining of large designs allows us to systematically store, analyze and interpret data. At the front end, a reporting engine presents all the relevant statistical information about the design in an easy to consume succinct format which helps in making more informed engineering and business decisions.

9427-39, Session PS1

The cell pattern correction through design-based metrology

Yonghyeon Kim, Kweonjae Lee, Jinman Chang, Taeheon Kim, Daehan Han, Kyusun Lee, Ae-Ran Hong, JinYoung Kang, Bumjin Choi, Joo-Sung Lee, Kyehee Yeom, Jooyoung Lee, Hyeongsun Hong, Kyupil Lee, Joosun Choi, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

Starting with the sub 2Xnm node, the process window becomes smaller and tighter than before.

Pattern related error budget is required for accurate critical-dimension control of Cell layers. Therefore, lithography has been faced with its various difficulties, as distribution, overlay, patterning etc.

The distribution of cell pattern and overlay management is the most important factors in DRAM field. We had been experiencing that the fatal risk is caused by the patterns located in the tail of the distribution. The overlay also induces the various defect sources and misalignment issues.

Even though we knew that these elements are important, we could not classify the defect type of Cell patterns. Because there is no way to gather massive small pattern CD samples in cell unit block and to compare layout with cell patterns by the CD-SEM.

The CD- SEM is used in order to gather these data through high resolution, but CD-SEM takes long time to inspect and extract data because it measures the small FOV. (Field Of View)

However, the NGR(E-beam tool) provides high speed with large FOV and high resolution. Also, it's possible to measure an accurate overlay between the target layout and cell patterns because they provide DBM. (Design Based Metrology)

By using this measurement method, we get the distribution of the Cell blocks, type of pattern defects and wafer uniformity.

Moreover, we could analyze data which consider the surrounding environment such as block edges.

The Cell distribution and the kind of defects were changed according to the each cell block surrounding environment in chip. Also, we could calculate the composited average distribution of measured many cell blocks that we didn't know when we analyzed each block through the composite technology. (In house Tool)

If we fail to identify these cell distributions, the process window would appear severely narrower than the real window and we may miss the chance to reinforce cell process window. We should be considered that cell size difference to target layout may have effects on yield of extreme edge chip.

While we proceed with this research,

In spite of being the cell pattern having the same pitch, Bridge defects were occurred in the specific order of block edge. But we could not find this reason from the inspected distribution, because it was hidden in the unmatched pair phenomenon due to DPT.

We got to know that real patterns are not same location with drawn layout patterns by DBM.

We expected this pattern shift induces the pattern bridge, so we challenged as various ways in order to find the shift amount. We have defined the difference of the center coordinates between the target layout and the contour outline is amount of pattern shift. Calculates the each skew between the Target Layout center coordinates and the coordinates Contour GDS. Then, we extract average skew in the cell block axial direction.

Finally, we got to know real cell shift quantity in cell blocks, and the cell pattern that had the max shift quantity induced the pattern bridge through a series of procedures of the above. (Figure1. Red line) Improved result was obtained by modified layout. Finally, the bridged patterns disappeared. By using massive measured data, we extract the result that it is persuasive by applying the various analysis techniques, as cell distribution and defects, the pattern shift correction etc.

It has become to use as a criterion for yield enhancement through enlarged PWQ margin. These analysis methods give a high degree of completion of the Cell Pattering and the Distribution. We are certain that it help also in the development of advanced process and Cell Layout.

9427-40, Session PS1

Breaking through 1D layout limitations and regaining 2D design freedom-part II: stitching yield modeling and optimization

Jun Zhou, Yijian Chen, Peking Univ. (China)

Self-aligned multiple patterning (SAMP) is a promising technology for IC device scaling to sub-10nm half pitch (HP). However, a major barrier preventing SAMP from dominating the critical layer patterning is that an efficient method for random 2-D layout decomposition and synthesis has not been found yet. In another paper, we propose an efficient layout decomposition and synthesis algorithm that can deal with random 2-D layout in polynomial time, based on a hybrid optical and self-aligned multiple patterning process. Similar to double patterning, we decompose the target layout into two parts and each part contains one or multiple sets of unidirectional patterns. Each set of patterns can be oriented in a different direction but all the decomposed patterns in the same part can be formed by a SAMP+cut process. Without using vias, the final random 2-D patterns are formed by stitching two parts together, as shown in Fig. 1. Therefore, the yield performance of the stitching process is critical to the above hybrid patterning process. Although a target layout can often be decomposed correctly, its synthesis/stitching need more consideration because of the overlay inaccuracy and cut hole CD variation when separately patterning two decomposed parts. For example, the optimal overhang in the orthogonal stitching must be designed and added to the ends of decomposed lines. In this manner, we can simultaneously avoid the non-touch of two orthogonal lines (due to line misalignment) and wrong touch of the neighbor line as well. In this paper, we shall discuss the impacts of various process fluctuations on the stitching yield, develop a statistical yield model, and carry out parametric optimization for the related stitching process. There exist two basic stitching mechanisms in the hybrid patterning process: orthogonal stitching (OS) and parallel stitching (PS). Through physical yield modeling and simulation, the optimal overhang in the orthogonal stitching and optimal overlap in the parallel stitching can be identified. Moreover, design rules to specify the minimum safe distance between stitched features are required to tolerate misalignment and CD variations. Fig. 4 shows three typical OS yield performance for three stitching cases shown in Fig. 3. We shall discuss more details of the parametric optimization for yield improvement in our paper.

9427-41, Session PS1

Automatic DFM methodology for bit line pattern dummy

Mohamed Bahr, Mentor Graphics Egypt (Egypt)

This paper presents an automated DFM solution to generate Bit Line Pattern

Dummy for memory devices. Dummy shapes are aligned with memory functional bits to ensure uniform and reliable memory device. This paper will present a smarter approach that uses an analysis based technique for adding the dummy shapes that have different types according to the space available. Experimental results based on layout of Mobile dynamic random access memory (DRAM).

9427-18, Session 7

Quantitative evaluation of manufacturability and performance for ILT produced mask shapes using a single-objective function

Heon J. Choi, Wei-Long Wang, Chidam G. Kallingal, GLOBALFOUNDRIES Inc. (United States)

The continuous scaling of semiconductor devices is quickly outpacing the resolution improvements of lithographic exposure tools and processes. This one-sided progression has pushed optical lithography to its limits, resulting in the use of well-known techniques such as Sub-Resolution Assist Features (SRAF's), Source-Mask Optimization (SMO), and double-patterning, to name a few. These techniques, belonging to a larger category of Resolution Enhancement Techniques (RET), have extended the resolution capabilities of optical lithography at the cost of increasing mask complexity, and therefore cost. One such technique, called Inverse Lithography Technique (ILT), has attracted much attention for its ability to produce the best possible theoretical mask design. ILT treats the mask design process as an inverse problem, where the known transformation from mask to wafer is carried out backwards using a rigorous mathematical approach. One practical problem in the application of ILT is the resulting contour-like mask shapes that must be "Manhattanized" (composed of straight edges and 90-deg corners) in order to produce a manufacturable mask. This conversion process inherently degrades the mask quality in inspection and CD variation point of view as it is a departure from the "optimal mask" represented by the continuously curved shapes produced by ILT. However, simpler masks composed of longer straight edges reduce the mask cost as it lowers the shot count and saves mask writing time during mask fabrication, resulting in a conflict between manufacturability and performance for ILT produced masks . In this study, various commonly used metrics will be combined into an objective function to produce a single number to quantitatively measure a particular ILT solution's ability to balance mask manufacturability and RET performance. Several metrics that relate to mask manufacturing costs (i.e. mask vertex count, ILT computation runtime) are appropriately weighted against metrics that represent RET capability (i.e. process-variation-band, edge-placement-error) in order to reflect the desired practical balance. This well-defined scoring system allows straight-forward direct comparison of several masks with varying degrees of complexities. Using this method, ILT masks produced with increasing mask constraints will be compared, and it will be demonstrated that using the smallest minimum width for mask shapes does not always produce the optimal solution.

9427-19, Session 7

Akaike information criterion to select well-fit resist models

Andrew Burbine, David Fryer, John L. Sturtevant, Mentor Graphics Corp. (United States)

In the field of model design and selection, there is always a risk that a model is over-fit to the data used to train the model (e.g., the selection of gauges from a layout). A model is well suited when it describes the system and not the stochastic behavior of the particular data collected. K-fold cross validation is a method to check this potential over-fitting to the data by calibrating with 'k'-number of folds in the data, typically between 4 and 10. Model training is a computationally expensive operation, however, and given a wide choice of models, calibrating each one repeatedly becomes prohibitively time consuming. Akaike information criterion is an information-theoretic approach to model selection based on the maximized log-likelihood for a given model that only needs a single calibration per model. It is used in this study to demonstrate model ranking and selection among a suite of compact modelforms that have various amounts and types of terms to describe photoresist behavior.

9427-20, Session 7

Fast source optimization by clustering algorithm based on lithography properties

Masashi Tawada, Waseda Univ. (Japan); Takaki Hashimoto, Keishi Sakanushi, Shigeki Nojima, Toshiya Kotani, Toshiba Corp. (Japan); Masao Yanagisawa, Nozomu Togawa, Waseda Univ. (Japan)

Lithography is a technology to make circuit patterns on a wafer. UV light diffracted by a photomask forms optical images on a photoresist. Then, a photoresist is melt by an amount of exposed UV light exceeding the threshold. The UV light diffracted by a photomask through lens exposes the photoresist on the wafer. Its lightness and darkness generate patterns on the photoresist. As the technology node advances, the feature sizes on photoresist becomes much smaller. Diffracted UV light is dispersed on the wafer, and then exposing photoresists has become more difficult.

Exposure source optimization, SO in short, techniques for optimizing illumination shape have been studied. Although exposure source has hundreds of grid-points, all of previous works deal with them one by one. Then they consume too much running time and that increases design time extremely. How to reduce the parameters to be optimized in SO is the key to decrease source optimization time.

In this paper, we propose a variation-resilient and high-speed cluster-based exposure source optimization algorithm. We focus on image log slope (ILS) and use it for generating clusters. When an optical image formed by a source shape has a small ILS value at an EPE (Edge placement error) evaluation point, dose/focus variation much affects the EPE values. When an optical image formed by a source shape has a large ILS value at an evaluation point, dose/focus variation less affects the EPE value. In our algorithm, we cluster several grid-points with similar ILS values and reduce the number of parameters to be simultaneously optimized in SO. Our clustering algorithm is composed of two STEPs: In STEP 1, we cluster grid-points into four groups based on ILS values of grid-points at each evaluation point. In STEP 2, we generate super clusters from the clusters generated in STEP 1. We consider a set of grid-points in each cluster to be a single light source element. As a result, we can optimize the SO problem very fast. Experimental results demonstrate that our algorithm runs speed-up compared to a conventional algorithm with keeping the EPE values.

9427-21, Session 8

Deploying DFM in an age of design restrictions: A foundry perspective *(Invited Paper)*

Cyrus E. Tabery, Intel Corp. (United States)

No Abstract Available

9427-22, Session 9

Statistical modeling of intra-cell and inter-die SRAM circuit variability

Qi Cheng, Yijian Chen, Peking Univ. (China)

Process variations such as line edge/width roughness (LER/LWR) and random dopant fluctuations (RDF) are serious design concerns as FinFET

devices are scaled down to sub-10 nm. Self-aligned multiple patterning (SAMP) processes have been adopted in critical-layer IC patterning while their process variability differs significantly from conventional optical lithography. Understanding and modeling the statistical fluctuation of circuit performance and the induced yield loss has become an urgent issue in the leading-edge logic IC design. In this paper, we report a statistical model to predict the intra-cell and inter-die SRAM circuit performance variability when fabricated by several typical SAMP processes.

For example, multi-modality variations in CDU and LER are often observed in a SAMP process in which mandrels and multiple types of spacers may co-exist and strongly interact. As shown in Fig. 1, when an inverter is fabricated by a self-aligned sextuple patterning (SASP) process, fins consist of either 1st spacers or 2nd spacers. This will result in two types of statistical behavior of the inverter cells. To predict the induced circuit behavior, the statistical distribution of threshold voltages is first obtained through TCAD simulation or compact modeling. By combining it with the actual circuit layout/structure, the inverter delay time can be calculated by (1) given on the next page. The flow chart of Fig. 2 shows our modeling methodology and Fig. 3 shows some examples of the inverter delay thus calculated. In our calculation, we considered 7-nm node FinFET and the corresponding device parameters such as power supply voltage (Vdd) and channel doping are extracted from [1]. The preliminary results clearly confirm the inverter delay is significantly different between these two types of circuits.

As demonstrated in Fig. 4, reading failure of a SRAM cell occurs when the reading voltage (Vread) at node "R" is higher than the trip point of the inverter (Vtrip) [4]. Both intra-cell and inter-die process variability in a FinFET based SRAM circuit is illuminated in Fig. 5. Following the method described above in Fig. 2, the standard deviation of Vtrip, Vread and the probability of reading failure Pread vs. standard deviation of the threshold voltage (of FinFETs fabricated by the second spacers) are shown in Fig. 6. Moreover, the corresponding yield model/analysis of SRAM circuit will be discussed in our paper.

9427-23, Session 9

Variability-aware compact modeling and statistical circuit validation on SRAM test array

Ying Qiao, Costas J. Spanos, Univ. of California, Berkeley (United States)

It is widely recognized that, in nano-scale CMOS technology, variation in manufacturing process has emerged as a fundamental challenge to IC design. While foundries are working hard to mitigate process variability, the design houses are asking for accurate and appropriate models to handle statistical circuit performance evaluation. Variability-aware compact transistor models can enable statistically optimized designs by capturing device variations in a concise, yet physically accurate fashion, and they are relatively easy to integrate with existing CAD tool flow. In addition, these compact transistor models require customized test structure designs as well as proper statistical characterization procedures. In this work, we have extracted variability-aware compact transistor models based on electrical measurements from carefully designed SRAM array test structures. We have also built a custom Monte Carlo simulation platform to utilize these compact transistor models in the IC design flow.

Our collaborating team has designed bit-transistor accessible SRAM array test structures, as shown in Figure 1, using foundry's 28nm FDSOI technology. This design enables high-volume transistor I-V measurements as well as cell DC characteristics measurements. We have collected I-V measurement data [1] of the pass-gate transistor within each SRAM cell across 5 rows and 512 columns of the test structure array. These I-V curves are then used for compact variability model characterization. Meanwhile, we have also measured the DC write noise margin characteristics of those SRAM cells. These unit circuit performance data will later be compared with our custom MC simulation results to demonstrate the validity and efficacy of these variability-aware compact transistor models.

As discussed in [2], properly selecting model parameters for statistical characterization is essential for compact variability modeling. We have proposed and implemented a stepwise parameter removal procedure to obtain an optimal model parameter set for both model extraction and custom MC simulation. Based on the test structure design, we have chosen the industry standard PSP 103.1 model with nominal parameter values from a foundry's default model. As depicted in Figure 2, the final four-parameter-set has clear physical property representations in the model equation, reasonable I-V curve model fitting error and far simpler statistical correlation structure. The various components of variability observed in these model parameters are extracted and added to the model cards for statistical circuit simulation.

Figure 3 shows the comparison of direct measurements (top) vs. custom MC simulations using extracted model parameters (bottom). The middle row of "standard" MC simulations based on the default design kit, is added for complete comparison and clear visualization. Our results to this stage demonstrate that the far simpler statistical structure, represented by only the four physical parameters that were selected, matches the full MC results.

In the immediate future we will focus on exploiting the simple statistical structure of the extracted parameters shown in Figure 2, in order to capture the non-linear correlations and the non-Gaussian distributions through appropriate parametric transformations. The goal is to demonstrate that important non-normality in the measured data can be predicted by our simplified model. We will also attempt to leverage the apparent clustering made visible in the simplified scatterplot matrix in order to identify faulty measurements or faulty devices in large sets of test patterns.

9427-24, Session 9

Layout optimization and trade-off between 193i and EUV-based patterning for SRAM cells to improve performance and process variability at 7nm technology node

Sushil S. Sakhare, Darko Trivkovic, Julien Ryckaert, Abdelkarim Mercha, Diederik Verkest, Aaron Thean, IMEC (Belgium); Mircea V. Dusa, ASML Leuven (Belgium)

Fin-FET Technology scaling to sub 7nm node using 193 immersion scanner is restricted due to reduced margins for process. The cost of the process and complexity of designs is increasing due to multi-patterning to achieve area scaling using 193i scanner. Processing Fins using SAQP is extremely challenging due to increasing aspect ratio of Fins at 24nm pitch. For SRAM cell, to enable Fin design requires etching of Fins in very narrow widow; Hence Fin patterning requires an optimum solution at lower cost. In this paper, we propose Fin-cut mask design used for Fin-pattering for 112 SRAM cell using 193i scanner(Fig. 4) and its comparison with EUV(Fig. 5). The maximum electrical performance is observed for 122 SRAM cell instead of 112 SRAM cell for 10nm technology[1]; Hence Fin-cut pattern is simplified further for 122 SRAM cell at 7nm with 5% improvement in process margins for newly optimized pattering solution for 193i scanner as well as for EUV.

At 7nm node, minimum area of isolated patterns and aggressive tip to tip constrains scaling of SRAM cell. A non-uniform Fin-pitch SRAM cell design is possible with aggressive middle of line (MOL) scheme where active local interconnect is patterned using SADP and five block masks at 42nm pitch (Fig. 3). This choice of MOL pattering increases cost exponentially along with drastic reduction in process margin. Under EUV assumption, MOL can be patterned as single print resulting in SRAM cell area gain of 58% from 10nm technology. In order to simplify process using 193i and to reduce cost of the technology, we propose a solution to design SRAM cell with increased height of the cell where MOL active is patterned using 2 keep masks instead of 5 block masks. The increased height of cell reduces resultant area gain to 50% with an additional benefit of placing all Fins at uniform pitch (uniform fins); Thus optimized uniform Fin SRAM cell gives area scaling at lower cost using 193i.

For unidirectional designs, margin require to ensure landing of VIA over gate MOL and active MOL is not sufficient when first metal is parallel to gate; Hence for reliable technology, first metal should be orthogonal to active MOL. For metal orthogonal to MOL carrying Bit-lines(BL/BLB) and word-line(WL) in 2nd metal (orthogonal to first metal) gives more than 30%

speed improvement for SRAM cell due to reduction of resistance of WL at improved contact margin for 193i and EUV patterning solution. If the 1st metal is patterned using single print EUV or LELE+SADP instead of SAQP then it will reduce resistances of Bit-line and supply lines by increasing effective widths of patterns which is constrained by SAQP patterning(Fig. 2).

[1]sushil sakhare, Kenichi Miyaguchi, et al. "Simplistic simulation based device VT targeting technique to determine technology high density LELE gate patterned FinFET SRAM in sub-10nm era" IEEE Transactions on Electron Devices January 2015 {accepted with minor revisions}.

9427-25, Session 10

Incorporating DSA in multipatterning semiconductor manufacturing technologies

Juan Andres Torres, Mentor Graphics Corp. (United States); Yasmine A. Badr, Univ. of California, Los Angeles (United States); Yuansheng Ma, Joydeep Mitra, Mentor Graphics Corp. (United States); Puneet Gupta, Univ. of California, Los Angeles (United States)

Multi-patterning is the process of record for many sub 10nm process technologies. The drive to higher densities has required the use of double and triple patterning for several levels. This reduces the profitability of the new processes especially for low volume products in which the mask set is a large percentage of the total cost. For that reason there has been a strong incentive to develop technologies like EUV, direct write or DSA to reduce the total number of masks needed in a new technology node.

A simple approach to integrate multi-patterning with DSA is to perform DSA grouping and MP decomposition in sequence whether it is: grouping-decomposition or decomposition-grouping. However, in this paper we describe why the simple approaches are sub-optimal from the point of view of design compliance or error placement.

Traditionally, DSA cylinder grapho-epitaxy only allows single-size holes in a single patterning approach as the diblock copolymers cannot be locally modified on a per guiding-pattern basis. This introduces design constraints that can be too strict for the intended layout. However, once multiple patterning is allowed, it is possible to come up with decomposition approaches that increase the design flexibility by combining a hybrid (litho-DSA) multiple patterning approach allowing different size holes or bar structures.

For processes in which only single holes of a constant diameter are required, there are several regions of interest for the pitch. The first is the "sub-assembly" range which is below the natural pitch (L0) of the diblock copolymer. In this region, grouping is not possible as the target pitch would cause the system to be in a phase transition region. Above the sub-assembly region is the "dsa-distance" defining the maximum distance at which consecutive holes can be grouped together. In addition, "forbidden-distance" defines a range of distances that are longer than the dsa-distance but modulation of the guiding pattern is not possible; thus the pitch cannot be stretched to the desired value. Finally there is a "litho-distance" which refers to the distance between target holes that can be resolved in a single exposure.

In the case where the process allows for additional shapes (i.e. bars or holes of larger width), the applicable metric of interest is the "litho-distance" as it defines a traditional pitch split multi-patterning distance. The spatial distribution and density of non-dsa-printable content at the end limits the possibility to reduce the number of total patterning steps.

Processes that integrate DSA and MP in a grouping-decomposition approach are likely to reduce the total number of masks for a given layout. Fewer elements need to be decomposed; and if conflicts arise it is possible to ungroup contacts and change the mask assignment to resolve conflicts in a way similar to how stitches are used in traditional multi-patterning conflict resolution. However, the placement error of larger groups limits how long a guiding pattern can be, since larger groups may exhibit worse placement error.

On the opposite side of the spectrum, a decomposition-grouping approach will result in a larger number of singletons which exhibit better error placement characteristics but can give rise to many more locations which cannot be decomposed. In those cases, grouping single contacts may resolve the conflicts.

This paper examines the multiple tradeoffs between design compliance and placement error on the different naïve decomposition strategies and highlights the need for custom dsa-aware multiple patterning algorithms.

9427-12, Session 11

A new lithography hotspot detection framework based on AdaBoost classifier and simplified feature extraction

Tetsuaki Matsunawa, Toshiba Corp. (Japan); Jhih-Rong Gao, Bei Yu, David Z. Pan, The Univ. of Texas at Austin (United States)

Under the low-k1 lithography process, lithography hotspot detection and elimination in both physical verification and physical design have become very important for reducing the process optimization cost and improving manufacturing yield. This paper proposes a highly accurate and low-false-alarm hotspot detection framework using new layout feature extraction and machine learning techniques. To define an appropriate layout feature for classification model training, we propose a novel feature space evaluation index. Furthermore, by applying a robust classifier based on the probability distribution function of layout features, our framework can achieve very high accuracy and almost zero false alarm. Our key contributions include (1) simplified yet effective layout feature extraction: a simple yet highly effective layout feature with high linear separability and low-dimensional space is defined by using our feature space index. By applying our feature space index for layout representation, a density-based feature is defined. Fig. 1 indicates the basic concept of the density-based feature. (2) Boosting-based classification model: a weakly nonlinear learning algorithm is developed by using simplified layout feature. The robust Adaboost classifier in conjunction with weakly nonlinear classifiers using a probability distribution function of simplified features is able to detect hotspots accurately with extremely low false alarm.

Our hotspot detection method consists of two phases, "Learning phase" and "Testing phase". In the learning phase, a training layout is given and a classification model is calibrated after optimization and extraction of a layout feature. In the testing phase, a verification layout that is not the same as the training layout and includes unknown hotspots is used as the input. After the feature extraction from the verification layout, labels, which consist of -1 for non-hotspots and +1 for hotspots, are predicted by using the classification model trained in the learning phase. The experimental results show that our method can achieve over 95% hotspot detection accuracy with almost zero false alarm and outperform the best published results for the ICCAD 2012 benchmarks. We believe this simple but effective methodology is promising to dramatically reduce the manufacturing and process optimization cost.

9427-26, Session 11

Design layout analysis and DFM optimization using topological patterns

Ji Xu, Karthik N. Krishnamoorthya, Edward Teoh, Vito Dai, Luigi Capodieci, GLOBALFOUNDRIES Inc. (United States); Jason Sweis, Ya-Chieh Lai, Cadence Design Systems, Inc. (United States)

During the yield ramp of semi-conductor manufacturing, data is gathered on specific design-related process window limiters, or yield detractors, through a combination of test structures, failure analysis, and model-based printability simulations. Case-by-case, this data is translated into design

for manufacturability (DFM) checks to restrict design usage of problematic constructs. This case-by-case approach is inherently reactive: DFM solutions are created in response to known manufacturing marginalities as they are identified.

In this paper, we propose an alternative, yet complementary approach. Using design-only topological pattern analysis, all possible layout constructs of a particular type appearing in a design are categorized. For example, all possible ways via forms a connection with the metal above it may be categorized. The frequency of occurrence of each category indicates the importance of that category for yield. Categories may be split into sub-categories to align to specific manufacturing defect mechanisms. Frequency of categories can be compared from product to product, and unexpectedly high frequencies can be highlighted for further monitoring. Each category can be weighted for yield impact, once manufacturing data is available.

This methodology is demonstrated on representative layout designs from the 28 nm node. We fully analyze all possible categories and sub-categories of via enclosure such that 100% of all vias are covered. The frequency of specific categories is compared across multiple designs. The 10 most frequent via enclosure categories cover ≥90% of all the vias in all designs. KL divergence is used to compare the frequency distribution of categories between products. Outlier categories with unexpected high frequency are found in some designs, indicating the need to monitor such categories for potential impact on yield.

9427-27, Session 11

Automation for pattern library creation and in-design optimization

Rock Deng, Sid Hone, JinYan Wang, Semiconductor Manufacturing International Corp. (China); Yifan Zhang, Cadence Design Systems, Inc. (China); Jason Sweis, Ya-Chieh Lai, Cadence Design Systems, Inc. (United States); Hua Ding, Cadence Design Systems, Inc. (China); Jason Huang, Cadence Design Systems, Inc. (Taiwan); Elain Zou, Semiconductor Manufacturing International Corp. (China)

Semiconductor manufacturing technologies are becoming increasingly complex with every passing node. Newer technology nodes are pushing the limits of optical lithography and requiring multiple exposures with exotic material stacks for each critical layer. All of this added complexity usually amounts to further restrictions in what can be designed. Furthermore, the designs must be checked against all these restrictions in verification and sign-off stages. Design rules are intended to capture all the manufacturing limitations such that yield can be maximized for any given design adhering to all the rules.

Most manufacturing steps employ some sort of model based simulation which characterizes the behavior of each step. The lithography models play a very big part of the overall yield and design restrictions in patterning. However, lithography models are not practical to run during design creation due to their slow and prohibitive run times. Furthermore, the models are not usually given to foundry customers because of the confidential and sensitive nature of every foundry's processes. The design layout locations where a model flags unacceptable simulated results can be used to define pattern rules which can be shared with customers.

With advanced technology nodes we see a large growth of pattern based rules. This is due to the fact that pattern matching is very fast and the rules themselves can be very complex to describe in a standard DRC language. Therefore, the patterns are left as either pattern layout clips or abstracted into pattern-like syntax which a pattern matcher can use directly. The patterns themselves can be multi-layered with "fuzzy" designations such that groups of similar patterns can be found using one description. The pattern matcher is often integrated with a DRC tool such that verification and sign-off can be done in one step. The patterns can be layout constructs that are "forbidden", "waived", or simply low-yielding in nature. The patterns can also contain remedies built in so that fixing happens either automatically or in a guided manner.

Building a comprehensive library of patterns is very difficult task especially when a new technology node is being developed or the process keeps changing. The main dilemma is not having enough representative layouts to use for model simulation where pattern locations can be marked and extracted. This paper will present an automatic pattern library creation flow by using a few known yield detractor patterns to systematically expand the pattern library and generate optimized patterns. We will also look at the specific fixing hints in terms of edge movements, additive, or subtractive changes needed during optimization. Optimization will be shown for both the digital physical implementation and custom design methods.

9427-29, Session 11

A methodology to optimize design pattern context size for higher sensitivity to hotspot detection using pattern association tree (PAT)

Shikha Somani, Piyush Verma, Piyush Pathak, Sriram Madhavan, Luigi Capodieci, GLOBALFOUNDRIES Inc. (United States)

At advanced VLSI technology nodes, design-process interactions have become very complex. Pattern-based flows have emerged as promising tools to capture this complexity[1]. Typically, design hotspots are classified into patterns with a fixed radius, and these fixed radius patterns are used to detect process weak points in new designs. Since different kinds of physical processes in the manufacturing flow have different radii of influence, there is a need to determine the optimal pattern radius for efficient hotspot detection. The methodology described here uses a combination of pattern classification and pattern search at different radii to create a directed graph, referred to as the Pattern Association Tree (PAT). The nodes of this graph correspond to patterns with varying radii. The pattern association tree is then carefully pruned based on the relevance, sensitivity and context area of each pattern node. The critical patterns are selected by traversing the tree and ranking the patterns based on their degree in the graph. The resulting set of variable radii patterns are very good predictors of hotspots and possess a wide range of applications, ranging from verification (design verification decks) to modification (decks that modify designs to improve their manufacturability).

Conference 9428: Advanced Etch Technology for Nanopatterning IV

Monday - Wednesday 23–25 February 2015

Part of Proceedings of SPIE Vol. 9428 Advanced Etch Technology for Nanopatterning IV

9428-1, Session 1

Blazing the trail through industry inflection points: We've done it before - We'll do it again *(Invited Paper)*

George A. Gomba, IBM Corp. (United States)

No Abstract Available

9428-2, Session 1

Status of EUV lithography *(Invited Paper)*

Anthony Yen, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

No Abstract Available

9428-3, Session 1

Scaling challenges for contact etching in logic devices *(Invited Paper)*

Eric A. Hudson, Lam Research Corp. (United States)

Logic device scaling presents several challenges for the etching of contacts. For contacts without self-alignment structures, the as-printed CD of the opening must be reduced considerably and this is typically accomplished while etching the ARC layer. Controlling the magnitude of CD shrink across different feature dimensions and shapes is difficult but can be addressed using advanced plasma etch schemes based on modulated process conditions. For self-aligned contact (SAC), conventional etch processes are limited by tradeoffs between 3 key requirements: protection of the barrier corner, deep etching in the small space created between the spacers, and minimal etch depth loading between features with different opening dimensions. These SAC challenges are addressed by a novel Atomic Layer Etch cyclic process. Plasma deposition of a thin layer of fluorocarbon polymer is followed by activation of the surface etch reaction by ion bombardment, which removes a corresponding increment of silicon dioxide and resets the surface for the next cycle. This process is shown to break the typical tradeoff between high etch selectivity and etch depth loading.

9428-4, Session 2

Etch patterning for advanced devices *(Invited Paper)*

Effendi Leobandung, IBM Thomas J. Watson Research Ctr. (United States)

Recent trend in CMOS technology shows migration towards new device structures. In order to reduce leakage at very small dimension, FINFET has been introduced into the roadmap. This introduces new challenges on etch patterning due to topography. Other devices structures beyond FINFET will also stress etch patterning such as Nanowire. New material introduction to replace Si such as SiGe and III-V will also add new challenges to etch patterning. In this paper, we will discuss these challenges.

FINFET gate etch and spacer etch are two of the most challenging steps. For gate last flow, the dummy gate etch is very similar to planar polysilicon gate etch. Selectivity > 1:100 can be easily achieved between polysilicon and silicon dioxide. However, for gate first flow, the gate stack consists of Si/Metal/HfO2 on FINFET topography, which makes gate etch very challenging. Significant over etch is needed to clear the gate materials from FIN side wall, so very high selectivity is needed between the multiple etch materials. Figure 1 shows the x-section of such gate without significant erosion of FIN itself [1]. A hot chuck chlorine based etch was used in this case. For spacer etch, similar high selectivity between nitride spacer and silicon is also needed. Complete spacer removal from FINFET sidewall is needed to allow epitaxial growth on FIN side wall as shown in Figure 2 [2]. In both gate and spacer etch, tapered FIN profile reduces the etch difficulty, since it allow more reactive ion to attack the gate and/or spacer on the tapered FIN sidewall. However, device degradation is observed with tapered FIN angle as shown in Figure 3.

Nanowire represents the next evolution from FINFET where the gate now surrounds the channel. With gate material on the bottom of the channel, it is impossible to remove the gate with conventional anisotropic RIE process. To overcome the challenge, one structure has been demonstrated utilizing a non conventional gate etch process to remove the gate material from under the nanowire as shown in Figure 4 [3]. Spacer etch in Nanowire is also more complicated than FINFET due to requirement to remove the spacer from under the nanowire. To improve process window, we can remove the spacer and nanowire under and above it altogether.

New materials are also being proposed to replace silicon such as SiGe [4] and III-V [5]. For both materials, high selectivity and low damage gate etch and spacer etch are required. Figure 5 shows the cross section of SiGe FINFET where excellent FIN profile and gate profile can be achieved with careful optimization. For III-V InGaAs MOSFET, the material is even more prone to damage than SiGe. Early MOSFET work has always rely on low damage gate patterning such as wet etch or lift-off. We have demonstrated that similar performance can be achieved with anisotropic low damage RIE gate etch.

9428-5, Session 2

Challenges in high-aspect ratio contact (HARC) etching for DRAM capacitor formation *(Invited Paper)*

Yongjin Kim, Sangdo Lee, SK Hynix, Inc. (Korea, Republic of); Taewoo Jung, SK hynix (Korea, Republic of); Byoungseok Lee, SK Hynix, Inc. (Korea, Republic of); Nohjung Kwak, SK hynix (Korea, Republic of); Sung-Ki Park, SK Hynix, Inc. (Korea, Republic of)

As design rule of DRAM shrinks, one of the most serious obstacles to overcome is to attain enough capacitance to comply with the refresh specification. The cell size shrink results in intrinsic decrease of the surface area of storage node. And the area decrease causes the decrease of the capacitance. To compensate the area decrease due to the design rule shrinkage, height of the storage node should be increased or high dielectric constant material should be implemented. The increase of the storage node height along with the design rule shrinkage brings about high aspect ratio contact (HARC) formation. In the HARC etching, many essential requirements such as CD uniformity, vertical profile, process margin and etc. should be satisfied. The CD uniformity not only of the contact hole but also of the space between adjacent contact holes determines the distribution of the cell capacitance and leakage characteristics. The CD uniformity is mainly determined by the mask etching. Recently, it was found that the CD uniformity of the space between contact holes becomes worse along with the design rule shrinkage. And the worse CD uniformity comes from the tilted profile of the hard mask. Obtaining vertical contact profile is a traditional problem in HARC etching. To achieve large enough bottom CD fundamentally erodes side surface of the upper part of the contact and thus forms so called bowed profile. Serious bowed profile decreases the

minimum space between adjacent contact holes and induces electrical leakage. In this paper, these issues and related challenges will be presented. And various approaches to understand the mechanism of the issues and to resolve them will be touched.

9428-6, Session 2

Dry etch challenges for CD shrinkage in memory process *(Invited Paper)*

Takaya Matsushita, Takanori Matsumoto, Hidefumi Mukai, Suigen Kyoh, Koji Hashimoto, Toshiba Corp. (Japan)

We present some challenges and solutions on Dry etch process for Flash memory process. Requirement to the Dry etch process for critical dimension (CD) shrinkage are becoming increasingly difficult. One example, pattern collapse that occur in reason for high aspect ratio are one of great concern for line and space patterning in the sub-20 nm half pitch. Shallow Trench Isolation (STI) fabrication process is particularly sensitive to pattern collapse. Aspect ratio reduction and precise control of Si etch profile are needed to prevent pattern collapse. As a one of method to lower aspect ratio of SiO2 mask, high selectivity etch of Si to SiO2 Mask were achieved using “Pulsed etch”. And furthermore, this method greatly helped the suppression of ?-loading effect on Si etch depth. However, Si etch profile is likely to occur “Bowing” in case of using pulsed etch. This etch profile make a high aspect ratio locally. Multi-step and/or Cycle etch has studied to decrease Si side etching. Si side etching was greatly reduced by inserting a deposition step or oxidation step in the middle of Si etch step.

As another example, we report to the hole etch process. In hole etch process, CD shrink process after Lithography patterning is necessary to achieve target CD. Hole CD shrink process was studied using In-situ plasma etch treatment in same chamber before hole etch step. Good uniformity CD shrink process was achieved by optimized CH4 gas based plasma etch treatment before hole etch.

9428-7, Session 2

Self-limited light ion implantation for nitride spacer etching

Nicolas Posseme, Olivier Pollet, Fabrice Nemouchi, Sébastien Barnola, CEA-LETI (France)

Today, the silicon nitride spacer etching is considered as one of the most challenging step in the high performance FDSOI devices realization. A trade-off has to be found between silicon germanium (or silicon) recess, foot formation and nitride spacer faceting on top of the hard mask directly impacting the device performances.

Lowering electron temperature (low Te) or pulsing the plasma (synchronized or bias) are proposed today as solutions, presenting different advantages and drawbacks.

In a recent study, we proposed a new etch approach to overcome these issues and meet the highly complex requirements imposed by device fabrication processes. This new etching process is based on a Self-Limited Light Ion Implantation by plasma. In a first step, the film is modified in volume by a H2 plasma performed in a conventional etch tool (ICP or RIE) followed in a second step by a 1%HF wet cleaning with respect to remove the modified layer selectively to the non-modified material. Using this new etch process, the silicon germanium recess was estimated to less than 6A with no foot formation, while a silicon germanium has grown by epitaxy without defect.

In this study, we propose to evaluate a dry etch approach to remove the modified silicon nitride film selectively to non-modified nitride and silicon germanium. By playing on plasma operating conditions, the dry etch approach provides infinite selectivity between modified silicon nitride and non-modified film (compared to a selectivity of 40 using 1% HF dip). The etch mechanisms to remove the modified layer by dry etch process will be understood thanks to XPS and infrared spectroscopy analyses. The compatibility of the dry etch process to remove the modified layer with the different integration steps (wet cleaning, epitaxy) will also be presented.

9428-8, Session 3

Patterning in the era of atomic scale fidelity *(Invited Paper)*

Thorsten B. Lill, Lam Research Corp. (United States)

Sub 10 nm devices will require atomic scale fidelity. Process technologies have to replicate the design intend on a scale that is commensurate with the lattice spacing of the materials to be processed.

In this presentation, we will focus on the unprecedented requirements to control the physical and chemical environment during plasma etch patterning. Novel approaches will be presented to achieve the desired level of performance and to be able to respond to incoming variations.

9428-9, Session 3

Plasma etch challenges with new EUV lithography material introduction for patterning for MOL and BEOL

Phillip A. Friddle, Changwoo Lee, Bhaskar Nagabhirava, Michael Goss, Stafan Schmitz, Peng Wang, Richard Yang, Jian Wu, Lam Research Corp. (United States); Yann Mignot, Nouradine Rassoul, Bassem Hamieh, STMicroelectronics (United States); Genevieve Beique, Andre Labonte, Catherine Labelle, GLOBALFOUNDRIES Inc. (United States); John C. Arnold, IBM Corp. (United States)

As feature critical dimension (CD) shrinks towards and beyond the 7 nm node, newly developed patterning techniques for optical lithography with double and triple exposure will be replaced by EUV patterning. EUV enables process and overlay improvement, as well as a potential cost reduction due to fewer wafer passes and masks required for patterning. However, the EUV lithography technique introduces newer types of resists that are thinner and softer compared to conventional 193nm resists currently being used. The main challenge is to find the key etch process knobs to improve the EUV resist selectivity, line edge roughness (LER), and line width roughness (LWR), minimize line end shrink, improve tip-to2-tip degradation, and avoid line wiggling while still being able to potentially use previous schemes such as trench-first-metal-hard-mask (TFMHM), self-aligned via (SAV) and self-aligned contact (SAC). These requirements are often conflicting, especially within a patterning scheme that requires self-aligned vias, where the desired high selectivity to the hard mask conflicts with the need to minimize the hard mask thickness in order to decrease aspect ratio.

In this paper, we will discuss some of the approaches that we have investigated to define the best etch knobs controls to enable EUV patterning. RF pulsing is identified as a key feature to one of the key parameters utilized to overcome most of the previously described challenges, along with some stack optimization. This study will focus on RF pulsing (high vs. low frequency results) and bias control (RF frequency dependence). In particular, pulsing effects on resist morphology, selectivity and profile management will be reported, as well as the role of aspect ratio and etch chemistry on organic mask wiggling and collapse.

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

Conference 9428:
Advanced Etch Technology for Nanopatterning IV

9428-10, Session 3

Spectral analysis of the line-width and line-edge roughness transfer during self-aligned double patterning approach

Erwine Pargon, Emmanuel Dupuy, CNRS-LTM (France); Marc Fouchier, LTM CNRS (France); Jonathan Pradelles, Helen Grampeix, Patricia Pimenta Barros, Sébastien Barnola, CEA-LETI (France); Maxime Darnon, Olivier Joubert, LTM CNRS (France)

For further semiconductor scaling, double patterning technology has emerged as the mainstream technique for bridging the technology gap between 193nm immersion and next generation lithography (NGL). Especially, Self-aligned spacer Double Patterning (SADP) has been adopted in High Volume Manufacturing of memory devices [1], and extending its application to logic devices is seen as a major turning point in downscaling.

The SADP concept [2], [3] proposes to double the pattern density by using subsequent lithography, deposition and plasma etching steps: a conformal spacer is deposited on a core pattern, then the spacer material deposited on top and bottom of the core material is etched back, and the core is removed, leaving only the sidewalls. Finally, the remaining sidewalls (named spacer patterns) are transferred into the hardmask and active layers (cf. Figure 1).

At the same time, linewidth/ linedge roughness (LWR/LER) remains a major issue in advancing downscaling and a revolution is needed in reducing them below 2 nm for the next sub-20 nm nodes. Minimizing LER at this nanometer scale thus requires an accurate and insightful characterization of the sidewall roughness.

In this work, SADP approach has been optimised to pattern 20-nm half-pitch silicon features from 40nm half-pitch lithography, using the resist pattern as the core material and SiO2 deposited by PEALD at low temperature as spacer material and, Si-ARC/Spin on carbon/Si bulk as a stack. (cf. Figure 1). For each technological steps involved in the SADP approach, LWR and LER have been finely characterized and evaluated using power spectral density (PSD) analysis.

The results show that the LWR of the final silicon patterns could be drastically decreased of more than 64% compared to the initial resist pattern lithography, resulting in final LWR of 2.3 nm (cf. Figure 2a). PSD analyses show that most of the low frequency roughness components present after the lithography step can be erased once the spacer patterns are formed (cf. Figure 2b). This is explained by the conformal spacer formation technology that should ideally lead to zero LWR. Concerning the LER, only a 53% of LER decrease is obtained in the silicon patterns (cf. Figure 2c). The first source of decrease is the resist trimming processing step that smoothes mostly the high frequency roughness components. Although the sidewalls of the deposition inherits the shape of the sidewalls of the resist after trimming (because of the conformal deposition), a slight LER decrease is observed after deposition still in the high frequency roughness region. Once the spacer are formed, a further 20% LER decrease is obtained, mainly in the mid frequency region. Indeed, it has been shown that plasma etching processes do not transfer high-mid frequency roughness components and can thus result in LER smoothening [5]. To conclude, LWR values matching with the LWR requirements for sub-20nm technological node can be obtained using SADP technology thanks to the conformal deposition step, while effort must be made to reach the LER specifications. For instance, cure treatments could be implemented to decrease the LER of the resist pattern before deposition.

9428-11, Session 3

Ar and H2 plasma and neutral/ion-beam treatment of EUV resist

Peter De Schepper, IMEC (Belgium) and Katholieke Univ. Leuven (Belgium); Daniil Marinov, The Open Univ. (United Kingdom); Ziad el Otell, Efrain Altamirano-Sánchez, Jean-François G. N. de Marneffe, IMEC (Belgium); Stefan De Gendt, IMEC (Belgium) and Katholieke Univ. Leuven (Belgium); Nicholas St. J. Braithwaite, The Open Univ. (United Kingdom)

To meet the demands for sub-20 nm feature devices in the semiconductor industry, minimizing the line width roughness (LWR) is a critical concern for ultra-large scale integrated circuit manufacturing. Postlithography treatments should reduce the LWR by at least 50 % to meet the technology requirements, but the available postlithography strategies come short. An in depth understanding of the interaction of such postlithography treatments with EUV resists is required; especially that plasmas are known to modify the chemical and structural properties of 248nm and 193nm photoresist. A more fundamental research is needed to determine the key-contributors of this LWR convergence. In order to shed more light on the complex plasma-polymer relation, the separate impact of species from the plasma must be studied.

This paper shows the evolution of the roughness of 32 nm lines exposed to an Ar and H2 plasmas produced in an ICP reactor. In addition, to segregate the influence of various plasma species, a stainless steel mesh and carbon disk were subsequently introduced (figure 1) to expose the EUV substrates to an Ar or H2 ion beam (IB) or energetic neutral beam (NB). The use of the perforated carbon disk also shields the substrate from plasma VUV exposure. The exposed EUV samples were generated with the state of the art ASML NXE: 3100 scanner and were evaluated through cross sectional scanning electron microscopy.

Similarly, blanket EUV resist substrates were exposed to various Ar and H2 process conditions to study the chemical/structural evolution of the resists under these treatments. These experiments present a comprehensive study of surface and bulk induced modifications using spectroscopic ellipsometry (SE), atomic force microscopy (AFM), Fourier-transformed infrared spectroscopy (FTIR), Raman spectroscopy, and x-ray photoelectron spectroscopy (XPS) to link these chemical changes to the evolution of LWR.

Preliminary results confirm the importance of the VUV radiation and its positive effect on roughness. Hydrogen ion impact also has a significant influence on chemical modifications (figure 2). On the other hand, none of the results showed the formation of a highly densified top surface layer, even though ions with an energy of about 130 eV were used. This suggests that only resist bulk modifications occur. The experimental results in this work provide new insight into the understanding of LWR-evolution.

We acknowledge support from the European Union under Grant Agreement No. 318804 (SNM).

9428-12, Session 4

DSA patterning for sub-10nm nodes: integration and etch challenges *(Invited Paper)*

Patricia Pimenta Barros, Aurélien Sarrazin, Nicolas Posseme, Sébastien Barnola, Guillaume Claveau, Raluca Tiron, Ahmed Gharbi, Sandra Bos, Maxime Argoud, Isabelle Servin, CEA-LETI (France); Xavier Chevalier, MINATEC (France); Christophe Navarro, Célia Nicolet, Arkema S.A. (France); Céline Lapeyre, Commissariat à l'Énergie Atomique (France); Cedric Monget, STMicroelectronics (France)

The optical limitations of conventional lithography lead to investigate other patterning techniques for the sub-10nm nodes. Among the different approaches explored, Directed Self-Assembly (DSA) of Block Copolymers (BCP) is one of the most promising solutions due to its simplicity and its low manufacturing costs [1]. This approach has already demonstrated the possibility to generate 12.5nm dense line/space [2], to shrink pre-defined contact holes or to generate contact multiplication with high resolution holes (~15nm) [3].

Conference 9428:
Advanced Etch Technology for Nanopatterning IV

However, some challenges concerning materials development, design and integration need to be addressed for a complete adoption of DSA in CMOS manufacturing. In this paper, we will focus on the integration and etch challenges to overcome for the implementation of PS-b-PMMA block copolymer in sub-10nm devices patterning. Using the 300mm pilot line available in LETI and Arkema's materials, our approach is based on a graphoepitaxy technique. After the BCP self-assembly inside guiding patterns and a selective PMMA removal, the PS patterns are transferred into an organic, metallic or dielectric hard mask depending on the targeted application.

One challenge of DSA integration is the PMMA removal selectively to PS. Dry etching is mandatory at this step for line application since wet development is prohibited with the risk of pattern collapse. In this work, we propose to study PMMA block plasma etching with a high selectivity over PS using oxidizing and reducing chemistries, in a CCP etching chamber. First, a screening of these chemistries has been performed on PS and PMMA films showing that CO based chemistry is the most interesting process providing infinite selectivity to PS. Then, the compatibility of these chemistries has been validated in term of etch rate, CD control, etch profile and PS consumption on PS-b-PMMA films. In this study, we have demonstrated the potential of a full dry PMMA removal for both cylindrical and lamellar PS-b-PMMA copolymers and compared this approach to wet developments (figure1).

Then, the transfer of DSA patterns will be discussed in terms of CD control, pattern fidelity and PS film thickness to achieve good etching performances. During this transfer, the etching of brush layer through the PS mask is the most crucial step due to its low selectivity and its short process time. Different strategies for brush layer etching will be discussed to minimize the impact of this step on PS patterns.

Finally, DSA performances as function of guiding patterns density are also investigated (figure 2). Thus, for the best integration approach, defect-free isolated and dense patterns are demonstrated on the same processed wafer. For contact-hole applications, the hole open yield and CD uniformity have been measured in order to study and classify the defects occurred during transfer. The DSA integration flow for via patterning has been investigated from the lithography step to the via metallization step.

We succeeded in achieving 26nm DSA hole patterns transferred into a metallic underlayer with a hole open yield of 100% using an optimized etch process. These results show that DSA patterning is well compatible and promising for advanced CMOS technology.

9428-13, Session 4

Integration of NAND flash memory ISO multilayer etching to improve productivity *(Invited Paper)*

Chang-kwon Oh, SK Hynix, Inc. (Korea, Republic of)

The process integration of this research is to improve cost competitiveness and productivity.

Generally, ISO HM, ISO POLY, and ISO STI are etched separately but the number of those processing steps could be reduced to one step by integration with preservation of those profiles and device properties.

9428-14, Session 4

Trench and hole patterning with EUV resists using dual frequency capacitively coupled plasma (CCP)

Yannick Feurprier, Katie Lutker-Lee, Vinayak Rastogi, Hiroie Matsumoto, Yuki Chiba, Andrew W. Metz, Kaushik Kumar, TEL Technology Ctr., America, LLC (United States); Genevieve Beique, Andre P. Labonte, Cathy Labelle, GLOBALFOUNDRIES Inc. (United States); Yann Mignot, Bassem Hamieh, STMicroelectronics (United States); John Arnold, IBM Corp. (United States)

Patterning at 10 nm and sub-10 nm technology nodes is one of the key challenges for the semiconductor industry. Several patterning techniques are under investigation to enable the aggressive pitch requirements demanded by the logic technologies. EUV based patterning is being considered as a serious candidate for the sub-10nm nodes. As has been widely published, a new technology like EUV has its share of challenges. One of the main concerns with EUV resists are that it tends to have a lower etch selectivity and worse LER/LWR than traditional 193nm resists. Consequently the characteristics of the dry etching process play an increasingly important role in defining the outcome of the patterning process.

In this paper, we will demonstrate the role of the dual-frequency capacitively coupled plasma (CCP) in the EUV patterning process with regards to improving LER/LWR, resist selectivity and CD tunability for holes and line patterns. One of the key knobs that have been utilized for improving LER and LWR has involved superimposing a negative DC voltage in RF plasma at one of the electrodes. The emission of ballistic electrons, in concert with the plasma chemistry, has shown to improve LER and LWR. Results from this study along with traditional plasma curing methods will be presented. In addition to this challenge, it is important to understand the parameters needed to influence CD tunability and improve resist selectivity. Data will be presented from a systematic study that shows the role of various plasma etch parameters that influence the key patterning metrics of CD, resist selectivity and LER/LWR.

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

9428-15, Session 4

Challenges and mitigation strategies for resist trim etch in resist-mandrel based SAQP integration scheme

Nihar Mohanty, Akiteru Ko, Kaushik Kumar, Peter Biolsi, Jefferey T. Smith, David O'Meara, Steven A. Scheer, Anton Devillers, TEL Technology Ctr., America, LLC (United States)

Patterning the desired narrow pitch at 10 nm technology node and beyond, necessitates employment of either extreme ultra violet (EUV) lithography or multi-patterning solutions based on 193 nm immersion-lithography. With enormous challenges being faced in getting EUV lithography ready for production, multi-patterning solutions that leverage the already installed base of 193 nm immersion-lithography are poised to become the industry norm for 10 and 7 nm technology nodes. For patterning sub-40 nm pitch line/space features, self-aligned quadruple patterning (SAQP) with resist pattern as the first mandrel shows significant cost as well as design benefit, as compared to EUV lithography or other multi-patterning techniques. One of the most critical steps in this patterning scheme is the resist mandrel definition step which involves trimming / reformation of resist profile via plasma etch for achieving appropriate pitch after the final pattern. Being the first mandrel, the requirements for the Line Edge Roughness (LER) / Line Width Roughness (LWR); critical dimension uniformity (CDU); and profile in 3-dimensions for the resist trim / reformation etch is extremely aggressive.

In this paper we highlight the unique challenges associated in developing resist trim / reformation plasma etch process for SAQP integration scheme and summarize our efforts in optimizing the trim etch chemistries, process steps and plasma etch parameters for meeting the mandrel definition targets. We will also demonstrate how the type of resist material impacts the choice of appropriate plasma etch chemistry and plasma parameter space in order to achieve desired resist profiles. Finally, we will show successful patterning of 30 nm pitch patterns via the resist-mandrel SAQP scheme and its implementation for Si-fin formation at 7nm node.

9428-16, Session 5

Photoresist performance modification through plasma treatment *(Invited Paper)*

Hidetami Yaegashi, Tokyo Electron Ltd. (Japan); Kenichi Oyama, Shohei Yamauchi, Arisa Hara, Sakurako Natori, Masatoshi Yamato, Noriaki Okabe, Tokyo Electron AT Ltd. (Japan)

For the fabrication of Single directional layout, any related process tools, such as Lithography, Etching, Deposition and Cleaning have to be harmonized smartly, and patterning capability also will be needed to observe from lithographic viewpoints. Especially, pattern fidelity on mandrel pattern in SAMP might be controlled precisely. One of important process step to maintain pattern fidelity is LER suppression on resist pattern and improvement pattern transfer fidelity through RIE, because any pattern performance transfer to pitch split secondary spacer pattern.

In this paper, we will introduce the experimental demonstration results of resist smoothing utilizing plasma treatment with comparison to other technique, and explain the importance of pattern fidelity control in Multi-patterning.

9428-17, Session 5

Finding practical solution to create phenomenological models that include both photoresist behavior and the etch process effect

Sunwook Jung, Mentor Korea Co., Ltd. (Korea, Republic of); Thuy Do, John Sturtevant, Mentor Graphics Corp. (United States)

For more than 5 decades, the Semiconductor industry has overcome technology challenges with innovative ideas that have continued to enable Moore's Law. It is clear that multi-patterning lithography is vital for 20nm half pitch using 193i. Multipatterning exposure sequences and pattern multiplication processes can create complicated tolerance accounting due to the variability of the component processes.

Predicting etch bias through etch compact model had been introduced and is well established as a fullchip solution into OPC/RET community for nearly a decade. However, recent challenges have lead us to re-exam the tolerance requirement to manage not only for early stage process development but also for production support. Recent studies on 3D structural influence into accuracy of lithography model have also explored the resist domain and this provides us the possible translation of resist profile from fullchip domain. It is essential to increase the predictive accuracy of etch models and this is a precursor to integrating lithography and etch models especially for muti-patterning.

9428-18, Session 5

Molecular glass resist performance for nano-pattern transfer

Ziad el Otell, IMEC (Belgium); Andreas Ringk, Tristan Kolb, Christian Neuber, Univ. Bayreuth (Germany); Jean-François de Marneffe, IMEC (Belgium)

The requirements of the N7 node are sub-20 nm lines and spaces, with pitch typically of 36 nm. Current optical lithographic techniques (EUV/DUV) cannot deliver directly such dimensions. Specific approaches to achieve sub-20 nm dimensions, currently promoted by VLSI industry, do include alternating litho-etch steps ((LE)x), directed self-assembly (DSA), self-aligned double and quadruple patterning (SADP / SAQP). In addition to that, the performance of the most novel resists post-litho exposure show a deterioration in the line edge/width roughness (LER/LWR). Such deterioration can be tackled by soft plasma post-litho treatments, however, even with the best known plasma treatment the LER/LWR does not fulfill technology requirements.

Alternative resist patterning techniques, mainly thermal Scanning Probe Lithography (tSPL) and Scanning Proximal Probe Lithography (SPPL), have been used to achieve 27 nm line features and are being optimized to achieve sub-10 nm dimensions. Probe Lithography is typically an AFM based patterning technique, which uses heated tips or a focused current beam to locally evaporate organic resists such as molecular glasses or thermally sensitive polymers. Specific molecular glass resists need to be tailored for tSPL/SPPL patterning but also they must be compatible with plasma pattern transfer requirements, in terms of etch resistance and roughness formation.

Molecular glass resists are low molecular-weight organic compounds that readily form stable amorphous glasses and show glass transitions usually associated with polymers. Several molecular glasses based on star-shaped molecules, calixarene derivatives, dendrimers, polyphenols, and cholates have been applied as resist materials. One of the advantages of molecular glass resists compared to photoresists currently used in industry is that they are much smaller in molecular size which has the potential to generate sub-10 nm features. Another advantage of these molecular glass resists is that they do not suffer from intermolecular chain entanglement like polymers that can lead to internal stress or swelling and pattern distortion.

The aim of this article is to assess the reliability of novel molecular glass resists, deposited mainly by physical vapor deposition (PVD), and their compatibility with plasma etching for the purpose of nano-patterning. Spectroscopic ellipsometry (SE), atomic force microscopy (AFM), and x-ray photoelectron spectroscopy (XPS) measurements were performed to determine etch rates, the evolution of the surface roughness, and the effect of plasma exposure on the chemical and structural composition of the resist.

Experiments were performed in a CCP chamber using CF4 and Ar plasmas to benchmark the resist performance. The first set of experiments was performed on a series of blanket samples UBTx (x=1 to 14) to further understand the plasma-polymer complex relation. Most recent experiments were performed on a mélange with different ratios of UBT8 and UBT14 and annealed resists to enhance the surface roughness properties and etch resistance. The second set of experiments was performed on patterned samples with line widths ranging from 75 down to 25 nm.

9428-19, Session 6

Investigation of line roughness and undulation during DSA pattern transfer for BEOL applications

Erik R. Hosler, Xunyuan Zhang, Genevieve Beique, Moshe E. Preil, Cathy Labelle, E. Todd Ryan, GLOBALFOUNDRIES Inc. (United States); Vinayak Rastogi, Yannick Feurprier, TEL Technology Ctr., America, LLC (United States); Richard A. Farrell, Tokyo Electron America, Inc. (United States); Kai-Hung Yu, Tokyo Electron Amierca, Inc. (United States); Richard Gaylord, Tokyo Electron America, Inc. (United States); Nihar Mohanty, David Hetzer, Kaushik Kumar, Akitero Ko, TEL Technology Ctr., America, LLC (United States)

Interconnect RC scaling is a critical part of overall product performance. Introducing low-k (ULK) nanoporous materials is necessary to mitigate capacitance, however, these materials pose integration challenges, especially at 28 nm pitch and smaller. For example, they are subject to pattern undulations (line wiggling) during wet clean drying, which may become a critical component to the overall pattern roughness. The risk of pattern undulations increases if the aspect ratio of the Cu line is increased to alleviate high resistivity. Void free Cu fill and maintaining a bamboo-like microstructure is also necessary for interconnect resistance and reliability, possibly requiring non-conventional metallization.

Should Mx (x = 0, 1, 2, etc...) be converted to unidirectional layout at a single pitch, directed self-assembly (DSA) would offer a greatly simplified alternative to high-order multipatterning techniques. However, two primary concerns regarding implementation of DSA patterning in high-volume manufacturing involve defectivity and pattern roughness. Furthermore, DSA pattern transfer into soft ULK materials poses additional challenges to pattern roughness control, and may require roughness optimization beyond the DSA guide pattern lithography; including both etch transfer and possibly wet clean optimization.

A chemoepitaxy polystyrene poly(methyl methacrylate) (PS-PMMA) DSA process flow is employed to pattern 28 nmP line/space features, which are subsequently etched into a BEOL dielectric stack. The critical feature short-range (line-width, line-edge, and spacer-width) roughness is quantified throughout the pattern transfer process to evaluate the etches' role on roughness evolution. Contribution of longer-range line undulation on pattern roughness is also evaluated by varying the dielectric trench aspect ratio and k-value (k = 2.7, 2.55, and 2.4); lower-k films having a lower modulus and greater risk of undulation. Lastly, the etched dielectric patterns were metallized and polished to form copper-filled interconnects.

9428-28, Session PS1

Magnetic VHF plasma etching process for high-aspect ratio Si structure

Taku Iwase, Hitachi, Ltd. (Japan); Takao Arase, Akira Hirata, Kenetsu Yokogawa, Masahito Mori, Hitachi High-Technologies Corp. (Japan)

Integration of semiconductor device for the next generation node of logic and memory presents a lot of challenges to an etching process; especially current planar type flash memory device is facing the critical scaling limitation. So 3D-NAND device architecture has been boosted in manufacturing fab for flash memory market by perpendicular integration [1]. The high aspect ratio (HAR) etching technology is a key factor for 3D-NAND fabrication. Current requirement of HAR structure is hole and trench of more than 20:1 aspect ratio with less than several tens nm of pitch stacked by poly-Si single film or laminated film containing poly-Si, SiO2 and SiN.

Shortage of selectivity and profile deterioration such as bowing and twisting has emerged from HAR etching studies. In general, pressure and bias power is especially important process parameter. High pressure and low bias power are effective on selectivity for low aspect region. On the other hand, low pressure and high bias power are effective on vertical profile for high aspect region. Therefore a new concept etching tool that has a wider process window is required, for example having an ion energy range from a few to several thousands eV and also the pressure range from sub-Pa to tens Pa.

In this study, a magnetic VHF plasma etching system was developed. The reactor consists of a parallel-plate type plasma. Plasma was generated by the interaction between the magnetic field of the solenoid coils and the VHF power supplied to the upper electrode. The distribution of ions and radicals that impinge on the wafer was controlled by the magnetic field control [2]. This magnetic VHF plasma reactor has achieved a precise and stable etching process in advanced wider pressures range. A bias power was applied to control the ion energy toward the wafer stage by wider ion energy range. The effectiveness of the magnetic VHF plasma in the 3D-NAND etching process was evaluated.

A gas inlet under the upper electrode in the reactor was made of dielectric material to etch poly-Si using Cl2 or HBr gas. Etch-rate uniformity was evaluated using blanket wafers deposited with poly-Si or SiO2 on a Si substrate. Bias power and pressure were changed independently with controlling magnetic field to confirm the process window. 50nm diameter holes were then formed on an amorphous carbon mask by EB lithography to demonstrate HAR etching. 8 pairs of poly-Si and SiO2 stacked film was etched using the amorphous carbon mask.

It was found that etch-rate distribution poly-Si and SiO2 can be controlled from concave to convex by adjusting the magnetic field strength. Less than ±3% etch-rate uniformity of poly-Si was obtained in a 0.4 ~ 12 Pa pressure range and a 50 ~ 4000 W bias power range. Furthermore, we fabricated 24:1 aspect ratio holes in a film stacked poly-Si and SiO2 alternately. The vertical profile and the high selectivity were obtained by wide range pressure and bias control depending on aspect ratio.

References

[1] H. Tanaka et al., Symposium on VLSI Tech. Dig., pp. 14-15 (2007).

[2] K. Yokogawa, et al., Jpn. J. Appl. Phys., 47, pp. 6854-6857 (2008).

9428-29, Session PS1

Direct comparison of the performance of commonly used e-beam resists during nano-scale plasma etching of Si, SiO2, and Cr

Andy L. Goodyear, Oxford Instruments (United Kingdom); Monika Boettcher, Ines A. Stolberg, Vistec Electron Beam GmbH (Germany); Mike Cooke, Oxford Instruments (United Kingdom)

Electron beam writing remains one of the reference pattern generation techniques, and plasma etching continues to underpin pattern transfer. We report a systematic study of the plasma etch resistance of several e-beam resists, both negative and positive as well as classical and Chemically Amplified Resists: HSQ (Dow Corning), PMMA (Allresist GmbH), AR-P6200 (Allresist GmbH), ZEP520 (Zeon Corporation), CAN028 (TOK), CAP164 (TOK), and an additional pCAR (non-disclosed provider).

Their behaviour under plasma exposure to various nano-scale plasma etch chemistries was examined (SF6/C4F8 ICP silicon etch, CHF3/Ar RIE SiO2 etch, Cl2/O2 RIE and ICP chrome etch, and HBr ICP silicon etch). Samples of each resist type were etched simultaneously to provide a direct comparison of their etch resistance. Resist thicknesses (and hence resist erosion rates) were measured by spectroscopic ellipsometer in order to provide the highest accuracy for the resist comparison.

Etch selectivities (substrate:mask etch rate ratio) are given, with recommendations for the optimum resist choice for each type of etch chemistry. Silicon etch profiles are also presented, along with the exposure and etch conditions to obtain the most vertical nano-scale pattern transfer. We identify one resist that gave an unusually high selectivity for chlorinated and brominated etches which could enable pattern transfer below 10nm without an additional hard mask. In this case the resist itself acts as a hard mask. We also highlight the differing effects of fluorine and bromine-based Silicon etch chemistries on resist profile evolution and hence etch fidelity.

9428-30, Session PS1

Challenges of contact etching for 14nm FDSOI technology

Mokrane Mebarki, STMicroelectronics (France) and Univ. de Grenoble (France) and LTM CNRS (France); Maxime Darnon, LTM CNRS (France) and Univ. de Grenoble (France); Cécile Jenny, Delia Ristoiu, STMicroelectronics (France); Nicolas Posseme, CEA-LETI (France); Olivier Joubert, LTM CNRS (France) and Univ. de Grenoble (France)

The reduction of device dimension at the sub 20 nm node requires the introduction of double patterning for contact etching. Line and space patterns are defined first in a thin TiN layer. Then, a trilayer stack with Si-containing anti reflection coating (SiARC) and organic planarizing layer (OPL) is used to define open areas The mask is defined by the intersections of both hard mask of TiN and OPL patterns and is used to etch contacts into silicon oxide (TEOS).This architecture leads to new challenges due to the integration of double patterning and TiN hard mask as compared to previous technology.

The OPL mask must conserve straight profiles during the different etching

steps and TiN is exposed to the plasma during silicon oxide etching (cf Fig 2). It is known that the OPL can be etched by different plasmas (N2/H2, O2/SO2, O2/CO2) that may induce a passivation layer on the sidewalls via different passivation elements such has CN, CS, CO [1]. Such passivation layers as well as the presence of TiN during contact etching can interfere with the following SiO2 etching process and change the final pattern profile.

In this paper, we investigated OPL mask etching with a COS/O2 plasma in comparison with a N2/H2-based etching process. We show that the profile of the SiO2 contact hole is influenced by the OPL etch process and its interaction with TiN hard mask. These interactions modify the shape of TiN hard mask impacting the contact profile into the SiO2 (cf Fig 3). The degradation of masks profiles leads to Ti or S containing residues formation which tends to block the SiO2 etching (cf Fig 4). To characterize these interactions we performed XPS analyses on TiN, OPL and TEOS after exposure to the various OPL etching processes (cf Fig 5). We show that these effects can be reduced by increasing COS/O2 ratio during OPL etching.

9428-31, Session PS1

A way to integrate multiple block layers for middle of line contact patterning

Eddy Kunnen, Steven Demuynck, IMEC (Belgium); Mohand Brouri, Lam Research Corp. (Belgium); Jürgen Bömmels, Janko Versluijs, Julien Ryckaert, IMEC (Belgium)

It is clear today that further scaling towards smaller dimensions and pitches requires a multitude of additional process steps. Within this work we look for solutions to achieve a middle of line 193i based patterning scheme for N7 logic at a contacted poly pitch of 40-45 nm. At these pitches trenches can still be printed by means of double patterning, however, they need to be blocked at certain positions because of a limited line end control below 90 nm pitch single print. Based on the 193i patterning abilities, the proposed SRAM cell requires 5 blocking layers. Integrating 5 blocking layers is a new challenge since down to N10 one blocking layer was usually sufficient. The difficulty with multiple blocking layers is removal of the masked parts, especially in cases of overlap. As a solution a novel patterning approach is proposed and tried out on relaxed dimensions (patent pending). The proposed solution is expected not to be sensitive to the number of blocking layers used and avoids masking of overlapped areas. The stack is constructed to be compatible with N7 substrates such as SiGe or P:Si. Experimental results of the stack blocking performance on relaxed pitch will be presented and discussed.

9428-33, Session PS1

Synchronous pulsing plasma utilization in dummy poly gate removal process

Ruixuan Huang, XiaoYing Meng, QiuHua Han, HaiYang Zhang, Semiconductor Manufacturing International Corp. (China)

When CMOS technology reaches 28/20nm node and beyond, several new schemes are implemented such as High K metal gate (HKMG) which can enhance the device performance and has better control of device current leakage. Dummy poly gate removal (DPGR) process is introduced for HKMG, and works as a key process to control the work function of metal gate and threshold voltage (Vt) shift.

In dry etch technology, conventional continuous wave (CW) plasma process has been widely used, however, it may not be capable for some challenging process in 28nm node and beyond. In DPGR process for HKMG scheme, CW scheme may result in plasma damage of gate oxide/capping layer for its inherent high electron temperature (Te) and ion energy while synchronous pulsing scheme is capable to simultaneously pulse both source and bias power, which could achieve lower Te, independent control of ion and radical flux, well control the loading of polymer deposition on dense/ isolate features. It's the first attempt to utilize synchronous pulsing plasma in DPGR process. Experiment results indicate that synchronous pulsing could provide less silicon recess under thin gate oxide which is induced by the plasma oxidation. Furthermore, the loading of HK capping layer loss between long channel and short channel can be well controlled which plays a key role on transistor performance, such as leakage and threshold voltage shift. Additionally, it has been found that synchronous pulsing could distinctly improve ILD loss when compared with CW, which is helpful to broaden the whole process window

9428-34, Session PS1

Characterization of the effect of etch process operating environment on the perfluoroelastomer chamber seal systems

Barry Kitazumi, Greene, Tweed & Co. Inc. (United States); Gary Reichl, Greene, Tweed & Co. (United States)

IDMs, Foundries and Equipment Manufacturers face significant challenges as they scale to smaller feature sizes and integrate novel architectures and materials into semiconductor wafer manufacturing. As their race accelerates to develop breakthrough architectures and integration schemes to stay on pace with the industry roadmap and end markets, there is additional pressure on the balance of the supply chain to maintain the pace of needed innovation.

The transition from planar to vertical architectures, and integration of selective material processes, necessitates changes in plasma etch processing power, pressure, energy and gas combinations. Combinations of power, pressure, energy and gases result in drastically different o-ring erosion rates and behaviors.

This poster session reviews a fundamental study and test methodology to assess how power, pressure, energy and gases impact o-ring erosion. The objective is to develop correlations for chemical composition of o-rings and performance in representative fab tools and conditions typical of advanced plasma etch processes. Characterization of control and study samples includes plasma resistance measured as weight loss and surface morphology change after process exposure.

Exploring the effect of only Argon plasma provides a simple demonstration of interactions and inter-dependence of chemical composition of an o-ring and performance within the plasma etch environment. Figure 1 illustrates 7 control samples representing different chemical compositions, polymer and formulation technologies. The results indicate that chemical composition of an o-ring does affect characteristics like plasma resistance, measured as weight loss, and conclusions can be drawn. This fundamental study included a total of 17 recipes to assess o-ring performance, and enhance cycles of learning to characterize and optimize o-ring materials for advanced plasma etch technology.

Conclusions are presented that enable the research community to understand how advanced plasma etch technology process integration schemes will impact o-ring erosion behavior. The intent of this fundamental study is to deliver predictive ability while protecting intellectual property and trade secrets within the process and equipment development research community.

An unabated pace of learning is expected within the supply chain. This fundamental study demonstrates effort to progress from traditionally qualitative definition of advanced plasma etch technology at the component level, and provides a model to characterize impact to WPE defect reduction and productivity improvement in HVM.

The potential impact to MWBC, throughput and yield is significant if a sealing o-ring that used to withstand the plasma etch environment for 3 months on the previous process node, begins catastrophically failing on the next node after 1 week. The resources invested, and time and dollars lost, during root cause investigation and corrective action are significant. Delays in any part of the semiconductor supply chain compound, posing critical threats to achieving unrelenting consumer product introduction schedules.

Conference 9428:
Advanced Etch Technology for Nanopatterning IV

9428-20, Session 7

Low-damage cryoetching of low-K materials *(Invited Paper)*

Remi Dussart, Group de Recherches sur l'Energétique des Milieux Ionisés (France) and Ctr. National de la Recherche Scientifique (France) and Univ. d'Orléans (France); Thomas Tillocher, Univ. d'Orléans (France); Floriane Leroy, Philippe Lefaucheux, Group de Recherches sur l'Energétique des Milieux Ionisés (France); Koichi Yatsuda, Tokyo Electron Ltd. (Japan); Kaoru Maekawa, Tokyo Electron Ltd. (United States); Eiichi Nishimura, Tokyo Electron AT Ltd. (Japan); Liping Zhang, Jean-François G. N. de Marneffe, Mikhail R. Baklanov, IMEC (Belgium)

Cryoetching of silicon was first introduced by a Japanese team in the late 80s [1]. Standard cryoetching of silicon basically relies on a SF6/O2 plasma interacting with a silicon wafer cooled down to a low temperature of typically -100°C. At this very low temperature, a SiOxFy passivation layer forms on the silicon sidewalls avoiding lateral etching [2,3]. Cryoetching processes are usually used for deep silicon etching of micrometer scale patterns. Very high-aspect-ratio silicon microstructures can be created using a wide variety of mask materials. Recent publications showed that it can also be used to etch nanoscale features [4,5].

More recently, cryoetching was applied to interconnects in back-end-of-line (BEOL) part of advanced CMOS technology, focusing on the etching of porous organosilicate glasses (OSG) [6]. Porous OSG are important low-k candidates for advanced interconnects. Their integration is very challenging because of plasma induced damage issues. This problem can be reduced by the Post Porosity Plasma Protection (P4) technique (for instance, by sacrificial polymers [7]) because it reduces penetration of active radicals and VUV light into the film. The P4 technique by sacrificial organic polymers is interesting but has few challenges, such as its impact on several steps of the patterning and metallization and possible deformation of low-k film during the process.

The objective of our work on porous OSG cryoetching is to minimize the plasma induced carbon depletion. We defined an equivalent damaged layer (EDL) by ellipsometry and FTIR experiments, and measured the change of dielectric constant after plasma exposure. The real damage layer was also evaluated by TOF SIMS and TEM. Etching experiments were performed on patterned and blanket wafers. In porous OSG low-k materials, pores can be filled with the introduced chemicals and/or etch by-products so that plasma-induced damage is significantly reduced. Although the passivation layer evaporates at ambient temperature, condensate by-products (carboxylic acids) remain stable at room temperature. However, this condensate can be removed easily by high-temperature annealing without additional damage to the low-k materials.

Cryoetching of organosilicate low-k materials appears as a very promising etching process for BEOL interconnects.

[1] Tachi S et al. Appl. Phys. Lett. 52 616 (1988)

[2] X. Mellhaoui et al. J. Appl. Phys., 98, 104901 (2005)

[3] R Dussart et al. J. Phys. D: Appl. Phys. 47 123001 (2014)

[4] Gu X et al. Adv. Mater. 24 5688 (2012)

[5] Liu Z et al. Nanotechnology 24 015305 (2013)

[6] L. Zhang et al, ECS Journal of Solid State Science and Technology, 2 (6) N131-N139 (2013)

[7] T. Frot et al. Adv. Funct. Mater., 22, 14, 3043 (2012)

9428-21, Session 7

Low-temperature and damage-free transition metal and magnetic material etching using a new metallic complex reaction *(Invited Paper)*

Toshihisa Nozawa, Tokyo Electron Ltd. (Japan)

No Abstract Available

9428-22, Session 7

Electron energy distribution control by Fiat: breaking from the conventional flux ratio scaling rules in etch *(Invited Paper)*

Alok Ranjan, Mingmei Wang, TEL Technology Ctr., America, LLC (United States); Peter Ventzek, Tokyo Electron America Inc. (United States)

With shrinking critical dimensions, dry etch faces more and more challenges. Minimizing each of aspect ratio dependent etching (ARDE), bowing, undercut, selectivity, and within die uniformly across a wafer is met by trading off one requirement against another. The problem of trade-offs is especially critical. At the root of the problem is that roles radical flux, ion flux and ion energy play may be both good and bad. Increasing one parameter helps meeting one requirement but hinders meeting the other. Managing process by managing flux ratios and ion energy alone with conventional sources is not adequate because surface chemistry is uncontrollable. At the root of lack of control is that the electron energy distribution function (eedf) has not been controlled.

Fortunately the high density surface wave and dc augmented-CCP sources control the eedf by fiat. High density surface wave sources are characterized by distinct plasma regions: an active plasma generation region and an ionization free but chemistry rich diffusive region. "Spatial pulsing" allows access to plasma chemistry with reasonably high ion flux, from the active plasma generation region, just above the wafer. The dc augmented-CCP sources, in contrast, employ an imposed dc bias augmented rf electrode to flood the plasma and wafer with a beam of suprathermal electrons. These electrons perform radical chemistry unavailable to electrons heated merely by VHF UHF in an either inductive or capacitive manner. Furthermore the electrons are able to interact with the wafer in a manner such that the surface chemistry renders masks more etch resistant even in the face of increasing ion flux, a usual trade-off. Both means of eedf control provide well defined impact at the feature scale. For example, feature-bottom charging is alleviated by beam of high energy electrons thereby eliminating bow and twisting.

This presentation will describe eedf control for two new classes of plasma sources. The background of the sources will be described in the context of over 20 years of source development. BEOL and FEOL process results will be used to substantiate performance principles.

9428-23, Session 7

Precise etch profile control by multistep cyclic process

Motohiro Tanaka, Hitachi High-Tech Science Corp. (Japan); Yasushi Sonoda, Yutaka Kozuma, Masahiro Sumiya, Hitachi High-Technologies Corp. (Japan); Naoki Yasui, Hitachi High-Tech Science Corp. (Japan)

Semiconductor devices have improved in their performance and integration density not only by shrinking, but also by introducing advanced technologies such as strained silicon and HKMG materials. The new 3D

transistor architecture called "FinFET" which has excellent switching performance has been introduced for high performance devices at the 22nm node and beyond. Precision etching requirements are higher than ever for FinFET in regards to etching fins at high aspect ratios, etching a vertical profiles, as well as achieving a flat etch front. Beside, as FinFET device shrink, tighter pitch and higher aspect ratio in the fin are needed. Then this shrinkage leads to severe requirements for profile control in etching to the atomic level. In order to improve the etching profile and selectivity, Time-Modulation(TM) techniques have been adopted, such as time modulated wafer bias [1] and time modulated plasma [2]. These TM techniques make it possible to control the by-product effect or the ionization and disassociation degrees of process plasma.

In this study, a time modulated multi-step cyclic process [3] in a microwave ECR plasma etching tool was evaluated as a novel technology for high precision etch profile control. This process includes several steps, which has each different property, in a repeated cycle. Each step in the cycle plays an independent role such as progression of etching and formation of passivation layer on the sidewall of etched surface, all which work together to achieve the demanded profile and selectivity. The conventional process is an optimized balance of etch and deposition in a single step. In the case of shrinking and high aspect etching, for instance fin etching process, enough etchant is needed to be delivered to the bottom of narrow pitch pattern, however, some of the etchant is consumed at the upper part of the sidewall, often resulting in side etch. Sufficient side wall protection is needed, but formation of durable and thick passivation layer often results in a tapered profile. In contrast, the effect of deposition and etching in a cyclic process can be optimized independently. Therefore, the passivation layer which has the durability and thickness matched for the impact of paired etching step can be formed, and higher etching controllability can be realized by this cyclic mechanism.

The etching properties and etching profile controllability were investigated by evaluating the post-etched simulated fin cross-sectional profile. It was found that the etching profile was able to be controlled by adjusting each step time, as the adjusted etching amount and protection effect of passivation layer by each step time was made. These results indicate the etching profile can be controlled linearly and easily. This is a great benefit compared to conventional process. By optimizing the cyclic process and its step time, the vertical profile, higher selectivity and flat etch front for future fin etching was obtained.

[1] T. Ono et al., Jpn. J. Appl. Phys. 39 (2000), p.5003

[2] M. Morimoto et al., SPIE Advanced Lithography 2014 [9054-18]

[3] K. Tsujimoto et al., Proc. Symposium on Dry Process, p.30 (IEE of Japan, Tokyo 1986).

9428-24, Session 8

Atomic layer etch *(Invited Paper)*

Olivier Joubert, LTM CNRS (France)

No Abstract Available

9428-25, Session 8

Etch aware EPE correction: the critical path toward multipatterning control *(Invited Paper)*

Kaidong Xu, IMEC (Belgium)

No Abstract Available

9428-26, Session 8

RIE challenges for sub-15nm lines and spaces patterning using directed self-assembly lithography with coordinated line epitaxy (COOL) process

Yusuke Kasahara, Yuriko Seino, Hironobu Sato, Hideki Kanai, EUVL Infrastructure Development Ctr., Inc. (Japan); Katsutoshi Kobayashi, EUVL Infrastructure Development Ctr, Inc. (Japan); Toshikatsu Tobana, Ken Miyagi, Shinya Minegishi, Naoko Kihara, Katsuyoshi Kodera, Noriyuki Hirayanagi, Tomoharu Fujiwara, EUVL Infrastructure Development Ctr., Inc. (Japan); Yoshiaki Kawamonzen, EUVL Infrastructure Development Ctr, Inc. (Japan); Tsukasa Azuma, EUVL Infrastructure Development Ctr., Inc. (Japan)

Directed self-assembly (DSA) is one of the promising candidates for next generation lithography. Several sub-15nm L/S patterning processes using polystyrene-block-poly(methyl methacrylate) (PS-b-PMMA) lamellar block copolymer (BCP) have been reported such as lift-off flow [1], LiNe flow [2,3] and SMART flow [4]. We developed a novel simple sub-15 nm lines and spaces (L/S) patterning process, "coordinated line epitaxy (COOL) process", using grapho- and chemo- hybrid epitaxy. The COOL process requires neither special pinning guide materials to control surface free energy on guide line patterns nor resist strip process after guide line patterns fabrication.

In this work, we demonstrated Reactive Ion Etching (RIE) process conditions dependence on critical dimension uniformity (CDU), pattern roughness (LER and LWR) and defects on 300 mm wafer using the COOL process. The CDU, LER, LWR and defects strongly depend on the RIE process conditions. In order to transfer DSA patterns to substrates successfully, extreme optimization of the RIE process conditions such as etching time, gas chemistry, RF power and pressure is of importance. Figure 1 shows pattern transfer processes for sub-15 nm L/S patterns. The extreme optimization of the RIE process conditions could improve the CDU, LER, LWR and defects. In the conference, results of pattern transfer to the hard mask will be also discussed.

A part of this work was funded by the New Energy and Industrial Technology Development Organization (NEDO) under the EIDEC project.

References

[1] J. Cheng, D. Sanders, H. Truong, S. Harrer, A. Friz, S. Holmes, M. Colburn, W. Hinsberg, ACS Nano. 4(8) (2010) 4815-4823.

[2] C. Liu, C. Estrada-Raygoza, H. He, M. Cicoria, V. Rastogi, N. Mohanty, H. Tsai, A. Schepis, K. Lai, R. Chao, D. Liu, M. Guillorn, J. Cantone, S. Mignot, R. Kim, J. Cheng, M. Tjio, A. Ko, D. Hetzer, M. Somervell, M. Colburn, Proc. SPIE, 9049-8 (2014)

[3] R. Gronheid, Y. Lee, Y. Cao, Y. Her, L. D'Urzo, D. Heuvel, P. Delgadillo, A. Romo-Negreira, M. Somervell, R. Harukawa, V. Nagaswami, Proc. SPIE, 9049-4 (2014)

[4] J. Kim, J. Wan, S. Miyazaki, Y. Cao, Y. Her, H. Wu, K. Kurosawa, G. Lin, J. Photopolymer Sci. and Tech. Vol. 26(5) (2013) 573-579.

9428-27, Session 8

A facile route for fabricating graphene nanoribbon array transistors using graphoepitaxy of a symmetric block copolymer

Jonathan Choi, Myungwoong Kim, Nathaniel S. Safron, Eunghak Han, Michael S. Arnold, Padma Gopalan, Univ. of Wisconsin-Madison (United States)

Conference 9428:
Advanced Etch Technology for Nanopatterning IV

Graphene nanoribbons (GNRs) with a sub-20 nm width exhibit an electronic band gap due to the quantum confinement effect, thereby emerging as a promising material for semiconducting applications. Several approaches have been used to fabricate an array of GNRs such as, electron-beam lithography, the unzipping of carbon nanotubes, surface-assisted coupling of molecular precursors into linear polyphenylenes, as well as top-down patterning using block copolymer (BCP) lithography. Most of these processes have limited technological applicability mainly due to lack of scalability and compatibility with current manufacturing processes, with the exception of BCP lithography. BCP lithography is a useful nanopatterning method to create nanostructures with high fidelity and throughput. Here, we report a facile route to form densely packed GNR arrays via homogeneous graphoepitaxial assembly of symmetric poly(styrene-block-methyl methacrylate) [P(S-b-MMA)].

In BCP lithography, graphoepitaxy refers to the use of topographic sub-micron patterns for inducing the alignment of BCP microdomains by physical confinement between the side walls in a trench. This process has been used to fabricate GNR arrays as the dimensions of topographic guiding channels are relatively easy to access with conventional photolithography or nanoimprint lithography. In the literature typically a step-wise approach is demonstrated, namely (i) patterning of graphene using graphoepitaxy of BCPs, and (ii) the fabrication of the FET device, adding to the complexity of the process. In order to avoid this complexity, we controlled the surface composition of trench bottom and side walls, i.e., the side edges of the source and the drain electrodes; then perpendicularly oriented lamellar domains of P(S-b-MMA) were aligned normal to the electrodes. By pattern transferring to the underlying graphene from the BCP template using reactive ion etching, GNR arrays were defined, providing conducting channels between the two electrodes.

Experimentally, mechanically exfoliated graphene was placed onto SiO2 substrates. The guiding channels of the graphoepitaxy act as the source and drain electrodes in a FET geometry avoiding any additional laborious nanopatterning and FET device fabrication processes. Additionally, a 10 nm buffer layer of SiO2 was thermally evaporated on top of the graphene and the source/drain to act as a wetting layer. This allowed the nonpreferential random copolymer to be grafted onto the trench bottom and sidewalls, allowing vertically oriented lamella P(S-b-MMA) to be aligned normal to the source/drain guiding channels. Through optimization of the reactive ion etching conditions of O2 and CHF3 + O2, the perpendicularly oriented lamellar domains were transferred to the underlying graphene, leading to GNR arrays that act as conducting channels with the average line width of the SiO2/graphene line arrays being 17.9 ± 1.9 nm. To investigate the device characteristics, the graphene FET device was electrically characterized at various stages of nanopatterning, confirming successful pattern transfer from BCP template to underlying graphene. Our method reduces the number of fabrication steps, leading to a facile and efficient route towards GNR array transistors.