2015 ADVANCED LITHOGRAPHY.

Call for Papers

Submit Abstracts by 8 September 2014
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San Jose Marriott and San Jose Convention Center
San Jose, California, USA

Conferences & Courses
22–26 February 2015

Exhibition
24–25 February 2015
2015 Advanced Lithography.

Present and publish your work at the world’s premier semiconductor lithography event

Call for Papers.

SPIE. ADVANCED LITHOGRAPHY

LOCATION
San Jose Marriott and
San Jose Convention Center
San Jose, California, USA

DATES
Conferences & Courses: 22–26 February 2015
Exhibition: 24–25 February 2015

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Lithography today, and even more tomorrow, is challenged with cost-effectively extending immersion patterning toward physical limits. This is being carried out using multiple-exposure and etch processes while striving to bring EUV lithography to production readiness. In parallel, the lithography community is aggressively pursuing other newer technologies, such as directed self-assembly. Success calls for unique interdisciplinary interactions, and coordinated efforts between lithographers, layout designers, materials scientists, and metrology/process control engineers to enable cost efficient patterning solutions.

For the past 39 years, SPIE Advanced Lithography has played a key role in bringing together the lithography community. The addition of other patterning-related technology over the past several years, has sought to solve the challenges presented by the continuous scaling of the semiconductor industry.

A full spectrum of lithographic and patterning technology is now present at the symposium across seven complementary conferences. Symposium participants come from a broad array of backgrounds to share and learn about state-of-the-art lithographic tools, resists, metrology, materials characterization, etch, design, and process integration. Also, through a series of provocative panel discussions and seminars, the symposium probes current issues being faced as we extend these technologies, switch to alternative technologies, or identify ways to complement one technology with another.

Over the years, SPIE Advanced Lithography has provided a unique forum for meeting and interacting with a wide-spectrum of industry experts and key industry players working on patterning technology developments.

Additional information is available from the many manufacturers’ exhibits, which allow tool makers, material and software suppliers to showcase new products while interacting one-on-one with customers.

We welcome your participation in the 40th SPIE Advanced Lithography, and urge you to submit your abstracts to the appropriate conference as described in the call for papers. Relevant topics for new technology groups or panel discussions are also solicited.

SPIE Advanced Lithography is structured into seven conferences:
- Alternative Lithographic Technologies
- Extreme Ultraviolet Lithography
- Metrology, Inspection, and Process Control for Microlithography
- Advances in Patterning Materials and Processing Technology
- Optical Microlithography
- Design-Process-Technology Co-Optimization for Manufacturability
- Advanced Etch Technology for Nanopatterning

All conferences are organized by current practitioners of the art, and numerous courses are taught by recognized industry experts.

2015 SYMPOSIUM CHAIR
Mircea V. Dusa
ASML US, Inc.

2015 SYMPOSIUM CO-CHAIR
Bruce W. Smith
Rochester Institute of Technology

Executive Committee
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Jason P. Cain, Advanced Micro Devices, Inc.
Luigi Capodieci, GLOBALFOUNDRIES Inc.
Mircea V. Dusa, ASML US, Inc.
Sebastian U. Engelmann, IBM Thomas J. Watson Research Ctr.
Andreas Erdmann, Fraunhofer Institute of Integrated Systems and Device Technology
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Kafai Lai, IBM Corp.
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Douglas J. Resnick, Canon Nanotechnologies, Inc.
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Obert R. Wood II, GLOBALFOUNDRIES Inc.

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C. Grant Willson, The Univ. of Texas at Austin
Anthony Yen, Taiwan Semiconductor Manufacturing Co., Ltd.
FRITS ZERNIKE AWARD FOR MICROLITHOGRAPHY
The Frits Zernike Award for Microlithography is given annually for outstanding accomplishments in microlithographic technology, especially those furthering the development of semiconductor lithographic imaging solutions.

Mordechai Rothchild, MIT, Lincoln Laboratory, Lexington, MA, USA, is the 2014 recipient of the Frits Zernike Award for Microlithography in recognition of his significant contributions made to the advancement of lithography through the exploration and demonstration of DUV/VUV materials, lasers, and systems.

Awards presented at the 2014 Advances in Resist Materials and Processing Technology Conference

The 2013 C. Grant Willson Best Paper Award was presented to Peter Trefonas, James W. Thackeray, Dow Electronic Materials (USA); Guorong Sun, Sangho Cho, Corrie Clark, Stanislav V. Verkhoturov, Michael J. Eller, Ang Li, Adriana Pavia-Jiménez, Emile A. Schweikert, Karen L. Wooley, Texas A&M Univ. (USA) for their paper 8682-37, Bottom-up/top-down high-resolution, high-throughput lithography using vertically assembled block brush polymers.

The 2013 Jeffrey Byers Memorial Best Poster Award was presented to Jing Jiang, Byungki Jung, Michael O. Thompson, Christopher K. Ober, Cornell Univ. (USA) for their poster 8682-58, Line edge roughness of high deprotection activation energy photoresist by using sub-millisecond post exposure bake.

The 2013 Hiroshi Ito Memorial Best Student Paper Award was presented to My-Phung Van, Cees W.M. Bastiaansen, Technische Univ. Eindhoven (Netherlands) and Queen Mary Univ. of London (United Kingdom); Dirk J. Broer, Technische Univ. Eindhoven (Netherlands), for their paper 8682-65, Selective photoresist doped with reactive liquid crystals doped with a dichroic photoinitiator.

The 2013 Hiroshi Ito Memorial Best Student Paper Award was presented to Xaver Thrun, Kang-Hoon Choi, Nobert Hanisch, Christoph K. Hohle, Katja Steidel, Fraunhofer-Ctr. Nanoelektronische Technologien (Germany); Douglas Guerrero, Brewer Science, Inc. (USA); Thiago R. Figueiro, Asela Nanographics (France); Johann W. Bartha, Technische Univ. Dresden (Germany), for their paper 8682-34, Effects on electron scattering and resist characteristics using assisting underlayers for e-beam direct write lithography.

The 2013 Diana Nysssonen Memorial Award for the Best Paper was presented to Ozan Ugurlu, Michael Strauss, Gavin Dutrow, Jeff Blackwood, Brian Routh, Corey Senowitz, Pavel Plachinda, Roger Alvis, FEI Co. (USA) for their paper 8681-6, High-volume process monitoring of FEOL 22nm FinFET structures using an automated STEM.

The 2014 Best Student Paper Award was presented to Julien Mailfert, and co-authors Peter De Bisschop, Kristin De Meyer, Jeroen Van de Kerkhof, IMEC (Belgium), for their paper 9052-25, Metal patterning study for random-logic applications with 193i, using calibrated OPC for litho and etch.

Awards presented at the 2014 Metrology, Inspection, and Process Control for Microlithography Conference

The 2013 Hiroshi Ito Memorial Best Student Paper Award was presented to My-Phung Van, Cees W.M. Bastiaansen, Technische Univ. Eindhoven (Netherlands) and Queen Mary Univ. of London (United Kingdom); Dirk J. Broer, Technische Univ. Eindhoven (Netherlands), for their paper 8682-65, Selective photoresist doped with reactive liquid crystals doped with a dichroic photoinitiator.

The 2013 Diana Nysssonen Memorial Award for the Best Paper was presented to Ozan Ugurlu, Michael Strauss, Gavin Dutrow, Jeff Blackwood, Brian Routh, Corey Senowitz, Pavel Plachinda, Roger Alvis, FEI Co. (USA) for their paper 8681-6, High-volume process monitoring of FEOL 22nm FinFET structures using an automated STEM.
Extreme Ultraviolet (EUV) Lithography VI (AL101)

Conference Chair:

Robert R. Wood II, GLOBALFOUNDRIES Inc.

Conference Co-Chair:

Eric M. Panning, Intel Corp.

Program Committee: Markus Bender, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); Joop Benschop, ASML Netherlands B.V. (Netherlands); Robert L. Brainard, College of Nanoscale Science & Engineering, Univ. at Albany (USA); Li-Jui Chen, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); Daniel A. Corliss, IBM Corp. (USA); Emily E. Gallagher, IBM Corp. (USA); Michael Goldstein, SEMATECH Inc. (USA); Frank Goodwin, SEMATECH Inc. (USA); Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan); Soichi Inoue, EUVL Infrastructure Development Ctr., Inc. (Japan); Bryan S. Kasprowicz, Photronics, Inc. (USA); Insung Kim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Seong-Sue Kim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Bruno La Fontaine, Cymer, Inc. (USA); Michael J. Lercel, SEMATECH Inc. (USA); Ted Liang, Intel Corp. (USA); Chang-Moon Lim, SK Hynix, Inc. (Korea, Republic of); Anna Lio, Intel Corp. (USA); Pawitter J. Mangat, GLOBALFOUNDRIES Inc. (USA); Hiroaki Morimoto, Toppan Printing Co., Ltd. (Japan); Patrick P. Naullleau, Lawrence Berkeley National Lab. (USA); Christopher S. Ngai, Applied Materials, Inc. (USA); Shinji Okazaki, Gigaphoton Inc. (Japan); Uzodinma Okoroanyanwu, Consultant (Germany); Jan Hendrik Peters, Carl Zeiss SMS GmbH (Germany); Jorge J. Roccio, Colorado State Univ. (USA); Kurt G. Ronse, IMEC (Belgium); Tsutomu Shoki, HOYA Corp. (Japan); Akiyoshi Suzuki, Gigaphoton Inc. (Japan); Anna Tchikoulaeva, Lasertec U.S.A., Inc. Zweigniederlassung Deutschland (Germany); Thomas J. Wallow, ASML Brion Technologies (USA); Masaki Yoshioka, Ushio Inc. (Japan)

In 2014 the installation and ramp up of the first group of production EUVL tools will be completed. In 2015 EUV Lithography technology development will require high power sources for full loop process development and optimization. Several critical technical challenges remain, i.e., fielding EUV sources with the power and reliability required for productive exposure tool throughput, mitigating all remaining printable mask blank defects, and developing manufacturing ready resists.

Looking longer term, many important questions with respect to the extendibility of the technology to 7nm and beyond remain unanswered. Chief among these are the roles of advanced resolution enhancement techniques, double-patterning EUVL, higher NA EUV imaging systems, new source technologies like FEL, and resist stochastic effects. Technical and scientific papers advancing the state of the art in EUV Lithography in the following areas are solicited:

**PATTERNING**
- integration learning and OPC
- in fab inspection and control
- double-patterning EUVL
- cost of ownership
- yield.

**MASKS**
- substrates and blanks
- defectivity and inspection
- absorber patterning
- non-flatness compensation
- backside contamination
- reticle handling solutions
- pellicle development and platform integration.

**EXPOSURE TOOLS**
- imaging performance
- focus, dose, and overlay control
- aberrations, flare, and out-of-band light
- optics design and fabrication
- multilayer coatings
- high-NA imaging systems.

**SOURCES**
- power scaling
- efficiency and reliability
- source characterization
- source collectors
- new concepts.

**EUV RESISTS**
- resolution
- line-edge roughness
- sensitivity improvement
- out-of-band sensitivity
- etch transfer
- novel chemistries.

**LIFETIME**
- environment control
- surface contamination
- capping layers
- particle contamination and removal
- cleaning techniques
- resist outgassing.
Alternative Lithographic Technologies VII (AL102)

Conference Chair:
Douglas J. Resnick, Canon Nanotechnologies, Inc. (USA)

Conference Co-Chair:
Christopher Bencher, Applied Materials, Inc. (USA)

Program Committee: Frank E. Abboud, Intel Corp. (USA); Alan D. Brodie, KLA-Tencor Corp. (USA); Kenneth R. Carter, Univ. of Massachusetts Amherst (USA); Joy Y. Cheng, IBM Almaden Research Ctr. (USA); Juan de Pablo, The Univ. of Chicago (USA); Elizabeth A. Dobisz, HGST (USA); Michael A. Guillorn, IBM Thomas J. Watson Research Ctr. (USA); Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan); Daniel J. C. Herr, The Univ. of North Carolina at Greensboro (USA); Tatsuhiko Higashiki, Toshiba Corp. (Japan); James A. Liddle, National Institute of Standards and Technology (USA); Shy-Jay Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); Hans Loeschner, IMS Nanofabrication AG (Austria); John G. Maltabes, Hewlett-Packard Labs. (USA); Dan B. Millward, Micron Technology, Inc. (USA); Laurent Pain, CEA-LETI (France); Ivo W. Rangelow, Technische Univ. Ilmenau (Germany); Benjamen M. Rothsack, Tokyo Electron America, Inc. (USA); Ricardo Ruiz, HGST (USA); Frank M. Schellenberg, Consultant (USA); Helmut Schift, Paul Scherrer Institut (Switzerland); Ines A. Stolberg, Vistec Electron Beam Lithography Group (Germany); Kevin T. Turner, Univ. of Pennsylvania (USA); Marco J. Wieland, MAPPER Lithography (Netherlands); Wei Wu, The Univ. of Southern California (USA); Todd R. Younkin, Intel Corp. (USA)

Our conference showcases novel lithographic and patterning techniques that provide emerging patterning solutions for applications that are scaled (i.e. 16 nm technology ITRS IC nodes and beyond), scaling-independent, or non-IC related. In particular we welcome contributions on hybrid approaches which employ a combination of two or more lithographic techniques. Successful adoption of a technique by one application would synergistically benefit others through improvements in processing capabilities and technological infrastructure, leading to reduced manufacturing costs.

POTENTIAL SOLUTIONS FOR POST OPTICAL LITHOGRAPHIC PATTERNING

DIRECTED SELF-ASSEMBLY (DSA)
- design and integration strategies
- defect management
- registration
- throughput
- pattern transfer fidelity with diblock copolymers
- patterning of NIL templates/masks
- novel 2D and 3D DSA concepts and implementations
- novel materials, such as:
  - phase segregating materials
  - molecular scaffolds, e.g. DNA nanostructures, and molecular nanostructures
  - predictive material, process, and compact models.

ALTERNATIVE PATTERN INTEGRATION TECHNIQUES
- spacer multiple patterning
- self-aligned strategies
- selective deposition.

NANO-IMPRINT LITHOGRAPHY (NIL)
- thermal, UV, J-FIL, and soft imprint lithography
- roll-to-roll large area nano-imprint lithography tooling and design
- resists and novel materials
- alignment and overlay
- defectivity, including defect sources and defect detection
- master and daughter mask/templates: fabrication, metrology, cleaning, and replication
- nanometrology for NIL
- novel imprint processes
- new markets and devices enabled by NIL.

MASK-LESS LITHOGRAPHY (ML2)
- single-beam or multi-beam e-beam lithography (EBL) and ion-beam lithography
- massively parallel multi-beam/multi-pixel EBL for wafer, mask, and template patterning
- electron and ion beam optics
- data path management
- methods of achieving registration and overlay control
- methods of achieving CD and LER control
- materials, such as for electron sources
- high-throughput e-beam resist processes
- resistless e-beam and ion beam patterning.

OTHER NOVEL LITHOGRAPHIC APPROACHES
- ML2 “Desktop Lithography,” such as:
  - plasmonic or nearfield/evanescent wave
  - micromirror optical lithography
  - interferometric patterning
  - large area nanopatterning for rigid and flexible substrates
  - parallel scanning tip-based nanolithography
  - scanning array lithography, dip-pen printing
  - droplet-on-demand inkjet printing.
CALL FOR PAPERS

ALTERNATIVE, NON-IC APPLICATIONS
• bioelectronics and genomics
• photovoltaics and related energy applications
• disk drives and patterned media
• flat panel displays
• optoelectronics and LEDs
• photonic crystals
• negative-refractive-index/meta materials
• nanopatterned sensors
• building blocks for defect tolerant computing
• smart resists and self-healing materials.

In the spirit of facilitating exchange of knowledge, we strongly encourage contributions in which information critical to understanding the topic is discussed.

The program committee will select approximately 10-15 manuscripts that represent conference highlights for consideration to be published in Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3), the world’s premier journal on alternative lithographic technologies. The manuscripts for these 10-15 papers must be included in the conference proceedings. No reformatting is necessary, but manuscripts intended to be reviewed by JM3 must adhere to the generally higher standards of content required of a refereed journal. For more information, please visit http://spie.org/x1833.xml or contact jm3@spie.org

IMPORTANT DATES

Abstracts Due: 8 SEPTEMBER 2014
Author Notification: 20 OCTOBER 2014
Manuscripts Due: 26 JANUARY 2015

Please Note: Submissions imply the intent of at least one author to pay registration, attend the symposium, make the presentation as scheduled, whether it is oral or poster, and submit a full length manuscript for publication in the conference proceedings.

“The conference is invaluable. I have attended almost continuously for the past 25 years and plan to continue for the next 25.”
—2014 Attendee

help@spie.org · TEL: +1 360 676 3290
Metrology, Inspection, and Process Control for Microlithography XXIX (AL103)

Conference Chair:
Jason P. Cain, Advanced Micro Devices, Inc. (USA)

Conference Co-Chair:
Martha I. Sanchez, IBM Research - Almaden (USA)

Program Committee: Ofer Adan, Applied Materials (Israel); John A. Allgair, Nanometrics Inc. (USA); Masafumi Asano, Toshiba Corp. (Japan); Benjamin D. Bundy, SEMATECH Inc. (USA); Alek C. Chen, ASML Taiwan Ltd. (Taiwan); Timothy F. Crimmins, Intel Corp. (USA); Daniel J. C. Herr, The Univ. of North Carolina at Greensboro (USA); Chih-Ming Ke, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); Shunsuke Koshihara, Hitachi High-Technologies Corp. (Japan); Yi-Sha Ku, Industrial Technology Research Institute (Taiwan); Byoung-Ho Lee, Ultratech (USA); Christopher J. Raymond, Nanometrics Inc. (USA); John C. Robinson, KLA-Tencor Corp. (USA); Matthew J. Sendelbach, Nova Measuring Instruments Inc. (USA); Richard Silver, National Institute of Standards and Technology (USA); Eric Solecky, IBM Corp. (USA); Costas J. Spanos, Univ. of California, Berkeley (USA); Alexander Starikov, I&I Consulting (USA); Vladimir A. Ukraintsev, Nanometrology International, Inc. (USA); Alok Vaid, GLOBALFOUNDRIES Inc. (USA)

Metrology-based technology learning, segmentation, and control of the error sources continue to enable rapid evolution of optical microlithography. Direct metrology of exposure dose and focus support ever smaller process windows. Dimensional metrology in layouts facilitates resolution enhancement and validation of control. Extremely tight overlay is required for double exposure. Development of materials, equipment, and processing in EUV lithography, direct write, nano-imprint, and directed self-assembly drive further innovation of metrology tools and applications.

This conference is the leading forum for the exchange of foundational information and discussion of novel concepts in patterning-related metrology and inspection. Consistent with the conference charter and goals, please submit original technical papers in these and related technology areas:

**METROLOGY AND INSPECTION**
- optical full-field and scanned microscopy, scatterometry and interference microscopy
- novel measurement techniques with high-resolution optics, scatterometry, SEM, AFM
- particle-beam scanned microscopy, materials characterization and elemental analysis
- design rules, design compliance, hot spots, design-based metrology and inspection
- metrology for design rules and process margins, budgeting, and budget control
- metrology for lithography development, patterning models build and validation
- metrology on photomasks, including pre-compensation, OPC, and phase shifting
- parametric electrical testing and other device performance-based metrology
- applications in emerging patterning technologies including optical immersion and EUV lithography, direct-write, nano-imprint, and directed self-assembly
- applications in manufacturing of ICs, cell stacking, wafer bonding, TSV and 3D integration, displays, thin-film heads, MEMs, bio-arrays, lab on the chip, integrated optoelectronics.

**CRITICAL DIMENSION, IMAGE PLACEMENT, AND OVERLAY**
- 1D, 2D, and 3D metrology of CD and pattern placement, including within device layouts
- alignment, registration and overlay metrology, processing and metrology integration
- edge profile and edge placement, roughness of edge, width, and centerline
- optical, SEM, and AFM based in-die overlay on small targets and devices.

**CALIBRATION AND ACCURACY**
- metrology quality, error diagnostics, and data culling
- measurement resolution and error, including precision and accuracy
- standards and reference materials, calibration methods, hybrid metrologies
- reference measurement systems and metrology comparisons
- tool fleet performance, maintenance, and matching.
PROCESS CHARACTERIZATION, CONTROL, PERFORMANCE, AND YIELD
• process metrology and monitors, segmentation and reduction of variance
• metrology sampling, excursion detection, costs, device performance, and yield
• data analysis and visualization, process control, feedback and feed forward.

DETECT DETECTION, ANALYSIS, AND CONTROL
• detection and control of pattern defects and across-wafer process variation
• environmental contamination, including impacts on processing and defects
• defect reduction, yield improvement, effective data use.

PERFORMANCE LIMITS IN METROLOGY AND INSPECTION
• responses to commanded skews and cross-technology comparisons
• models of tool-sample interaction, noise, and error mechanisms.

MEASUREMENT SYSTEM MODELING AND SIMULATION
• physics and mathematical models of metrology process and detection methods
• physical characterization of both systems and samples, model parameters
• data analysis methods, library-based image analysis, and algorithms.

THE KAREL URBANEK BEST STUDENT PAPER AWARD
The conference features the Karel Urbanek Best Student Paper Award sponsored by KLA-Tencor Corporation and consists of an SPIE citation and an honorarium. This award recognizes the most promising contribution to the field by a student, based on the technical merit and persuasiveness of the paper presentation at the conference. To be eligible, the leading author and presenter of the paper must be a student. To establish eligibility, the principal author’s bio submitted with the abstract must state the academic status and the institution, as well as the advisor’s name and contact information.

“Best conference if looking for a complete immersion in advances across a wide technical front.”
—2014 Attendee

IMPORTANT DATES
Abstracts Due: 8 SEPTEMBER 2014
Author Notification: 20 OCTOBER 2014
Manuscripts Due: 26 JANUARY 2015

Please Note: Submissions imply the intent of at least one author to pay registration, attend the symposium, make the presentation as scheduled, whether it is oral or poster, and submit a full length manuscript for publication in the conference proceedings.
Advances in Patterning Materials and Processes XXXII (AL104)

Conference Chair:
Thomas I. Wallow, ASML Brion Technologies (USA)

Conference Co-Chair:
Christoph K. Hohle, Fraunhofer Institute for Photonic Microsystems IPMS (Germany)

Program Committee:
Robert Allen, IBM Almaden Research Ctr. (USA); Ramakrishnan Ayothi, JSR Micro, Inc. (USA); Luisa D. Bozano, IBM Almaden Research Ctr. (USA); Sean D. Burns, IBM Corp. (USA); Ralph R. Dammel, AZ Electronic Materials USA Corp. (USA); Roel Gronheid, IMEC (Belgium); Douglas Guerrero, Brewer Science, Inc. (USA); Clifford L. Henderson, Georgia Institute of Technology (USA); Scott W. Jessen, Texas Instruments Inc. (USA); Yoshio Kawai, Shin-Etsu Chemical Co., Ltd. (Japan); Qinghuang Lin, IBM Thomas J. Watson Research Ctr. (USA); Nobuyuki N. Matsuzawa, Sony Corp. (Japan); Katsumi Ohmori, Tokyo Ohka Kogyo Co., Ltd. (Japan); Daniel P. Sanders, IBM Almaden Research Ctr. (USA); Mark H. Somervell, Tokyo Electron America, Inc. (USA); James W. Tackeray, Dow Electronic Materials (USA); Plamen Tzviatkov, FUJIFILM Electronic Materials U.S.A., Inc. (USA); Todd R. Younkin, Intel Corp. (Belgium)

Advances in patterning materials and processes are at the heart of innovation in the semiconductor industry. The development of high-performance resists and the continuous evolution of their applications and processing have been critical enablers for lithography technology improvements for all device generations. The limits of optical lithography have been extended, in no small part, by innovative materials and processes that expand and improve on fundamental resist progress to provide high-resolution, robust, and cost-effective technologies for both mass production and development of future device generations. Evolutionary and ultimately revolutionary innovations will be required in patterning processes and resist materials to achieve the combination of resolution, edge roughness, and sensitivity required for future technology nodes at the needed technological pace.

The Advances in Patterning Materials and Processes conference continues to be the leading forum for scientists and engineers from around the world to present and discuss research on the chemistry, physics, and performance of resist materials. Its scope encompasses the latest advances in patterning materials technology including patterning stack and process innovation, pitch division processes, template processing for self-assembling materials, imprint lithography, non-traditional scaling approaches (3D integration, etc.) and other topics.

The conference welcomes submissions of original papers that emphasize recent advances in high-performance patterning processes and materials and their integration in established, maturing, emerging, and new lithographic technologies. Consistent with the conference’s charter and goals, authors are required to provide a description of chemical and physical principles as well as sufficient chemical structural detail in presented work. Papers which do not reveal sufficient chemical details so as to add value to the readers or are principally of a commercial nature may not be accepted for presentation and publication.

Original technical papers are solicited, but not limited to, the following traditional topics:

**RESISTS AND PROCESSES FOR**
- 193 nm lithography
- EUV lithography
- electron-beam lithography
- negative tone materials
- longer UV wavelengths.

**PATTERNING FILMS AND APPLICATIONS**
- topcoats: contamination control, reflection control
- underlayers: reflection control, pattern transfer, process enhancement
- multilayer integration
- chemistry and materials science of self-assembling materials
- new pattern transfer approaches.

**RESIST APPLICATIONS**
- single and multiple patterning
- implant processing
- templating for self assembly
- thick films for SOC/SIP integration.

**PROCESSING AND PROCESS CONTROL**
- resist smoothing, rectification, trim and shrink
- applied processing, including defect control
- materials challenges related to etch, process control, and metrology
- new processing techniques and applications.

**SIMULATION AND MODELING**
- resist chemistry and processing
- assessment of patterning and materials scaling limits
- variability, stochastics, and pattern formation
- new processes and applications.
Optical Microlithography XXVIII (AL105)

Conference Chair:

Kafai Lai, IBM Corp. (USA)

Conference Co-Chair:

Andreas Erdmann, Fraunhofer-Institut of Integrated Systems and Device Technology (Germany)

Program Committee:

Pary Baluswamy, Micron Technology, Inc. (USA);
Peter D. Brooker, Synopsys, Inc. (USA);
Will Conley, Cymer, Inc. (USA);
Nigel R. Farrar, Cymer Inc. (USA);
Carlos Fonseca, Tokyo Electron America, Inc. (USA);
Bernd Geh, Carl Zeiss SMT Inc. (USA);
Yuri Granik, Mentor Graphics Corp. (USA);
Young Seog Kang, SAMSUNG Electronics Co., Ltd. (Korea, Republic of);
Sachiko Kobayashi, Toshiba Corp. (Japan);
Jongwook Kye, GLOBALFOUNDRIES Inc. (USA);
Tsai-Sheng Gau, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan);
Soichi Owa, Nikon Corp. (Japan);
John S. Petersen, Periodic Structures, Inc. (USA);
Daniel Sarlette, Infineon Technologies Dresden (Germany);
Sam Sivakumar, Intel Corp. (USA);
Bruce W. Smith, Rochester Institute of Technology (USA);
Kazuhiro Takahashi, Canon Inc. (Japan);
Geert Vandenberghe, IMEC (Belgium);
Reinhard Voelkel, SUSS MicroOptics SA (Switzerland)

While EUV lithography is maturing, optical lithography is expected to continue as the primary lithographic technology for manufacturing over the next several years. Extension of water-based immersion lithography to below 32nm half-pitch requires the use of innovative resolution enhancement techniques, solutions to complexities introduced by hyper-NA optics, and extensive use of double or multiple sequential exposure and patterning techniques. The combination of optical lithography for the generation of guiding patterns and directed self-assembly can provide new possibilities for cost effective scaling. In addition to resolution, very tight overlay control and high quality photomasks are also necessary. The successful use of optics to provide viable working solutions for these device nodes will require fundamental integration of all aspects of the patterning process. The cost of advanced lithography is another concern that is in need of creative solutions, such as “freezing” first resist in double patterning approach. This conference welcomes abstract submissions covering topics that are advancing the field of optical nano- and micro lithography.

In addition to optical projection lithography for semiconductor fabrication, submissions are invited that present applications of optical lithography beyond traditional semiconductor fabrication. This includes also alternative optical exposure techniques ranging from mask proximity printing, gray tone techniques, interference lithography and Talbot imaging to innovative direct laser writing techniques such as 2-photon absorption and STED-inspired techniques for 3D patterning.

Specific topics include:

**PUSHING THE LIMITS OF OPTICAL LITHOGRAPHY**

- optical lithography at $k_1 < 0.3$ options
- multiple exposure and multiple masking techniques including requirements and challenges of cut-mask
- novel illumination and mask types
- novel material and process to break optical diffraction limit
- 2-color, 2-photon lithography
- layout regularization and optimization to extend the limits of optical lithography
- design compliance towards multiple patterning/SADP
- complementary Lithography with DSA, e-beam, EUV, imprint to extend resolution for optical lithography.

**LITHOGRAPHIC IMAGING FUNDAMENTALS AND PROCESS INTEGRATION**

- multiple masking in manufacturing: results and issues
- simulation of full systems and process components
- process integration of resolution enhancement methods
- process issues for multiple patterning
- image analysis and assessment
- characterization and minimization of CD and overlay variation
- mask effects on imaging, including mask-induces focus shifts and aberrations
- rigorous modeling of optical, resist and mask effects
- overlay requirements in the context of multiple patterning.

**COMPUTATIONAL LITHOGRAPHY**

- predictive modeling and verification
- fast 3D mask and wafer topography models
- 3D resist and etch modeling for OPC
- advanced pattern correction and OPC
- advanced OPC verification
- advanced pattern matching for hotspot detection
- source mask pupil optimization
- inverse lithography technology (ILT)
- advanced mask decomposition algorithm
- model-based retargeting
- model-based layout modification to compensate process effect.

continued
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LITHOGRAPHY TOOLS AND SUBSYSTEMS
• exposure tools and tracks that support multiple exposure processes
• overlay control down to 2nm, including effects of grid matching
• overlay mark optimization towards product feature placement
• advances in hyper-NA optical design
• tool control for OPC stability and matching
• through multiple layers integrated OPC and tool control
• design and materials issues for imaging
• advances in system design and integration
• novel advances in system self-metrology
• exposure tool and source developments
• illumination metrology and control, including polarization
• evaluation and characterization of lens performance
• metrology systems for set-up, adjustment, and control
• system environmental and contamination control.

LITHOGRAPHY COSTS
• high-throughput tools and processes
• productivity improvement
• process simplifications including “freezing” alternatives
• product layout and cost considerations.

OPTICAL LITHOGRAPHY FOR NON-IC APPLICATIONS
• flat panel and display applications
• silicon photonics
• MEMS, NEMS, and microfluidics
• biological applications
• HDD and patterned media
• flexible electronics
• organic electronics
• lighting, PV and solar
• micro-stereolithography
• holographic applications
• plasmonic applications
• alternative exposure techniques.

IMPORTANT DATES
Abstracts Due:
8 SEPTEMBER 2014
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26 JANUARY 2015

Please Note: Submissions imply the intent of at least one author to pay registration, attend the symposium, make the presentation as scheduled, whether it is oral or poster, and submit a full length manuscript for publication in the conference proceedings.

STUDENT AWARD
Students submitting papers to this conference only, will be considered for the Cymer Scientific Leadership Award for Best Student Paper. This award is given each year at this conference and recognizes extraordinary work achieved by students interested in the microlithography field, and strongly supports the contributions made to scientific advancement at the conference. The award includes a plaque along with a monetary award to help support the student’s future research activities.

If you are/have a student author or co-author that is making the presentation in the Optical Microlithography conference, please send your tracking number to Will Conley at will_conley@cymer.com

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Design-Process-Technology Co-optimization for Manufacturability IX (AL106)

Conference Chair:
John L. Sturtevant, Mentor Graphics Corp. (USA)

Conference Co-Chair:
Luigi Capodieci, GLOBALFOUNDRIES Inc. (USA)

Program Committee: Robert Aitken, ARM Inc. (USA); Jason P. Cain, Advanced Micro Devices, Inc. (USA); Fang-Cheng Chang, Cadence Design Systems, Inc. (USA); Lars W. Liebmann, IBM Corp. (USA); Ru-Gun Liu, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); Mark E. Mason, Texas Instruments Inc. (USA); Andrew R. Neureuther, Univ. of California, Berkeley (USA); Shigeki Nojima, Toshiba Materials Co., Ltd. (Japan); David Z. Pan, The Univ. of Texas at Austin (USA); Chul-Hong Park, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Michael L. Rieger, Synopsys, Inc. (USA); Vivek K. Singh, Intel Corp. (USA); Chih-Min Yuan, Freescale Semiconductor, Inc. (USA)

Process-driven constraints to design have been a reality for multiple generations of semiconductor manufacturing, and design for manufacturability has become a widely adopted spectrum of tools and methods. This conference, aimed at technical and management professionals engaged with the interface between integrated circuit design and manufacturing, invites articles that examine novel approaches for design and process integration aimed at “more Moore” enablement, fast turn-around, cost-effectiveness, and high-yielding integrated circuit (IC) creation.

Contributions should emphasize fundamentals of technical solutions rather than their commercial embodiments. Submissions in design-for-manufacturability, circuit and yield characterization, and other interdisciplinary studies, including but not limited to those based on electronic design automation (EDA), are welcome.

Topics of interest include:

**DESIGN FOR MANUFACTURING**
- physical layout optimization for advanced or novel patterning methodologies
- design and verification methodologies using novel manufacturing models
- layout optimization for systematic and random yield loss reduction
- layout optimization for minimizing circuit variability
- manufacturing friendly circuit design styles and methodologies
- DFM for “more than Moore” applications (analog, RF, digital/SoC, etc.).

**DESIGN-AWARE MANUFACTURING**
- leveraging design-intent information (beyond layout) for RET/OPC application
- propagating electrical design intent for RET/OPC optimization and verification
- performance-power-manufacturability (speed-leakage-RET) optimization.

**DESIGN AND MANUFACTURING CO-OPTIMIZATION**
- design for multipatterning (MP) technology
- design for direct self-assembly (DSA) technology
- design-rule development strategies and methodologies
- layout style and lithography co-optimization (including optical source and design co-optimization
- design-to-process simulation and calibration
- design-to-manufacturing methodologies for analog circuits, MEMs, and other microlithography applications.

**DESIGN-TO-MANUFACTURING ECONOMICS**
- cost-performance tradeoffs between design and manufacturing
- design to manufacturing flow methodologies for productivity improvement, time-to-market, and cost reduction
- new models for maximizing net return on investment in design and manufacturing.

Special consideration will be given to papers that emphasize methodologies for using manufacturing information in the design flow.

Abstracts with a preview of results and conclusions supported by technical data are favored for oral presentation.
**Advanced Etch Technology for Nanopatterning IV (AL107)**

**Conference Chair:**
Qinghuang Lin, IBM Thomas J. Watson Research Ctr. (USA)

**Conference Co-Chair:**
Sebastian U. Engelmann, IBM Thomas J. Watson Research Ctr. (USA)

**Program Committee:**
Julie Bannister, Tokyo Electron America, Inc. (USA); Sang-Hoon Cho, SK Hynix, Inc. (Korea, Republic of); Maxime Daron, LTM CNRS (France); Eric A. Hudson, Lam Research Corp. (USA); Catherine B. Labelle, GLOBALFOUNDRIES Inc. (USA); Nae-Eung Lee, Sungkyunkwan Univ. (Korea, Republic of); Erwine Pargon, LTM CNRS (France); Nicolas Possemé, CEA-LETI (France); Ricardo Ruiz, HGST (USA); Seiji Samukawa, Tohoku Univ. (Japan); Rich Wise, IBM Corp. (USA); Jeff Xu, Qualcomm Technologies Inc. (USA); Anthony Yen, TSMC Taiwan (Taiwan); Ying Zhang, Applied Materials, Inc. (USA)

Nanopatterning with advanced lithographic technologies including 193nm immersion optical lithography, multiple patterning with 193nm immersion lithography, EUV lithography, multi-e-beam direct writing (MEBDW), and alternative lithographic technologies, such as direct self-assembly (DSA) patterning, and nanoprinting lithography, all depend on advanced plasma etch technology, either when directly involved in the lithography technology itself, such as patterning and forming lithography masks, or when transferring lithographical patterns into other layers, such as in the processes of multi-litho and multi-etching lithography patterning, which has been adopted for high-volume manufacturing (HVM) at 45nm technology node and beyond. The increasing importance of interactions and inter-dependence of lithography technologies, photoresist technologies, and plasma etch technologies inevitably makes advanced lithography technology and advanced plasma etch technology more challenging. This situation was the motivation for having an “Advanced Etch Technology for Nanopatterning conference” as a key part of SPIE Advanced Lithography Conferences. After a successful start of three conferences since 2012, this conference will continue to bring lithography and plasma etching communities together to exchange ideas, share new research and development results in these fields, discuss the fundamental understanding and resolve challenges required by the semiconductor industry. Consistent with the conference’s charter and goals, authors are required to provide a description of the chemical and physical principles. Papers which do not reveal sufficient details so as to add value to the readers or are of commercial nature will not be accepted for presentation and publication.

Original and overview technical papers are solicited on the following topics, but not limited to:

- plasma-photoresist interaction, fundamentals, modeling, LER, plasma effects on advanced resists, such as 193i resists, EUV resists, e-beam resists, diblock co-polymers, etc.
- FEOL patterning, such as double patterning(PD)/pitch-splitting(PS), tri-layer schemes, and other alternative lithographic technologies to pattern active areas, gate stacks, FinFET’s Tri-Gates, and other 3D structures, etc.
- MOLE (middle-of-line) patterning, such as PD/PS and tri-layer schemes to pattern contacts for planar devices, 3D devices, local interconnects for advanced technology nodes, etc.
- BEOL patterning, including PD/PS, self-aligned BEOL processes, plasma/low-k and porous ultra-low-k material interactions, patterning process for airgap BEOL, etc.
- advanced memory applications, DRAM, eDRAM, Flash, MRAM, PCM, 3D memories, etc., with 1x nm node patterning
- plasma etching transferring or patterning optical lithographic masks for 139i lithography, EUVL, and alternative lithography technologies
- DSA pattern transfer and other emerging alternative lithography and patterning technologies, e.g., nanoprinting lithography patterning, etc.
- plasma etching/patterning III-V, carbon-based materials, novel 2D materials, and other materials for extreme scaling of CMOS and beyond CMOS era explorations using conventional lithography and alternative lithography technologies
- plasma etching-based transfer or patterning MEMS and other nanostructures, sensors, bio-medical applications using conventional lithography and alternative lithography technologies
- photoresist stripping and clean
- FEOL and BEOL cleaning and substrate preparation
- novel defect reduction or yield improvement techniques by dry plasma cleaning or wet cleaning
- fundamentals of plasma processes and modeling
- advanced plasma sources and emerging plasma etching patterning technologies.
As you submit your manuscript to the conference proceedings, we encourage you to also consider submitting it to the SPIE peer-reviewed *Journal of Micro/Nanolithography, MEMS, and MOEMS* (JM3). Manuscripts submitted to the journal will go through the normal JM3 peer-review process. Revisions are not required for initial submission to the journal, but manuscripts intended to be reviewed by JM3 must adhere to the generally higher standards of content required of a refereed journal and must be prepared according to the journal guidelines. For more information, please visit [http://spie.org/journalpolicies](http://spie.org/journalpolicies) or contact jm3@spie.org.
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The comprehensive Advance Technical Program will list conferences, paper titles, and authors in order of presentation. This piece provides an outline of all planned special events and hotel and registration information.

REGISTRATION
All participants, including invited speakers, contributed speakers, session chairs, co-chairs, and committee members must pay a registration fee. Fee information for conferences, courses, a registration form, and technical and general information will be available on the SPIE website in November 2014.

HOTELS
Opening of the hotel reservation process for Advanced Lithography is scheduled for November 2014. SPIE will arrange special discounted hotel rates for attendees that will be available when housing opens. Please do not call SPIE for information. The SPIE website will be kept current with any updates.

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- Presenters are encouraged to take advantage of the opportunity to submit their completed manuscripts to SPIE's peer-reviewed Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3), the world's premier journal for reporting on Advanced Lithography. For more information, please visit http://spie.org/x1833.xml or contact jm3@spie.org.

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